Distortion in Current Commutating Passive CMOS Downconversion Mixers

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*Abstract—***CMOS passive mixer linearity is analyzed using a** Volterra-series analysis and closed-form expressions for IIP_2 , two-tone IIP₃, and cross-modulation IIP₃ are presented, ex**hibiting dependence upon the mixer source and load impedances. Design guidelines are suggested for improving the mixer linearity performance. Accurate expressions are presented for the input impedance of an ideal passive mixer with an arbitrary load impedance. The calculations are in close agreement with the measured results and the simulated response.**

*Index Terms—***Analog integrated circuits (ICs), CMOS passive mixer, current commutating mixer, intermodulation distortion, passive mixer nonlinearity, Volterra series analysis.**

I. INTRODUCTION

DOWNCONVERTING mixers are an indispensable part
of any modern communication receiver. Active Gilbert mixers have been the mainstay of integrated receiver systems due to their superior gain performance. However, they suffer from voltage headroom limitations and high flicker noise, as technologies scale to sub-100 nm. These drawbacks pose serious challenges in a direct conversion receiver (DCR) design. Despite higher conversion losses, current commutating passive CMOS mixers are preferred in integrated DCR designs, due to their modest headroom requirements and excellent flicker noise performance [1]–[3]. Several detailed studies have been undertaken to address passive mixer design concerns such as noise, dc offset, and second-order distortion [3]–[7]. However, little has been published on the fundamental nonlinear behavior of these current-commutating passive mixers.

An analysis of the intermodulation distortion of current commutating CMOS *active* mixers was presented in [8]. A distortion analysis of MOS track-and-hold sampling mixers involving a time-varying Volterra series analysis was presented in [9]. These analyses cannot be directly applied to current commutating passive mixers since the transistors in passive mixers are biased in deep triode, and the later case assumes voltage commutation (i.e., a high load impedance) and does not account for the effects of source and load impedances.

High-linearity passive mixers are crucial for successful design of CDMA receivers without the interstage RF filter be-

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tween the LNA and mixer. In these receivers, the transmitter (TX) signal leaking into the receiver cross-modulates with a close-in jammer to produce in-band distortion [10]. It is shown in this paper that the mixer linearity is significantly affected by its source and load impedances. We have developed a general distortion theory of current commutating passive field-effect transistors (FET) mixers and establish the relationship between mixer HP_2 , two-tone HP_3 , and cross-modulation (XM) IIP_3 , and its frequency-dependent source and load impedances.

Section II presents the mixer modeling for distortion analysis using a Volterra series, which is presented in Section III. The effects of frequency-varying mixer source and load impedances are analyzed in Section IV. High-frequency effects arising from the transistor capacitances and local oscillator (LO) feedthrough are discussed in Section V. This paper concludes in Section VI with measurement results that confirm the theory.

II. MIXER MODELING

A. Device Modeling

A typical monolithic DCR block diagram is shown in Fig. 1(a). As shown in Fig. 1(b), the low-noise amplifier (LNA) can be modeled as a transconductance stage feeding its output current into the passive mixer. The mixer output current drives the transimpedance amplifier (TIA), which generates the baseband output voltage. Typically, the common-mode feedback loop of the TIA provides the dc bias (V_{CM}) to the input and output terminals of the mixer. Due to the ac coupling capacitor (C_c) between the LNA output and the mixer input, the transistors in the mixer are biased in the deep triode region with $V_{DS} = 0$. We assume that the transistor gates are driven by an ideal square wave LO signal.

Due to symmetric dependence of the drain current I_D , either of the terminals can be assumed to be the drain or the source [11]. Hence, without loss of generality, we assume the input node to be the source S and the output node to be the drain D . It is crucial to choose a correct MOS model for analyzing the passive mixer nonlinearity. At the $V_{\text{DS}} = 0$ bias, the industry standard models like BSIM3v3, BSIM4, Philips MM9, and EKV models deviate from the measured results, due to discontinuities in the higher order derivatives of drain current and terminal charges [12]–[15]. The latest surface potential-based model, PSP [16] and the next-generation BSIM model BSIM5 [17], [18] use a single equation to define the drain current across all biasing conditions and have continuous first and higher derivatives.

The models are typically tested for Gummel symmetry [19], where equal and opposite voltages are applied at the source and drain terminals of the MOSFET and drain current is measured

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Fig. 1. (a) Receiver block diagram. (b) Simplified receiver model.

Fig. 2. Schematic for dc analysis of an NMOS transistor.

(Fig. 2). The drain current and its first-, second-, and third-order derivatives with respect to V_{DS} are plotted in Fig. 3 for BSIM3v3 and PSP models. The second-order derivative of I_D shows discontinuity at $V_{DS} = 0$ for the BSIM3v3 model and this has been asserted as the reason behind the anomalous third-order distortion slope of $2:1$, instead of $3:1$, in passive mixer simulations [20], [21]. Hence, the PSP model was chosen for the simulation results presented in this paper.

B. Nonlinearity Modeling

The primary sources of nonlinearity in a passive CMOS mixer driven by a square-wave LO are the: 1) nonzero rise and fall time of the LO; 2) nonlinear device capacitances C_{gs} and C_{gd} ; and 3) the nonlinear I_D versus V_{DS} relationship.

At lower microwave frequencies, a square-wave LO can be faithfully achieved in an integrated circuit (IC) environment, and hence, the contributions from the finite rise time and nonlinear capacitances are negligible for short gate-length devices. Those sources have been initially ignored; but at higher frequencies, these effects can be nonnegligible and their impact is discussed later in Section V. The receiver model in Fig. 1(b) can be further simplified to Fig. 4(a). The double-balanced passive mixer is assumed to be driven by an ideal square-wave LO with a 50% duty cycle. The LNA output is modeled as an ideal current source i_{RF} , shunted by impedance Z_{S} , which acts as a signal source for the mixer. Similarly, the TIA input is represented by the load impedance Z_L . In practice, the LNA load is typically a shunt LC tank terminated at V_{DD} , and the output buffer of the TIA provides the ground termination to Z_L ; hence, a common-mode

Fig. 3. I_D and first three derivatives with respect to V_{DS} for a MOSFET transistor simulated with BSIM3v3 and PSP models. The source and drain voltages are equal and opposite (Fig. 2). $V_{GG} = 1.5$ V and the transistor size is 50 μ m/0.18 μ m.

ground is justified. Additional differential capacitances at the mixer output (not shown here) filter off the high-frequency signals and have been ignored in this analysis, as they do not affect the signal and the intermodulation distortion tones.

The mixer operation can be analyzed by expressing the mixer input and output voltages as weakly nonlinear Volterra series expanded about the periodically varying LO voltage [22]. The series coefficients are time varying; however, for low-frequency operation relative to the f_t of the transistor, the memory elements in the mixer and the load impedance can be ignored and the coefficients are assumed to be constants. Each transistor can be modeled as a nonlinear transconductance q_{NL} in series with an ideal switch, as shown in Fig. 4(b). Assuming no device mismatches and nonoverlapping LO waveforms, the circuit can be further simplified to Fig. 4(c), where $Z_{L,\text{RF}}$ refers to the load impedance Z_L transformed into the RF domain. The relationship between $Z_{L,\text{RF}}$ and Z_L is developed later in Section IV. Due to its symmetry, the circuit can be further simplified to its single-ended version in Fig. 4(d).

III. MIXER LINEARITY ANALYSIS

In general, the large-signal drain current i_D is a function of the drain and source voltages referred to the bulk, rather than the large-signal drain–source voltage v_{DS} . Hence, i_D can be expressed as

$$
i_D = g_1 v_D + g_{2_D} v_D^2 + g_{3_D} v_D^3 + \cdots
$$

\n
$$
- g_1 v_S + g_{2_S} v_S^2 + g_{3_S} v_S^3 + \cdots
$$

\n
$$
+ g_{2_{D\&S}} v_D v_S + g_{3_{D\&S}} v_D^2 v_S
$$

\n
$$
+ g_{3_{D\&S}} v_D v_S^2 + \cdots
$$

\n(1)

where v_D and v_S are the large-signal drain and source voltages of the MOSFET referred to the bulk, respectively. By symmetry, the coefficients of v_D and v_S are equal and opposite. All the coefficients in (1) depend on the process technology, gate bias voltage, and transistor size. Assuming q_{NL} to be a weakly nonlinear conductance, fourth-order and higher order terms in (1)

Fig. 4. (a) Double-balanced passive MOSFET mixer. (b) Passive FET mixer with transistors modeled as nonlinear conductances and ideal switches. (c) Simplified model of (b) for nonoverlapping LO^+ and LO^- and real load impedance. (d) Single-ended equivalent model of the mixer.

have been ignored. Hence, in Fig. 4(d), the input and output voltages can be expressed as a converging Volterra series of the source current i_{RF} . Thus,

$$
v_S = H_{1_S}(s) \circ i_{\text{RF}} + H_{2_S}(s_1, s_2) \circ i_{\text{RF}}^2 + H_{3_S}(s_1, s_2, s_3) \circ i_{\text{RF}}^3 + \cdots
$$
 (2a)

$$
v_D = H_{1_D}(s) \circ i_{\text{RF}} + H_{2_D}(s_1, s_2) \circ i_{\text{RF}}^2 + H_{3_D}(s_1, s_2, s_3) \circ i_{\text{RF}}^3 + \cdots
$$
 (2b)

where H_{n_S} and H_{n_D} are the *n*th-order Volterra kernels for the input and the output nodes, respectively. The first-order Volterra kernels are

 $\Delta(s) = g_1 g_S(s) + g_S(s) g_L(s) + g_L(s) g_1$

$$
H_{1_S}(s) = \frac{g_1 + g_L(s)}{\Delta(s)}
$$
 (3a)

$$
H_{1_D}(s) = \frac{2}{\pi} \frac{g_1}{\Delta(s)}
$$
 (3b)

where

Fig. 5. Schematic for computation of the second-order (and third-order) Volterra kernels.

and the $2/\pi$ factor is added to $H_{1_D}(s)$ to account for the doublebalanced mixer gain. The second-order Volterra kernels can be obtained by solving for the node voltages in Fig. 5. The nonlinear current source i_{NL2} is a function of the first-order Volterra kernels [23], and is given by

$$
i_{\rm NL2} = \frac{1}{\Delta(s_1)\Delta(s_2)} \Biggl\{ g_{2_D} g_1^2 + g_{2_S} (g_1 + g_L(s_1)) (g_1 + g_L(s_2)) + g_{2_{D\&S}} g_1 \left(g_1 + \frac{g_L(s_1) + g_L(s_2)}{2} \right) \Biggr\}.
$$
\n
$$
(5)
$$

Solving the circuit in Fig. 5 yields

$$
H_{2_S}(s_1, s_2) = \frac{g_L(s_1 + s_2)}{\Delta(s_1 + s_2)} i_{\text{NL2}}(s_1, s_2)
$$
 (6a)

$$
H_{2_D}(s_1, s_2) = -\frac{2}{\pi} \frac{g_S(s_1 + s_2)}{\Delta(s_1 + s_2)} i_{\text{NL2}}(s_1, s_2).
$$
 (6b)

In a similar fashion, the third-order nonlinear current can be computed with i_{NL3} as the current source. The third-order Volterra kernels are

$$
H_{3_S}(s_1, s_2, s_3) = \frac{g_L(s_1 + s_2 + s_3)}{\Delta(s_1 + s_2 + s_3)}
$$

\n
$$
\times i_{\text{NL3}}(s_1, s_2, s_3)
$$

\n
$$
H_{3_D}(s_1, s_2, s_3) = -\frac{2}{\pi} \frac{g_S(s_1 + s_2 + s_3)}{\Delta(s_1 + s_2 + s_3)}
$$

\n
$$
\times i_{\text{NL3}}(s_1, s_2, s_3).
$$
 (7b)

 $i_{\rm NL3}$ can be computed from lower order Volterra kernels, as outlined in [23].

A. HP_2 and HP_3

For two input signals at frequencies ω_1 and ω_2 , the secondorder input intercept point HP_2 refers to the input power when the output power due to second-order intermodulation distortion $P_{\text{out}}(\omega_1 - \omega_2)$ equals the fundamental output power $P_{\text{out}}(\omega_{\text{LO}} \omega_1$). Analytically,

$$
IIP2 = \frac{P_{\text{out}}(\omega_{\text{LO}} - \omega_1)}{P_{\text{out}}(\omega_1 - \omega_2)} P_{\text{in}}(\omega_1)
$$

$$
= \left\{ \frac{v_D(\omega_{\text{LO}} - \omega_1)}{v_D(\omega_1 - \omega_2)} \right\}^2 P_{\text{in}}(\omega_1)
$$
(8)

(4) where P_{in} is the input power, and v_D is the single-ended drain voltage. Similarly, the third-order intermodulation distortion Authorized licensed use limited to: Univ of Calif San Diego. Downloaded on October 20,2024 at 11:27:28 UTC from IEEE Xplore. Restrictions apply.

due to two tones at ω_1 and ω_2 appears at $2\omega_1 - \omega_2$. For this downconverter, it can be expressed as

$$
IIP_3 = \left\{ \frac{P_{\text{out}}(\omega_{\text{LO}} - \omega_1)}{P_{\text{out}}(\omega_{\text{LO}} - (2\omega_1 - \omega_2))} \right\}^{1/2} P_{\text{in}}(\omega_1)
$$

=
$$
\frac{v_D(\omega_{\text{LO}} - \omega_1)}{v_D(\omega_{\text{LO}} - (2\omega_1 - \omega_2))} P_{\text{in}}(\omega_1).
$$
 (9)

The single-ended fundamental, second-order, and third-order intermodulation distortion voltages at the mixer output can be evaluated as

$$
v_D(s_{\text{LO}} - s_1) = H_{1_D}(s_1)i_{\text{RF}}(s_1)
$$
 (10a)

$$
\times i_{\text{RF}}^2(s_1, s_2) \qquad (10b)
$$

$$
v_D(s_{\text{LO}} - (2s_1 - s_2)) = \frac{3}{4} H_{3D}(s_1, s_1, -s_2)
$$

$$
\times i_{\text{RF}}^3(s_1, s_1, -s_2). \quad (10c)
$$

Keeping in mind that $|Z_S|$ is typically much greater than both $1/g_1$ and $|Z_{L,\text{RF}}|$, we can, therefore, assume that

$$
g_S(s_1), g_S(s_1 - s_2), g_S(2s_1) \ll g_L(s_1)
$$
 (11a)

$$
g_L(-s_2) \approx g_L(s_1) \tag{11b}
$$

$$
\Delta(s_i) \approx g_1 g_L(s_i) \qquad (11c)
$$

and the simplified expressions for H_{2_D} and H_{3_D} are given by

$$
H_{2_D}(\omega_1, -\omega_2)
$$

\n
$$
\approx -\frac{g_S(\omega_1 - \omega_2)}{g_L^2(\omega_1)g_L(\omega_1 - \omega_2)}
$$

\n
$$
\times [A_2 g_L^2(\omega_1) + A_1 g_L(\omega_1) + A_0]
$$

\n
$$
H_{2D}(\omega_1 \omega_2 - \omega_2)
$$
\n(12a)

$$
\approx -\frac{2}{\pi} \frac{g_S(2\omega_1 - \omega_2)}{g_1^5 g_L^3(\omega_1) g_L(2\omega_1 - \omega_2)} \times \left[B_3 g_L^3(\omega_1) + B_2 g_L^2(\omega_1) + B_1 g_L(\omega_1) + B_0 \right] \tag{12b}
$$

where the coefficients A_n 's and B_n 's are defined in Appendix II.

For verification, the circuit in Fig. 4(a) was simulated and the single-ended fundamental $IMD₂$ and $IMD₃$ components of the mixer output voltage were compared with the calculated values. As we assumed low-frequency operation, all the simulation were carried out at LO frequency of 1 MHz to show the excellent agreement with the calculations. Later, in Section V, mixer single-ended HP_2 and HP_3 are plotted against frequency to show that there is less than 3-dB variation up to 1 GHz. The device parameters in (1) were estimated from the dc analysis using the technique described in Appendix I. Fig. 6 shows an excellent agreement between the simulation and calculation.

For the differential operation, the fundamental and third-order voltages will be doubled, while the second-order voltage will cancel and can be represented as

$$
v_D(\omega_1 - \omega_2) = -\frac{g_S(\omega_1 - \omega_2)}{g_L^2(\omega_1)g_L(\omega_1 - \omega_2)} \times \left[\Delta_2 g_L^2(\omega_1) + \Delta_1 g_L(\omega_1) + \Delta_0\right] i_{\rm RF}^2(s_1, s_2)
$$
\n(13)

Fig. 6. Comparison between simulated (using PSP model) and calculated [using (10a)–(10c)] single-ended fundamental, second-order, and third-order intermodulation distortion signals for the mixer operated at low frequencies. P_{in} is the input to the LNA with $g_{m,\text{LNA}} = 30 \text{ mS}$ in Fig. 1(a). The mixer source and load impedances are 500 Ω and 5 Ω , respectively.

where Δ_n 's are the differences between A_n 's for the positive and negative mixer output terminals. This difference can be nonzero due to the mismatches and imbalances in the mixer, LO circuitry, and signals. In an ideal case with no mismatches, the Δ_n 's are zero, resulting in zero $v_D(\omega_1 - \omega_2)$ and infinite $HP₂$.

Assuming a 50- Ω match at the LNA input in Fig. 1(a), the LNA input power can be expressed as

$$
P_{\rm in} = \frac{i_{\rm RF}^2}{50g_{m,\rm LNA}^2}.\tag{14}
$$

Thus, the second- and third-order input intercept points are given by

$$
IIP_2(W) = \left\{ \frac{v_D(\omega_{LO} - \omega_1)}{v_D(\omega_1 - \omega_2)} \right\}^2 \frac{i_{RF}^2}{50g_{m,\text{LNA}}^2}
$$

$$
\approx \frac{1}{50g_{m,\text{LNA}}^2} \times \left\{ \frac{g_L(\omega_1)g_L(\omega_1 - \omega_2)}{g_S(\omega_1 - \omega_2)} \right\}^2
$$

$$
\times \left[\Delta_2 g_L^2(\omega_1) + \Delta_1 g_L(\omega_1) + \Delta_0 \right]^{-2} \tag{15a}
$$

$$
IIP3(W) = \frac{v_D(\omega_{LO} - \omega_1)}{v_D(\omega_{LO} - (2\omega_1 - \omega_2))} \frac{i_{RF}^2}{50g_{m, LNA}^2}
$$

\n
$$
\approx \frac{2}{75g_{m, LNA}^2} \times \frac{g_1^5 g_L^2(\omega_1)g_L(2\omega_1 - \omega_2)}{g_S(2\omega_1 - \omega_2)}
$$

\n
$$
\times [B_3 g_L^3(\omega_1) + B_2 g_L^2(\omega_1) + B_1 g_L(\omega_1) + B_0]^{-1}.
$$

\n(15b)

B. XM

The XM distortion is the most significant distortion mechanism in CDMA receivers, where the modulated TX signal in the receiver path cross-modulates with a close-in jammer to produce in-band distortion [10]. This can be modeled by representing the close-in jammer as a single tone at ω_1 and the modulated TX signal as two closely spaced tones at ω_2 and ω_3 ; the distortion

1

being at $\omega_1 + \omega_2 - \omega_3$. Let the IIP₃ due to these three tones be defined as

$$
IIP3,XM(W)
$$

= $K_{\text{XM}}P_{\text{in}}(\omega_1)$

$$
\times \left\{ \frac{P_{\text{out}}(\omega_{\text{LO}} - \omega_1)}{P_{\text{out}}(\omega_{\text{LO}} - (\omega_1 + \omega_2 - \omega_3))} \right\}^{1/2}
$$

= $K_{\text{XM}} \frac{v_D(\omega_{\text{LO}} - \omega_1)}{v_D(\omega_{\text{LO}} - (\omega_1 + \omega_2 - \omega_3))} P_{\text{in}}(\omega_1)$ (16)

where K_{XM} is a constant dependent on the spectral shape of the modulated signal [10]. The distortion voltage $v_D(\omega_{LO} - (\omega_1 +$ $(\omega_2 - \omega_3)$ relates to the third-order Volterra kernel as

$$
v_D(\omega_{\text{LO}} - (\omega_1 + \omega_2 - \omega_3)) = \frac{3}{2} H_{3_D}(\omega_1, \omega_2, -\omega_3)
$$

$$
\times i_{\text{RF}}^3(\omega_1, \omega_2, -\omega_3). \quad (17)
$$

 $H_{3n}(\omega_1, \omega_2, -\omega_3)$ can be simplified by assuming (11a)–(11c) in addition to

$$
g_L(-\omega_3) \approx g_L(\omega_2) \tag{18a}
$$

$$
g_L(\omega_1 + \omega_2) \approx \infty \tag{18b}
$$

$$
g_L(\omega_1 - \omega_3) \approx \infty \tag{18c}
$$

$$
g_L(\omega_2 - \omega_3) \approx \infty. \tag{18d}
$$

Equation (18a) is justified since ω_2 and ω_3 are close together and the load impedance is assumed to be real, while (18b)–(18d) imply that the load impedance at high frequency is assumed to be zero, which is justified due to large filtering capacitances at the mixer output. The simplified $H_{3n}(\omega_1, \omega_2, -\omega_3)$ is given by

$$
H_{3D}(\omega_1, \omega_2, -\omega_3)
$$

\n
$$
\approx \frac{g_S(\omega_1 + \omega_2 - \omega_3)}{3g_1^5 g_L(\omega_1)g_L^2(\omega_2)g_L(\omega_1 + \omega_2 - \omega_3)}
$$

\n
$$
\times \left[C_{3}g_L(\omega_1)g_L^2(\omega_2) + C_{2}g_L(\omega_1)\{g_L(\omega_2) + 2g_L(\omega_1)\} + C_1\{g_L(\omega_2) + 2g_L(\omega_1)\} + C_0\right]
$$
(19)

where the C_n 's, as defined in Appendix II, are independent of the source and load impedances. Equation (20) gives the intercept point for the XM distortion as follows:

$$
\Pi P_{3,XM} \n\approx \frac{K_{\text{XM}}}{25g_{m,\text{LNA}}} \frac{g_1^5 g_L^2(\omega_2)g_L(\omega_1 + \omega_2 - \omega_3)}{g_S(\omega_1 + \omega_2 - \omega_3)} \n\times \left[C_{3}g_L(\omega_1)g_L^2(\omega_2) + C_{2}g_L(\omega_1)\{g_L(\omega_2) + 2g_L(\omega_1)\} + C_1\{g_L(\omega_2) + 2g_L(\omega_1)\} + C_0 \right]^{-1}.
$$
\n(20)

From (15a), (15b), and (20), it can be shown that the mixer linearity improves by increasing q_1 , assuming that the derivatives of g_1 scale proportionally. However, this may have an adverse effect on the system noise performance and the LO power consumption. Typically, an optimal transistor size and LO swing should be chosen by iteratively optimizing over these specifications.

IV. EFFECT OF SOURCE AND LOAD IMPEDANCES ON MIXER LINEARITY

A. Computation of Mixer Input Impedance

 $Z_{L,RF}$ is the input impedance of an ideal passive mixer with load impedance Z_L , as shown in Fig. 7(a). For this analysis, the mixer is driven by an ideal square wave LO with frequency ω_{LO} , and i_{test} is an ideal single-tone current source with amplitude A and frequency $\omega_{\rm in}$. The current at the load is given by multiplying the i_{test} with a periodic square wave function f_{sw} . Analytically,

$$
i_{\text{out}}(t) = i_{\text{test}}(t) f_{\text{sw}}(t)
$$

= $\frac{2A}{\pi} \sum_{n=1,3,5...}^{\infty} \frac{1}{n} \left(\sin(n\omega_{\text{LO}} + \omega_{\text{in}})t + \sin(n\omega_{\text{LO}} - \omega_{\text{in}})t \right).$ (21)

The output voltage $v_{\text{out}}(t)$ across nodes O^+ and O^- can be computed as the product of $i_{\text{out}}(t)$ and $2Z_L(\omega)$

$$
v_{\text{out}}(t) = \frac{2A}{\pi} \sum_{n=1,3,5...}^{\infty} \times \frac{1}{n} [2|Z_L(n\omega_{\text{LO}} + \omega_{\text{in}})|\sin((n\omega_{\text{LO}} + \omega_{\text{in}})t + \theta_1) + 2|Z_L(n\omega_{\text{LO}} - \omega_{\text{in}})|\sin((n\omega_{\text{LO}} - \omega_{\text{in}})t + \theta_2)]
$$
\n(22)

where θ_1 and θ_2 are arguments of $Z_L(n\omega_{LO} + \omega_{in})$ and $Z_L(n\omega_{LO} - \omega_{\rm in})$, respectively. The same mixer can be envisaged as a voltage commutator with $v_{\text{out}}(t)$ as the source voltage and $v_{\text{test}}(t)$ as the voltage across the open load [see Fig. 7(b)]. Hence,

$$
v_{\text{test}}(t)
$$

= $v_{\text{out}}(t) f_{\text{sw}}(t)$
= $\frac{4A}{\pi^2} \sum_{n=1,3,5...}^{\infty} \sum_{m=1,3,5...}^{\infty}$
 $\times \frac{1}{nm} [2|Z_L(n\omega_{\text{LO}} + \omega_{\text{in}})|\cos(((n-m)\omega_{\text{LO}} + \omega_{\text{in}})t + \theta_1)$
-2|Z_L(n\omega_{\text{LO}} + \omega_{\text{in}})|\cos(((n+m)\omega_{\text{LO}} + \omega_{\text{in}})t + \theta_1)
+2|Z_L(n\omega_{\text{LO}} - \omega_{\text{in}})|\cos(((n-m)\omega_{\text{LO}} - \omega_{\text{in}})t + \theta_2)
-2|Z_L(n\omega_{\text{LO}} - \omega_{\text{in}})|\cos(((n+m)\omega_{\text{LO}} - \omega_{\text{in}})t + \theta_2)]. (23)

Using an approach similar to the conversion matrix approach [24], the input impedance $Z_{L,RF}$ can be computed by finding the coefficient of $\cos \omega_{\rm in} t$ in (23), which is given by

$$
Z_{L,RF} = \frac{4}{\pi^2} \sum_{n=1,3,5...}^{\infty} \frac{1}{n^2} \left[|Z_L(n\omega_{LO} + \omega_{in})|e^{j\theta_1} + |Z_L(n\omega_{LO} - \omega_{in})|e^{-j\theta_2} \right]
$$

$$
= \frac{4}{\pi^2} \sum_{n=1,3,5...}^{\infty} \frac{1}{n^2} \left[Z_L(n\omega_{LO} + \omega_{in}) + Z_L^*(n\omega_{LO} - \omega_{in}) \right].
$$
 (24)

Fig. 7. (a) Ideal current commutating mixer schematic with current source and load impedance. (b) The same mixer acts as an ideal voltage commutating mixer having open load with voltage v_{test} across it.

For a resistive load R_L , this results in

$$
Z_{L,\text{RF}} = \frac{4}{\pi^2} \left[2R_L \sum_{n=1,3,5...}^{\infty} \frac{1}{n^2} \right] = R_L.
$$
 (25)

Whereas for a capacitive load, the higher order terms $(n > 1)$ can be ignored. Thus,

$$
Z_{L,\text{RF}} \approx \frac{4}{\pi^2} \left[\frac{1}{j(\omega_{\text{LO}} + \omega_{\text{in}})C} + \frac{1}{-j(\omega_{\text{LO}} - \omega_{\text{in}})C} \right]
$$

$$
= \frac{j8}{\pi^2 C} \frac{\omega_{\text{in}}}{\omega_{\text{LO}}^2 - \omega_{\text{in}}^2}.
$$
(26)

Specifically,

$$
Z_{L,\text{RF}} \approx \begin{cases} \frac{4}{\pi^2} \cdot \frac{1}{j(\omega_{\text{in}} - \omega_{\text{LO}})C}, & \omega_{\text{in}} \approx \omega_{\text{LO}}\\ \frac{8}{\pi^2} \cdot j\omega_{\text{in}} \Big(\frac{1}{\omega_{\text{LO}}^2 C}\Big), & \omega_{\text{in}} \approx 0. \end{cases}
$$
(27)

This suggests that for a capacitive load at the mixer output, a very large reactive impedance at the mixer input when $\omega_{\text{in}} \approx \omega_{\text{LO}}$ is observed [7]. While at much lower input frequencies, a capacitive load appears as inductive at the mixer input. Fig. 8 depicts the normalized simulated and the calculated input impedance for an ideal mixer with a capacitive load.

The expression for $Z_{L,\text{RF}}$ can be simplified by observing that in a typical zero or low IF receiver design, large capacitances are placed at the mixer output to shunt away any undesired high-frequency signals. This implies that $Z_L(\omega_{\text{LO}} + \omega_{\text{in}})$ is negligible. Thus, (24) can be further simplified to

$$
Z_{L,\text{RF}} \approx \frac{4}{\pi^2} \left[Z_L^*(\omega_{\text{LO}} - \omega_{\text{in}}) \right]. \tag{28}
$$

Intuitively, this suggests that the load impedance is scaled and frequency translated by ω_{LO} at the mixer input. Thus,

$$
g_L(\omega) \approx \frac{\pi^2}{4} \frac{1}{Z_L^*(\omega_{\text{LO}} - \omega)}.\tag{29}
$$

Fig. 8. Normalized simulated and calculated [using (26)] input impedance for a capacitive load of 1 nF with 1-MHz LO frequency for a passive mixer with ideal switches.

Hence, for a frequency-dependent resistive load impedance, the HP_2 , HP_3 , and $\text{HP}_{3,XM}$ can be computed using (15), (20), and (29) as

$$
\text{IIP}_{2} \approx K_{a} \left\{ \frac{Z_{L}(\omega_{1})Z_{S}(\omega_{1} - \omega_{2})}{Z_{L}(\omega_{1} - \omega_{2})} \right\}^{2}
$$
\n
$$
\times \left[\Delta_{2}' + \Delta_{1}' Z_{L}(\omega_{LO} - \omega_{1}) + \Delta_{0}' Z_{L}^{2}(\omega_{LO} - \omega_{1}) \right]^{-2} \tag{30a}
$$
\n
$$
\text{IIP}_{3} \approx K_{b} \times \frac{Z_{L}(\omega_{LO} - \omega_{1})Z_{S}(2\omega_{1} - \omega_{2})}{Z_{L}(\omega_{LO} - (2\omega_{1} - \omega_{2}))} \times \left[B_{3}' + B_{2}' Z_{L}(\omega_{LO} - \omega_{1}) + B_{1}' Z_{L}^{2}(\omega_{LO} - \omega_{1}) + B_{0}' Z_{L}^{3}(\omega_{LO} - \omega_{1}) \right]^{-1} \tag{30b}
$$
\n
$$
\text{IIP}_{3,XM} \approx K_{x} \frac{Z_{L}^{2}(\omega_{LO} - \omega_{1})Z_{S}(\omega_{1} + \omega_{2} - \omega_{3})}{Z_{L}(\omega_{LO} - (\omega_{1} + \omega_{2} - \omega_{3}))} \times \left[C_{3}' Z_{L}(\omega_{LO} - \omega_{1}) + C_{2}' Z_{L}(\omega_{LO} - \omega_{2}) \right] \times \left\{ Z_{L}(\omega_{LO} - \omega_{1}) + 2Z_{L}(\omega_{LO} - \omega_{2}) \right\}
$$

+
$$
C'_1 Z_L(\omega_{LO} - \omega_1) Z_L(\omega_{LO} - \omega_2)
$$

\n× $\{Z_L(\omega_{LO} - \omega_1) + 2Z_L(\omega_{LO} - \omega_2)\}$
\n+ $C'_0 Z_L^2(\omega_{LO} - \omega_1) Z_L^2(\omega_{LO} - \omega_2)\right]^{-1}$ (30c)

where K_a , K_b , and K_x are independent of the load and source impedances, and

$$
\Delta'_n = \left(\frac{\pi^2}{4}\right)^n \Delta_n,\tag{31a}
$$

$$
B'_n = \left(\frac{\pi^2}{4}\right)^n B_n \tag{31b}
$$

$$
C'_n = \left(\frac{\pi^2}{4}\right)^n C_n.
$$
 (31c)

B. Effect of Source Impedance on Mixer Linearity

Equation (30a) highlights the dependence of the second-order intercept point on the load and source impedances. It suggests

Fig. 9. Simulated (using PSP model) and calculated low-frequency HP_3 variation with the mixer source impedance. The RF tone power at the input of Fig. 9. Simulated (using PSP model) and calculated low-frequency IIP₃ variation with the mixer source impedance. The RF tone power at the input of the LNA is -50 dBm with $g_{m,LNA} = 30$ mS in Fig. 1(a). The mixer load the LNA is -50 dBm with $g_{m,\text{LNA}} = 30 \text{ mS}$ in Fig. 1(a). The mixer load impedance is 5 Ω , the transistor g_1 is 76 mS, and the square wave LO frequency is 1 MHz.

that for good IIP₂, $|Z_S(\omega_1 - \omega_2)|$ should be as large as possible. Physically, a low source impedance at $(\omega_1 - \omega_2)$ amplifies the IMD_2 currents due to the mismatches in the mixer transistors or LO signals. In a typical receiver, the parasitic capacitances at the LNA–mixer interface can lower the input impedance. Hence, in a receiver design with an inductive LNA load, it is desired to resonate any capacitance at the LNA output node. Additionally, an ac coupling capacitor between the LNA and the mixer can boost the mixer source impedance at $(\omega_1 - \omega_2)$, while passing the RF signal [25]. For a noninductive LNA load, it might be desirable to place additional series resistance at the interface to improve HP_2 [26].

Equations (30b) and (30c) also reflect that, to improve both the two-tone HP_3 and XM $\text{HP}_{3,XM}$, the source impedance at the RF signal frequency should be as high as possible. This effect is verified in Fig. 9, which shows the simulated and the calculated IIP_3 against the mixer source impedance Z_S .

As depicted in Fig. 10, for an LNA with an inductive load L and quality factor Q , the mixer source impedance is constrained by

$$
|Z_S| < |\omega L Q|.\tag{32}
$$

To maximize $|Z_{S}|$ a large high-Q inductor is desired, which resonates with shunt capacitances at the signal frequency, i.e.,

$$
L = \frac{1}{\omega_{\text{RF}}^2 (C_{\text{tune}} + C_{\text{par}})}\tag{33}
$$

where C_{tune} and C_{par} are the tuning and parasitic capacitors at the LNA output, respectively (Fig. 9). Hence, for achieving high linearity, it is highly desired to minimize the parasitic capacitances at the LNA output node so that a larger inductor can be accommodated while having some additional tuning capacitance.

C. Effect of Load Impedance on Mixer Linearity

A passive mixer is typically cascaded with a TIA, as shown in Fig. 1. Thus, the mixer load impedance is low at dc, but in-

Fig. 10. Constraints on the mixer source impedance for maximizing the linearity of a passive mixer preceded by a cascode CMOS LNA with an inductive load.

Fig. 11. Simulated (using PSP model) and calculated low-frequency HP_2 and $\overline{\text{HP}}_3$ variation with mixer load impedance. The RF tone power at the input of Fig. 11. Simulated (using PSP model) and calculated low-frequency HP_2 and HP_3 variation with mixer load impedance. The RF tone power at the input of the LNA is -50 dBm with $g_{m,\text{LNA}} = 30$ mS in Fig. 1(a). The the LNA is -50 dBm with $g_{m,\text{LNA}} = 30 \text{ mS}$ in Fig. 1(a). The mixer source impedance is 500 Ω , the transistor g_1 is 76 mS, and the square wave LO frequency is 1 MHz.

creases rapidly with frequency as the open-loop TIA gain drops. Hence, the downconverted jammers outside the desired signal band encounter a relatively high TIA input impedance.

From (30a)–(30c), it is evident that $|Z_L(\omega_{\text{LO}} - (\omega_1 - \omega_2))|$, $|Z_L(\omega_{\text{LO}} - \omega_{\text{RF}})|$, and $|Z_L(\omega_{\text{LO}} - \omega_1)|$ should all be minimized simultaneously to maximize HP_2 and HP_3 . The first term corresponds to a load impedance at high frequency, which is small due to the large filtering capacitors at the mixer output. The second term $Z_L(\omega_{\text{LO}} - \omega_{\text{RF}})$ corresponds to the load impedance at baseband, which is small due to the low input impedance of the TIA. The frequency $(\omega_{LO} - \omega_1)$ refers to the downconverted jammer frequency where the TIA input impedance may be high due to the finite open-loop bandwidth of the amplifier, especially for out-of-band jammers. Fig. 11 shows the simulated and calculated HP_2 and HP_3 as a function of resistive load impedance Z_L . As predicted, both HP_2 and HP_3 degrade as the load impedance increases.

Similarly, for the XM distortion, $(\omega_{LO} - (\omega_1 + \omega_2 - \omega_3))$ and $(\omega_{LO} - \omega_1)$ correspond to the RF and the close-in blocker frequencylocations,wheretheloadimpedanceissmall.However, the effect of out-of-band jammer at $(\omega_{LO} - \omega_2)$ is much more Authorized licensed use limited to: Univ of Calif San Diego. Downloaded on October 20,2024 at 11:27:28 UTC from IEEE Xplore. Restrictions apply.

drastic in comparison to that for HP_3 . Hence, apart from providing low load impedance at baseband and high frequency, it is of paramount importance to filter off the out-of-band blockers.

For instance, consider the case of a CDMA-2000 receiver in the personal communication system (PCS) band. The baseband bandwidth is 625 kHz, whereas the strongest jammer, due to TX leakage, is downconverted to 80 MHz. At 80 MHz, the TIA input impedance is large, resulting in poor mixer linearity performance. As suggested by (30a)–(30c), this term contributes to HP_2 , HP_3 , and $\text{HP}_{3,XM}$, making the high load impedance at the downconverted jammer frequency the single most dominant factor in degrading the passive mixer linearity. Hence, instead of placing an interstage RF filter, a linear filtering technique at the mixer output can be helpful in improving the mixer linearity.

Several implementations are feasible for such a linear filter. Typically, there is a tradeoff associated, which is dependent upon the technique under consideration. For instance, the modified downconverting mixer with filtering proposed in [27] requires additional power for the LO and area for the capacitance. The passive filter at mixer output in [28] occupies a die area and active filtering technique proposed in [29] consumes power and degrades noise performance. However, despite the tradeoffs, these techniques reduce the overall cost in comparison to using an off-chip surface acoustic wave (SAW) filter.

Intuitively, a large $|Z_L(\omega_{LO} - \omega_1)|$ results in a large voltage swing at the mixer IF node. This voltage swing boosts the second- and third-order nonlinear current sources resulting in larger distortions. In addition, this can amplify the nonlinear charging and discharging effects of the transistor capacitances.

Agilent Goldengate simulations were performed with low load resistances at $\omega_{\text{LO}} - (\omega_1 - \omega_2)$ and $\omega_{\text{LO}} - (2\omega_1 - \omega_2)$, while resistance at $\omega_{LO} - \omega_1$ is varied. As predicted, a rapid degradation in mixer linearity is observed with increasing mixer load impedance at downconverted jammer frequency $(\omega_{\text{LO}} - \omega_1)$, as shown in Fig. 12.

V. HIGH-FREQUENCY EFFECTS ON MIXER LINEARITY

As the LO frequency increases, the reactive impedances of the nonlinear gate–source and gate–drain capacitances become comparable to the transistor conductance (q_1) , and the mixer linearity performance degrades due to the nonlinear charging and discharging of these capacitors. However, as the technology is scaling to shorter gate lengths, these parasitic capacitances are reduced, and their effects are typically negligible up to a few gigahertz. Typically, the effect of gate–source and gate–drain capacitance nonlinearity on the overall circuit nonlinearity is small, as long as the operating frequency is a small fraction of the transistor unity current gain frequency (f_T) [30].

Another source of nonlinearity is introduced due to the LO rise and fall times [9]. It is straightforward to reduce the rise and fall times of the square-wave LO signal so that its effect is minimal in this frequency range, albeit at the cost of slightly larger LO driver power consumption. These high-frequency effects

Fig. 12. Simulated (using PSP model) and calculated HP_3 variation with the Z_L at Jammer Frequency (Ω)
Fig. 12. Simulated (using PSP model) and calculated IIP₃ variation with the
mixer load impedance at the downconverted jammer frequency ($\omega_{LO} - \omega_1$). The Fig. 12. Simulated (using PSP model) and calculated IIP₃ variation with the mixer load impedance at the downconverted jammer frequency ($\omega_{\text{LO}} - \omega_1$). The RF tone power at the input of the LNA is -30 dBm with $g_{m,\text{$ Fig. 12. Simulated (using PSP model) and calculated IIP₃ variation with the mixer load impedance at the downconverted jammer frequency ($\omega_{\text{LO}} - \omega_1$). The RF tone power at the input of the LNA is -30 dBm with $g_{m,\$ 500 and 5 Ω , respectively, the transistor g_1 is 76 mS, and the square wave LO frequency is 1 MHz.

Fig. 13. Simulated variation in mixer single-ended HP_2 and HP_3 with fre-Frequency (Hz)
Fig. 13. Simulated variation in mixer single-ended HP_2 and HP_3 quency. The RF tone power at the input of the LNA is -50 dBm with g quency. The RF tone power at the input of the LNA is -50 dBm with $g_{m,LNA}$ = 30 mS in Fig. 1(a). The mixer load and source impedances are 5 and 500Ω , respectively, and the transistor g_1 is 76 mS.

will continue to reduce with the shrinking technology and parasitic capacitances. The simulated single-ended HP_2 and HP_3 are plotted as a function of frequency in Fig. 13, and there is little variation in the HP_2 performance, while HP_3 degrades by only 3 dB at 1 GHz with 50 μ m \times 0.18 μ m transistors.

VI. MEASUREMENT RESULTS

Measurements were conducted with a double-balanced passive MOSFET mixer fabricated in a CMOS silicon-on-insulator (SOI) technology [31]. This technology uses an insulating substrate, which reduces the substrate losses and improves device performance. Since the preceding analysis does not involve any assumptions based on the substrate, the results are valid for SOI and non-SOI technologies.

Fig. 14 shows the measurement setup. The RF balun has a 1 : 4 turn ratio, which provides a desirable high source impedance to the mixer. A shunt resistance R_{shunt} was added to create the Authorized licensed use limited to: Univ of Calif San Diego. Downloaded on October 20,2024 at 11:27:28 UTC from IEEE Xplore. Restrictions apply.

Fig. 14. Passive mixer measurement setup.

Fig. 15. Measured and calculated fundamental and third-order intermodulation distortion output powers for the passive CMOS mixer with load impedance of 5Ω . The LO power was $+15$ dBm.

desired load impedance at the IF port. The calculated and measured fundamental and third-order intermodulation powers at the mixer output are plotted in Fig. 15. The measurements are done with 15-dBm sinusoidal LO at 500 MHz, 800 MHz, and 1 GHz with the two input tones placed at 20- and 39.5-MHz offset.

Fig. 16 shows the measured HP_3 with increasing load impedance, which is in close agreement with the calculated values. IIP_3 is computed by comparing the distortion voltage at the mixer output to a reference voltage measured with $5-\Omega$ load impedance. As predicted, HP_3 degrades with the increasing load impedance.

VII. CONCLUSION

We have analyzed the linearity of a current-commutating passive CMOS zero intermediate frequency (ZIF) downconverting FET mixer and highlighted its dependence on the mixer source and load impedances. Closed-form expressions have been presented for the second-order, third-order, and XM input-intercept points of the mixer using a Volterra-series analysis, and are

Fig. 16. Degradation in the measured and calculated HP_3 with increasing load impedance. The LO power was $+15$ dBm and the input power was -10 dBm, and the measurement was done at 800 MHz.

found to be in close agreement with the simulated response with the PSP MOSFET device model.

An accurate relationship has been established between the input impedance and an arbitrary load impedance for an ideal passive mixer. Through this analysis, it is observed that while a resistive load appears unaltered at the mixer input, a capacitive load undergoes a frequency translation, peaking at odd orders of LO harmonics with the peak amplitude going down as $1/n²$, *n* being the order of the harmonic. In particular, the input impedance appears inductive from dc to ω_{LO} and then becomes capacitive from ω_{LO} to $2\omega_{\text{LO}}$.

Dependence of passive mixer linearity on the load and source impedances has been analyzed and design guidelines have been suggested for improving it. Through Volterra series analysis, it is shown that the load impedance should be minimized at downconverted jammer frequencies for improving mixer linearity, particularly, due to the XM distortion. Additionally, the source impedance should be kept as large as possible at dc and the RF signal frequency.

Measurements were conducted with SOI-based passive CMOS mixers and the results have been found to be in close agreement to the calculations for different load impedances.

APPENDIX I POWER-SERIES PARAMETER EXTRACTION

Equation (1) in Section II can be rewritten as

$$
\begin{bmatrix}\nV_D - V_S \\
V_D^2 \\
V_B^3 \\
V_S^3 \\
V_S^4 \\
V_D V_S \\
V_D V_S \\
V_D V_S^2\n\end{bmatrix}\n\begin{bmatrix}\ng \\
g_{2_D} \\
g_{3_D} \\
g_{2_S} \\
g_{3_S} \\
g_{3_D k_S} \\
g_{3_D k_S} \\
g_{3_D k_S}\n\end{bmatrix} = [I_D]
$$
\n(34)\n(34)

where V_D , V_S , and I_D are the dc drain and source voltages, and dc drain current, respectively. From the dc simulation or measurement, the drain current can be obtained for numerous values of V_D and V_S . From n such evaluations, V and I will be $n \times 8$ and $n \times 1$ matrices, respectively, with each row representing a measurement for particular V_D and V_S . Using singular value decomposition (SVD) [32], unitary matrices X , and Y of sizes $n \times n$ and 8×8 respectively, can be obtained such that

$$
V = X\Sigma Y'
$$
 (36)

where Σ is an $n \times 8$ diagonal matrix. Equation (35) can be solved by finding the pseudoinverse of V , defined as

$$
\mathbf{V}^+ = \mathbf{Y} \mathbf{\Sigma}^+ X' \tag{37}
$$

where Σ^+ is the transpose of Σ with every element being replaced by its reciprocal. Thus,

$$
\mathbf{G} = \mathbf{V}^+ I. \tag{38}
$$

This technique computes the least mean-square values of the coefficients in (1).

APPENDIX II DISTORTION COEFFICIENTS

The coefficients for the second-order Volterra kernel of the drain voltage in (12a) are given by

$$
A_2 = \frac{g_{2_S}}{g_1^3} \tag{39a}
$$

$$
A_1 = \frac{(g_{2D\&S} + 2g_{2D})}{g_1^2}
$$
 (39b)

$$
A_0 = \frac{(g_{2_D} + g_{2D\&S} + g_{2S})}{g_1}
$$
 (39c)

and the coefficients for the third-order Volterra kernel of the drain voltage in (12b) are given by

$$
B_3 = 2g_{2_S}^2 + g_1 g_{3_S}
$$
 (40a)

$$
B_2 = g_1(3g_{2_{D\&S}}g_{2_S} + 6g_{2_S}^2 + g_1g_{3_{D\&2S}} + 3g_1g_{3_S})
$$
 (40b)

$$
B_1 = g_1^2(g_{2_{D\&S}}^2 + 2g_{2_D}g_{2_S} + 6g_{2_{D\&S}}g_{2_S} + 6g_{2_S}^2)
$$

$$
+2g_1g_{3_{D&2S}} + g_1g_{3_{D&S}} + 3g_1g_{3_S}
$$
 (40c)

$$
B_0 = g_1^3 (g_{2_D} g_{2_{Dks}} + g_{2_{Dks}}^2 + 2g_{2_D} g_{2_S} + 3g_{2_{Dks}} g_{2_S} + 2g_{2_S}^2 + g_1 (g_{3_D} + g_{3_{Dks2S}} + g_{3_{2Dks}} + g_{3_S})).
$$
\n(40d)

The coefficients for the Volterra kernel for the XM distortion in (19) are given by

$$
C_3 = 3(2g_{2s}^2 + g_1 g_{3s})
$$
\n(41a)

$$
C_2 = g_1(3g_{2_{Dks}}g_{2s} + 6g_{2s}^2 + g_1g_{3_{Dks2s}} + 3g_1g_{3s})
$$
 (41b)

$$
C_1 = g_1(g_{2pks} + 2g_{2p}g_{2s} + 6g_{2pks}g_{2s} + 6g_{2s} + 2g_{2p}g_{2s} + 2g_{2p}g_{2s} + 2g_{1}g_{3pks} + 3g_{1}g_{3s})
$$
(41c)

$$
C_0 = 3g_1^3(g_{2p}g_{2pks} + g_{2pks}^2 + 2g_{2p}g_{2s} + 3g_{2pks}g_{2s} + 2g_{2s}^2 + g_{1}g_{3p} + g_{1}g_{3pks} + g_{1}g_{3pks} + g_{1}g_{3s}).
$$
(41d)

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REFERENCES

- [1] B. Razavi*, Design of Analog CMOS Integrated Circuits*. Boston, MA: McGraw-Hill, 2001.
- [2] T. Lee*, The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge, U.K.: Cambridge Univ. Press, 2004.
- [3] S. Zhou and M.-C. Chang, "A CMOS passive mixer with low flicker noise for low-power direct-conversion receiver," *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1084–1093, May 2005.
- [4] D. Manstretta and F. Svelto, "Analysis and optimization of IIP2 in CMOS direct down-converters," in *Proc. IEEE Custom Integrated Circuits Conf.*, 2002, pp. 243–246.
- [5] M. Lehne, J. Stonick, and U. Moon, "An adaptive offset cancellation mixer for direct conversion receivers in 2.4 GHz CMOS," in *Proc. IEEE Int. Circuits Syst. Symp.*, 2000, vol. 1, pp. 319–322.
- [6] W. Redman-White and D. M. W. Leenaerts, " $1/f$ noise in passive CMOS mixers for low and zero IF integrated receivers," in *Proc. IEEE Eur. Solid-State Circuits Conf.*, Sep. 18–20, 2001, pp. 41–44.
- [7] B. W. Cook, A. Berny, A. Molnar, S. Lanzisera, and K. S. J. Pister, "Low-power 2.4-GHz transceiver with passive RX front-end and 400-mV supply," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2757–2766, Dec. 2006.
- [8] M. Terrovitis and R. Meyer, "Intermodulation distortion in currentcommutating CMOS mixers," *IEEE J. Solid-State Circuits*, vol. 35, no. 10, pp. 1461–1473, Oct. 2000.
- [9] W. Yu, S. Sen, and B. H. Leung, "Distortion analysis of MOS trackand-hold sampling mixers using time-varying Volterra series," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 46, no. 2, pp. 101–113, Feb. 1999.
- [10] V. Aparin and L. Larson, "Analysis and reduction of cross-modulation distortion in CDMA receivers," *IEEE Trans. Microw. Theory Tech.*, vol. 51, no. 5, pp. 1591–1602, May 2003.
- [11] M. White, F. Van De Wiele, and J. Lambot, "High-accuracy MOS models for computer-aided design," *IEEE Trans. Electron Devices*, vol. ED-27, no. 5, pp. 899–906, May 1980.
- [12] K. Joardar, K. K. Gullapalli, C. C. McAndrew, M. E. Burnham, and A. Wild, "An improved MOSFET model for circuit simulation," *IEEE Trans. Electron Devices*, vol. 45, no. 1, pp. 134–148, Jan. 1998.
- [13] BSIM3v3 BSIM Team, Univ. California at Berkeley, Berkeley, CA, Jul. 2005. [Online]. Available: http://www-device.eecs.berkeley.edu/ bsim3/get.html

- [14] M. Bucher, C. Lallement, and C. C. Enz, "An efficient parameter extraction methodology for the EKV MOST model," in *Proc. IEEE Int. Microelectron. Test Structures Conf.*, Mar. 25–28, 1996, pp. 145–150.
- [15] N. D. Arora, R. Rios, C.-L. Huang, and K. Raol, "PCIM: A physically based continuous short-channel IGFET model for circuit simulation," *IEEE Trans. Electron Devices*, vol. 41, no. 6, pp. 988–997, Jun. 1994.
- [16] G. Gildenblat, X. Li, W. Wu, H. Wang, A. Jha, R. V. Langevelde, G. D. J. Smit, A. J. Scholten, and D. B. M. Klaassen, "PSP: An advanced surface-potential-based MOSFET model for circuit simulation," *IEEE Trans. Electron Devices*, vol. 53, no. 9, pp. 1979–1993, Sep. 2006.
- [17] X. J. Xi, J. He, M. Dunga, H. Wan, M. Chan, C.-H. Lin, B. Heydari, A. M. Niknejad, and C. Hu, "BSIM5 MOSFET model," in *Proc. IEEE Int. Solid State and IC Tech. Conf.*, Oct. 18–21, 2004, vol. 2, pp. 920–923.
- [18] J. He, J. Xi, M. Chan, H. Wan, M. Dunga, B. Heydari, A. M. Niknejad, and C. Hu, "Charge-based core and the model architecture of BSIM5," in *Proc. IEEE Int. Quality Electron. Design Symp.*, Mar. 21–23, 2005, pp. 96–101.
- [19] N. Arora*, MOSFET Models for VLSI Circuit Simulation: Theory and Practice*. New York: Springer-Verlag, 1993.
- [20] P. Bendix, P. Rakers, P. Wagh, L. Lemaitre, W. Grabinski, C. C. McAndrew, X. Gu, and G. Gildenblat, "RF distortion analysis with compact MOSFET models," in *Proc. IEEE Custom Integr. Circuits Conf.*, Oct. 3–6, 2004, pp. 9–12.
- [21] H. Khatri, P. S. Gudem, and L. E. Larson, "Simulation of intermodulation distortion in passive CMOS FET mixers," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 7–12, 2009, pp. 1593–1596.
- [22] S. A. Maas, "Two-tone intermodulation in diode mixers," *IEEE Trans. Microw. Theory Tech.*, vol. MTT-35, no. 3, pp. 307–314, Mar. 1987.
- [23] P. Wambacq and W. Sansen*, Distortion Analysis of Analog Integrated Circuits*. Norwell, MA: Kluwer, 1998.
- [24] S. A. Maas, "Theory and analysis of GaAs MESFET mixers," *IEEE Trans. Microw. Theory Tech.*, vol. MTT-32, no. 10, pp. 1402–1406, Oct. 1984.
- [25] Y. Han and L. E. Larson, "A low-power 5 GHz transceiver in 0.13 μ m CMOS for OFDM applications with sub-mm² area," in *Proc. IEEE RF Integr. Circuits Symp.*, Jun. 3–5, 2007, pp. 361–364.
- [26] N. Kim, V. Aparin, and L. E. Larson, "A resistively degenerated wide-band passive mixer with low noise figure and $+60$ dBm IIP2 in 0.18μ m CMOS," in *Proc. IEEE RF Integr. Circuits Symp.*, Jun. 17, 2008, pp. 185–188.
- [27] N. Kim, L. E. Larson, and V. Aparin, "A highly linear SAW-less CMOS receiver using a mixer with embedded Tx filtering for CDMA," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2008, pp. 729–732.
- [28] H. Khatri, L. Liu, T. Chang, P. S. Gudem, and L. E. Larson, "A SAWless CDMA receiver front-end with single-ended LNA and single-balanced mixer with 25% duty-cycle LO in 65 nm CMOS," in *Proc. IEEE RF Integr. Circuits Symp.*, Jun. 7–9, 2009, pp. 13–16.
- [29] H. Khatri, P. S. Gudem, and L. E. Larson, "A SAW-less CMOS CDMA receiver with active Tx filtering," in *IEEE Custom Integr. Circuits Conf.*, Sep. 2009.
- [30] C. Wang, M. Vaidyanathan, and L. E. Larson, "A capacitance-compensation technique for improved linearity in CMOS class-AB power amplifiers," *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 1927–1937, Nov. 2004.
- [31] "P4140 ultra-high linearity broadband quad UltraCMOS(TM) FET array," Peregrine Semiconduct., San Diego, CA, Product Specification, 2009. [Online]. Available: http://www.psemi.com/pdf/datasheets/ pe4140ds.pdf
- [32] G. Golub and C. Van Loan*, Matrix Computation*, 3rd ed. Baltimore, MD: The Johns Hopkins Univ. Press, 1996.

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