A CMOS Multi-Phase Injection-Locked Frequency Divider for V-Band Operation

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***Abstract*—An inductor-less injection-locked frequency divider for high-speed frequency synthesis at V-band is presented. It achieves division by six and operates up to 65 GHz. In addition, it can achieve division ratios of four and two when 44 GHz or 22 GHz input signals are applied, respectively. Implemented in a 0.13 μm digital CMOS technology, the divider draws an average current of 18 mA, and the core area is 0.026 mm^2.**

***Index Terms*—Frequency divider (FD), inductor-less design methodology, injection-locking, locking range, ring-oscillator, self-resonance frequency (SRF).**

I. Introduction

HIGH-SPEED frequency dividers are key building blocks in the implementation of high-frequency phase locked loops (PLLs). There have been many efforts to implement low power, area efficient, frequency dividers for V-band [1], [2]. Implementing dividers with division ratios of larger than two can ease frequency synthesis at high frequencies and reduce power consumption and die area. Static frequency dividers work well up to a fraction of the transition frequency (f_T), and above that limit their power consumption becomes extremely high. Moreover, they require a large signal swing, which is not easy to achieve at frequencies close to f_T. In addition, static frequency dividers usually achieve a division ratio of two, and to achieve larger division ratios, a cascade is required.

Injection-locked frequency dividers can work at higher frequencies compared to static frequency dividers. However, they usually suffer from a narrow input frequency locking range. Several groups have reported regenerative, or injection-locked, dividers working at frequencies up to 70 GHz [1]–[3]. However most designs cannot supply quadrature phases at the output. Furthermore, these architectures are inductor-based, which may require a large die area.

The goal of this research is to implement multi-phase frequency dividers capable of operating at frequencies close to f_T with division ratios of larger than two. For compatibility with digital CMOS technology, the frequency divider must be able to operate at supply voltages as low as 1.2 V, and an inductor-less design methodology is adopted which leads to a smaller die area. But the power consumption of such an approach may be higher in the absence of tunable circuits and inductors.

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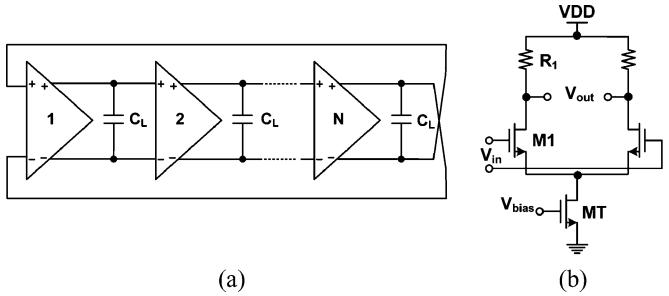

Fig. 1. (a) N-stage ring-oscillator, (b) resistive load differential pair delay cell.

II. Injection-Locked Frequency Divider Design

Consider an N-stage ring-oscillator [Fig. 1(a)]. As shown in [4], the oscillation frequency of the ring-oscillator is given by

$$f_{\rm osc} \approx \frac{1}{2NR_LC_L\ln 2} \tag{1}$$

where R_L and C_L are respectively the equivalent resistance and capacitance at the output of each delay cell.

At the oscillation frequency, each stage must introduce a phase shift of π/N to satisfy the criteria for oscillation. This ring-oscillator can be implemented using the differential pair delay stage with resistive load shown in Fig. 1(b). However, more than two delay stages are required to meet the phase shift requirement. Here, we generate quadrature phases at the output, so a ring oscillator is required with at least four delay stages, when the delay stage in Fig. 1(b) is used. Increasing the number of stages beyond four increases the area and power dissipation, and reduces the achievable self-resonance frequency (SRF).

To analyze injection-locking in ring-oscillators, we use the nonlinear ILFD model introduced in [5], which is shown in Fig. 2. The input signal is injected to the tail current source of the first delay stage of the ring-oscillator, which is modeled as a single-balanced mixer. The function $f(\cdot)$ models the nonlinearity caused by the differential pair in commutating the tail current. The nonlinearity of $f(\cdot)$ introduces harmonics of ω_o prior to mixing. In this case the current at the mixer output [drain current of M1 in Fig. 1(b)] can be written as

$$I_D = g_m A_{\rm inj}\sin(\omega_{\rm inj}t + \phi_{\rm inj})f(V_O) \tag{2}$$

where g_m is the transconductance of the tail current source (MT) in Fig. 1(b). For simplicity, the LO-to-output leakage of the single balanced mixer is not considered in (2). It can be shown that this term does not contribute to the locking range or division ratio of the ILFD.

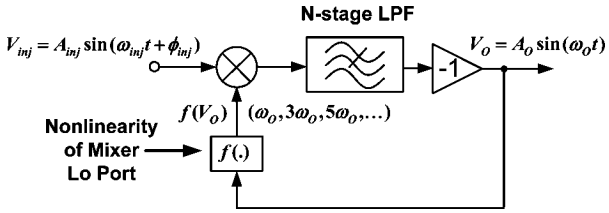

Fig. 2. Nonlinear model for ring-oscillator based ILFD [4].

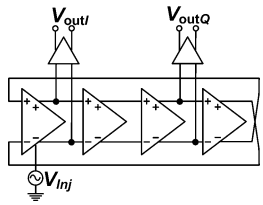

Fig. 3. Four stage ring-oscillator based ILFD.

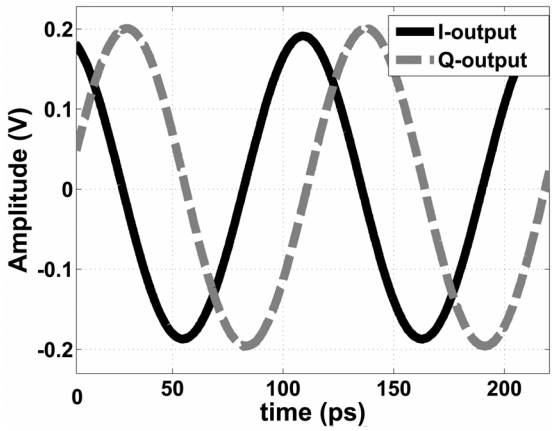

Fig. 4. In-phase and quadrature phases at the output of ILFD operated in the divide-by-6 mode, $f_{\rm in} = 55$ GHz.

Since V_O is a periodic signal, $f(V_O)$ can be expressed using a Fourier series expansion of the harmonics

$$f(V_O) = \sum_{k=-\infty}^{\infty} a_k \, e^{jk\omega_o t} \tag{3}$$

where a_k coefficients are the Fourier coefficients of the output. If V_O is large enough, has a 50% duty cycle and the nonlinearity of the $f(\cdot)$ has odd symmetry, and we can estimate $f(\cdot)$ by a ± 1 square wave. In this case, the differential output current of the mixer can be expressed as

$$I_D = \sum_{k=1}^{\infty} (\pm) \frac{2 g_m A_{\rm inj}}{(2k-1)\pi} \times \cos\left[\omega_{\rm inj} t + \phi_{\rm inj} \mp (2k-1)\omega_o t\right]. \tag{4}$$

The LPF removes the high-frequency mixing components, and only those that satisfy the following condition survive:

$$|\omega_{\rm inj} - (2k-1)\omega_o| = \omega_o. \tag{5}$$

Assuming $\omega_{\rm inj} > (2k-1)\omega_0$ (low side injection in the mixer), it can be concluded that

$$\frac{\omega_o}{\omega_{\rm inj}} = \frac{1}{2k}. \tag{6}$$

The ILFD must be locked to the $2k$th harmonic of its SRF. In this case $\omega_{\rm inj}$ and the $(2k-1)^{th}$ harmonic of the SRF (ω_0) satisfy (5). On the other hand, the $(2k+1)^{th}$ harmonic of the SRF, which corresponds to high-side injection in the mixer, also satisfies (5). Therefore, after low-pass filtering, (4) can be simplified as follows:

$$I_D \cong \frac{4 g_m A_{\rm inj}}{\pi(4k^2-1)} \times (2k \cos\, \phi_{\rm inj} \cos\, \omega_o t - \sin\, \phi_{\rm inj} \sin\, \omega_o t). \tag{7}$$

The upper limit of the mixer output current derived in (7) is therefore

$$|I_{D_{\max}}|_{\omega=\omega_o} < 4 g_m \, A_{\rm inj} \frac{2k}{\pi(4k^2-1)}. \tag{8}$$

As can be seen in (7) and (8), the mixer output current drops inversely with the division ratio. This leads to a reduction of the input sensitivity of the ILFD when injection-locked to higher-order harmonics of ω_o. This leads to the well-known narrower input frequency range for larger division ratios. In this work, we use a tuning mechanism to compensate for this problem.

III. Circuit Implementation

The quadrature output ring-oscillator based ILFD is shown in Fig. 3. It consists of four delay stages. This divider generates eight different phases of the output signal.

Compared to two or three-stage ring-oscillators, a four-stage ring-oscillator relaxes the gain requirement of each stage to meet the loop gain criteria. As a result, a smaller load resistor is used in the delay cell, which will allow the ring-oscillator to achieve a higher self-resonance frequency, but this will increase the required power consumption to achieve the desired voltage swing. As was discussed in Section II, the ILFD needs some tuning mechanism to overcome the narrow locking range problem. An additional tuning element will add some parasitics, and limit the maximum achievable SRF, so the SRF is tuned by changing the bias current of each delay cell. Changing the bias current directly affects the output impedance of each cell, which changes the SRF of the ring-oscillator, as shown in (1).

IV. Measurement Results

This frequency divider is implemented in an IBM 0.13 μm CMOS technology. The differential quadrature phases of the output when the ILFD is operating as a divide-by-6 are shown in Fig. 4. The I/Q phase and amplitude mismatch are roughly 4° and 0.5 dB for a 55 GHz input.

Input sensitivity curves at different division ratios are plotted in Fig. 5. This ILFD achieves a locking range of roughly 5.5 GHz when operated as a divide-by-two, a locking range of 1.4 GHz when operated as a divide-by-four, and 1 GHz for divide-by-six mode.

Tuning curves of this ILFD for operation in the divide-by-six mode are shown in Fig. 6. Although these curves are plotted for 50 mV steps in VDD, this tuning can be done continuously.

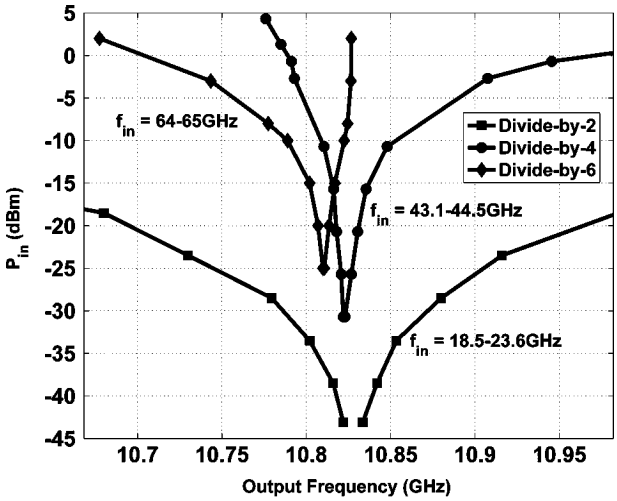

Fig. 5. Input sensitivity curves for different modes of operation.

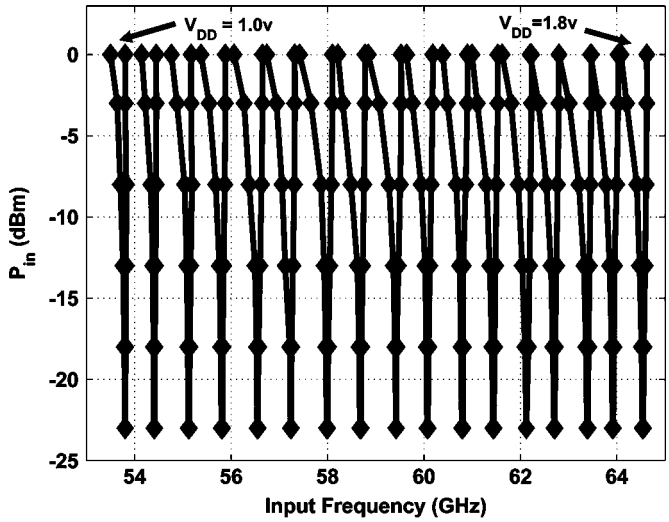

Fig. 6. Input frequency range for divide-by-six mode when external tuning is applied.

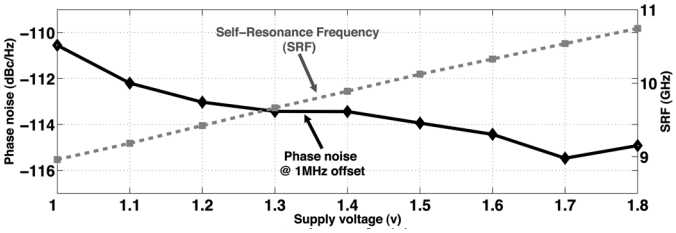

Fig. 7. Phase noise, and SRF for divide-by-six mode vs. external tuning.

These curves show the possibility of extending the effective input range of the ILFD to 51–65 GHz. Moreover, this tuning capability provides margin to compensate for process variations.

Fig. 7 shows the measured SRF and the measured phase noise of the ILFD, when operated as a divide-by-six, for different values of external tuning. As is shown in this figure, the phase noise is better than -110 dBc/Hz at 1 MHz offset for all the values of external tuning.

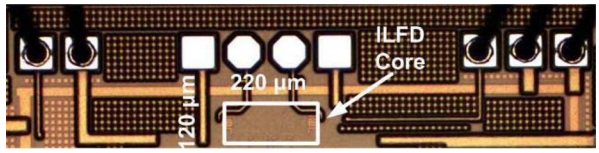

Fig. 8. Chip microphotograph.

TABLE I
PERFORMANCE COMPARISON WITH RECENT V-BAND DIVIDERS

Reference	[1]	[2]	This Work
Input Frequency	70GHz	70GHz	65GHz
Output phases	1	2	4 (Capable of 8)
Division Ratio	4	2	6
Lock Range	1.3%	9.4%	1.5%
Tuning Range	63-72GHz	No tuning	51-65GHz
Input Level	0 dBm	-2 dBm	0 dBm
Phase Noise (@ 1MHz offset)	-	-114 dBc/Hz	-110 - -115 dBc/Hz
Technology	90nm	130nm	130nm
Supply current	5.5mA	5mA	12-24mA
Die Size	0.014 mm^2	0.120 mm^2	0.026 mm^2

The performance of this ILFD is compared with other published CMOS V-band frequency dividers, and is summarized in Table I. Fig. 8 shows the chip microphotograph.

V. CONCLUSION

A CMOS V-Band multi-phase divide-by-six ring-oscillator-based ILFD is presented. The divider also achieves division ratios of four and two when 44 GHz or 22 GHz signals are applied respectively. It does not contain any on-chip inductor nor on-chip transformer, and the core area is 0.026 mm^2. This work demonstrates the possibility of designing compact, low-noise, multi-phase frequency dividers at frequencies close to (f_T) with CMOS technology.

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