A Differential Floating Gate Capacitance Mismatch Measurement Technique

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Abstract:
This paper describes a differential floating gate capacitance matching measurement technique that offers a significant improvement in resolution over those previously reported. It's smaller differential output voltage can be measured to a much higher precision than that of a standard structure. In addition, the differential technique offers superior cancellation of parasitic overlap capacitance effects. Our technique was successfully demonstrated on a 0.50um analog BiCMOS technology.

1. Introduction

The ability of a process to manufacture matched pairs of capacitors is an important requirement for analog applications. Analog-to-digital and digital-to-analog converters are only two of the many types of circuitry that depend on matched or precisely ratioed capacitors. The floating gate test structure is one of the simplest available for measuring capacitance matching, and advances in its evolution have been presented at past sessions of this conference [1,2,3]. When we tried to reproduce the technique here at Cadence, we found we were limited by the resolution of our measurement equipment. Rather than rely on time consuming averaging techniques as proposed in [2], we devised an improved, differential version of the test structure, which involves the measurement of a much smaller differential voltage. This differential signal can be measured to a greater precision than the output voltage of the standard floating gate structure.

2. The Conventional Floating Gate Capacitor Matching Test Structure

A schematic of the conventional floating gate test structure is shown in figure 1. It consists of a symmetric capacitive voltage divider that biases the gate of a pmos source follower. When C1 and C2 are equal, and parasitics can be neglected, half of the input voltage (Vin) appears at the gate (Vg). When C1 and C2 are not equal, a different proportionality constant will be observed. The source follower is in saturation with a fixed current supplied by an external current source flowing through it. The output voltage (Vout) will be clamped to a value of:

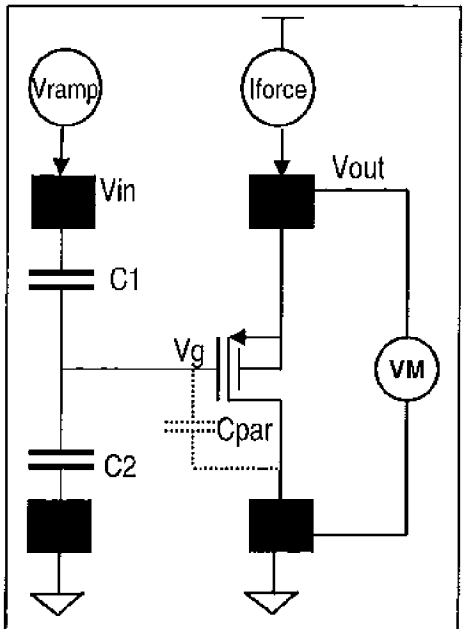

Figure 1: Schematic of Conventional Floating Gate Capacitance Matching Test Structure.

$$Vout = \left(\frac{C1}{C1 + C2 + Cpar}\right) Vin + Vt$$

where Cpar is the parasitic gate to drain overlap capacitance (Cgd), and Vt is the threshold of the Pmosfet. The Vout/Vin transfer curve should be a linear ramp with slope:

$$Slope = \left(\frac{C1}{C1 + C2 + Cpar}\right) \approx \left(\frac{C1}{C1 + C2}\right) \approx \left(\frac{1}{2}\right)$$

The conventional structure is measured by acquiring two Vout vs Vin sweeps [2]. First, C1 is connected to Vin, with C2 being grounded. The resulting Vout vs Vin sweep is linear with slope S1. Then C1 and

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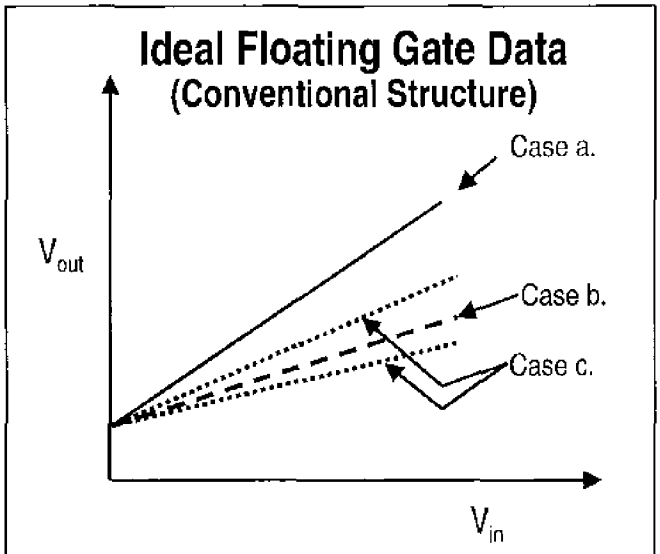


Figure 2 : Ideal Vout/Vin data for three cases:

a. No mismatch, and Cpar can be neglected.
$S_1 = S_2 = 0.5$

b. No mismatch, but Cpar not neglected.
$S_1 = S_2 = 0.5*(1\text{-}Cpar/2C)$

c. Mismatch, and Cpar not neglected.
$S_1 = C1/(C1 + C2 + Cpar)$
$S_2 = C2/(C1 + C2 + Cpar)$

C2 are swapped, with Vin connected to C2, and C1 grounded. The measurement is repeated, yielding a second slope S2. An ideal example of these measurements is shown in figure 2. If there is no mismatch and Cgd is much smaller than C1 and can be neglected, then both S1 and S2 should equal one half. If there is no mismatch, but Cgd cannot be ignored, then S1 will still equal S2, but both be decreased from their ideal values of one half by the factor (Cgd/2C), as shown in figure 2. If there is also mismatch between C1 and C2, then the two slopes will split from their 'matched' values by equal and opposite amounts. If C1 is larger than C2, then S1 will be slightly larger than its ideal value, with S2 being smaller by the same amount. This is important, because the value of Cgd does have a direct effect on the magnitude of Vout, and the slope of (Vout/Vin), which ultimately determines the precision to which mismatch can be measured.

Using simple arithmetic as proposed in [2], the first-order effects of Cpar, the parasitic capacitance resulting from the drain-to-gate overlap capacitance are neutralized:

$$S1 = \frac{C1}{C1 + C2 + Cpar}$$

and

$$S2 = \frac{C2}{C1 + C2 + Cpar}$$

which gives:

$$2\left(\frac{S1 - S2}{S1 + S2}\right) = 2\left(\frac{C1 - C2}{C1 + C2}\right) = \frac{\Delta C}{C}$$

The main drawback we found with the standard floating gate structure is that we were equipment limited. A sample of the measured data for a 30fF capacitor pair is shown in the upper half of figure 3. Vout (shown on the left Y-axis) ranged from 2 to 4 volts, and the resolution of our measurement unit (HP4142 with standard 42424

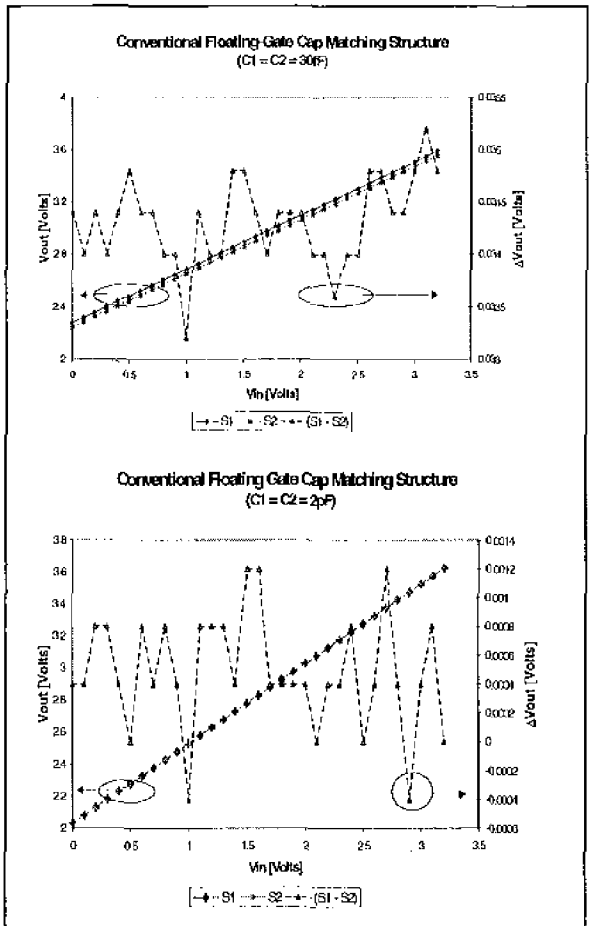


Figure 3: Typical Standard Floating Gate Data
Top: 30fF Pair, (ΔC/C)=612ppm.

Bottom: 2pF Pair, (ΔC/C)=495ppm.

SMUs) at that range was 400uV. The two slopes are different, but since the difference between the two Vouts (shown on the right Y-axis) is quantized by the minimum resolution of the meter, the differences between the two slopes cannot be measured with the desired precision. The situation is

$$S_1 = \left(\frac{C}{2C + \Delta C_L + Cpar_L}\right) - \left(\frac{C+\delta}{2(C+\delta) + \Delta C_R + Cpar_R}\right)$$
$$\approx \frac{(Cpar_R - Cpar_L) + (\Delta C_R - \Delta C_L)}{4C}$$

$$S_2 = \left(\frac{C+\Delta C_L}{2C + \Delta C_L + Cpar_L}\right) - \left(\frac{C+\delta+\Delta C_R}{2(C+\delta) + \Delta C_R + Cpar_R}\right)$$
$$\approx \frac{(Cpar_R - Cpar_L) - (\Delta C_R - \Delta C_L)}{4C}$$

Finally we have...

$$S_1 - S_2 = \frac{(\Delta C_R - \Delta C_L)}{2C}$$

even worse when we look at the data from a large (2pF) pair, shown in the lower half of figure 3, where the mismatch is much smaller. The current way of dealing with this problem is to average a large numbers of readings[2].

To accurately discern 50 parts per million (ppm) we would need to accurately measure differences on the order of 200uV. To have confidence in this result, we feel that the meter's resolution should be at least a factor of ten lower, or 20uV. Most standard instruments can achieve this precision on their smaller scales, so what is really needed, is a structure with a much smaller output voltage. We believe we have the answer with our differential floating structure, which is described next in section 3.

3. The Differential Floating Gate Capacitor Matching Test Structure

A schematic of the differential structure, along with the measurement circuit, is shown in figure 4. It is basically two parallel standard structures, sharing pads for their drains and capacitor connections. Kelvin source pads were added to increase the precision for Vout.

The measurement technique closely resembles that of the conventional structure. An example of ideal measurement data is shown in figure 5.

Vout represents the differential voltage between the outputs of the two sub-structures, and is much smaller, on the order of millivolts. This is much smaller than the output voltage of the conventional structure, which was several volts, as shown earlier in figure 3. The accuracy of a voltage measurement is a function of the full-scale reading of the range that the instrument is operating on. This means that the output voltage of the differential

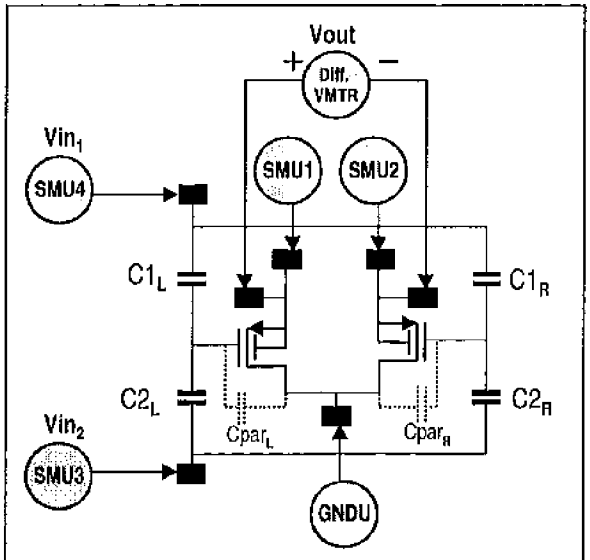


Figure 2: Schematic of Differential Floating Gate Capacitance Matching Test Structure

structure can be measured much more accurately than that of the conventional structure.

Another important improvement is that the parasitics are a function of the difference of the two gate

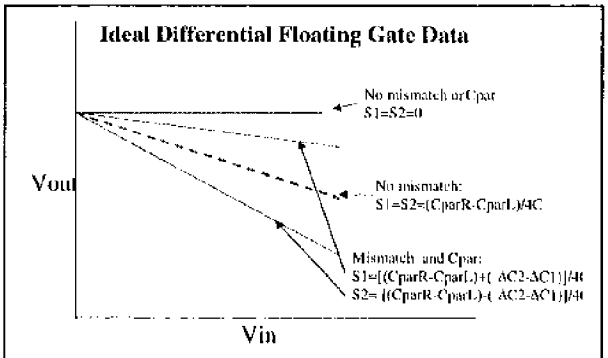


Figure 5: Ideal Measurement Data from a Differential Floating Gate Test Structure

to drain overlap capacitances. This is much smaller than the magnitude of the entire capacitance, which is the parasitic term for the conventional structure. By swapping the upper and lower capacitors, remeasuring, finding a second slope, and then taking the difference between the two slopes, all parasitic terms again drop out, as shown on the next page:

$$S1 = \frac{C_L}{2C_L + \Delta C_L + Cpar_L} - \frac{C_R}{2C_R + \Delta C_R + Cpar_R}$$

$$S2 = \frac{C_L + \Delta C_L}{2C_L + \Delta C_L + Cpar_L} - \frac{C_R + \Delta C_R}{2C_R + \Delta C_R + Cpar_R}$$

Defining C1L=C, C2L=C+ΔCL, C1R= C+δ, and C2R= C+δ+ΔCL, we can rewrite and reduce this as:

$$S_1 = \left(\frac{C}{2C + \Delta C_L + Cpar_L}\right) - \left(\frac{C+\delta}{2(C+\delta) + \Delta C_R + Cpar_R}\right)$$

$$\approx \frac{(Cpar_R - Cpar_L) + (\Delta C_R - \Delta C_L)}{4C}$$

$$S_2 = \left(\frac{C+\Delta C_L}{2C + \Delta C_L + Cpar_L}\right) - \left(\frac{C+\delta+\Delta C_R}{2(C+\delta) + \Delta C_R + Cpar_R}\right)$$

$$\approx \frac{(Cpar_R - Cpar_L) - (\Delta C_R - \Delta C_L)}{4C}$$

Finally we have...

$$S_1 - S_2 \approx \frac{(\Delta C_R - \Delta C_L)}{2C}$$

Mismatch is usually expressed as the sigma of the mismatch of a population, $\sigma(\Delta C/C)$. If one assumes that the distributions of $(\Delta C_L/C)$ and $(\Delta C_R/C)$ are equal, have a mean of zero, and are independent of each other, then we can relate the sigma of $(\Delta C/C)$ to that of $[(\Delta C_R/C) - (\Delta C_L/C)]$, and ultimately (S1-S2) by:

$$\sigma^2\left(\frac{\Delta C_R - \Delta C_L}{C}\right) = \sigma^2\left(\frac{\Delta C_L}{C}\right) + \sigma^2\left(\frac{\Delta C_R}{C}\right) = 2\cdot\sigma^2\left(\frac{\Delta C}{C}\right)$$

$$\sigma\left(\frac{\Delta C}{C}\right) = \sqrt{2}\cdot\sigma(S_1 - S_2)$$

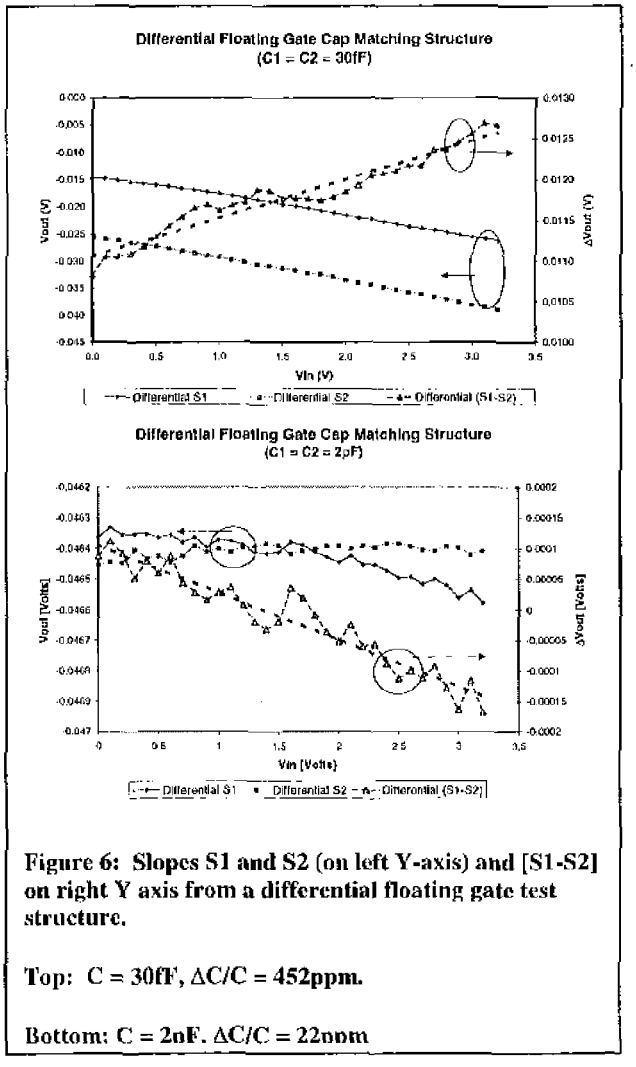


Figure 6: Slopes S1 and S2 (on left Y-axis) and [S1-S2] on right Y axis from a differential floating gate test structure.

Top: C = 30fF, ΔC/C = 452ppm.

Bottom: C = 2nF. ΔC/C = 22ppm

Figure 6 shows a sample of data from a typical structure for two capacitor sizes. Vout1 and Vout2 are the two (differential) outputs, one for each orientation of the capacitive divider, and are plotted on the left side Y-axis. Their difference is plotted on the right side Y-axis. The slope of this curve, multiplied by the square root of two, is the sigma(ΔC/C) of the set of four capacitors within the structure. Clearly, the data from the differential structures (figure 6) is less noisy, and superior to that of the same structures tested as conventional floating gate structures (shown earlier in figure 3).

An important difference between the standard and differential techniques is that for the standard structure, the parasitic term that drops out by subtracting the two slopes is Cpar, (or Cgd), while for the differential technique, the corresponding parasitic term is $(Cpar_R - Cpar_L)$, which can also be written as$(Cgd_R - Cgd_L)$, which is a much smaller quantity. This, along with the smaller magnitude of output voltage, is why measurement data from the differential floating gate structure is superior to that of the standard one.

6: Results:

Our technique was demonstrated on a 0.50um analog BiCMOS process. This process featured an analog double poly precision capacitor option. The interpoly dielectric thickness was 300A, which gives a specific capacitance of approximately 1.1fF/um^2. Structures with five different sizes of capacitors were tested: 2.0pF, 1.0pF, 500fF, 100fF, and 30fF. An example of a layout of one such structure is shown in figure 7. The floating nodes of this structure feature a diode to protect the floating node from excessive charging during fabrication [3].

Since the biggest factor affecting capacitance matching is dimensional variation, designers usually protect matched capacitors from loading-induced etching

non-uniformities by enclosing them in a floating 'dummy' ring. To assess the value of such dummy rings, the 100fF device was also instantiated without them. It was expected that the matching of the 100fF devices with the dummies would be better than that of the 100fF devices without them.

The results are shown on figure 8. The data shows a clear agreement with the inverse square root behavior predicted by Pelgrom's law [4]. They show a $1/(Area)^n$ dependence, with n~0.532. As expected, the 100fF devices with dummies matched better than the 100fF devices without them.

The differential structure could also be measured as a pair of standard structures as described in section 1. A comparison of the results for fitting the data to the model $\sigma(\Delta C/C) = K/(Area)^n$ for the same set of structures using both differential and non-differential methods is shown in table 1.

Table 1 : Comparison of differential vs non-differential measurement methods

Measurement Mode	K	n	R_value
Differential	12851	0.532	0.9971
Non-differential	15779	0.5595	0.9903

The standard (non-differential) analysis technique overestimated the mismatch, as shown by the larger values of K in table 1. The data from the differential analysis also showed a better match with the inverse square root of area dependence as predicted by Pelgrom's law. This is evidenced by the higher goodness of fit R_value and an n value that is closer to one-half for the differential analysis.

7: Conclusion: An improved differential floating gate capacitance matching structure was developed and demonstrated. It relies on measurement of a much smaller (differential) voltage than the standard technique, and can be measured to a much finer precision. In subtracting the two slopes from the two measurement orientations, the term that cancels out is the much smaller difference of parasitic capacitance, rather than the parasitic capacitances themselves. Very good results were obtained without time consuming averaging techniques, which demonstrates that the floating gate technique can be extended into a wider range of capacitor sizes. Due to the superior resolution, it is possible to measure larger capacitors that are typically well matched. And due to the superior first order cancellation of parasitic overlap capacitance effects, it is possible to accurately measure the mismatch of smaller sizes of capacitors than is presently possible with the conventional floating gate structure.

8: References:

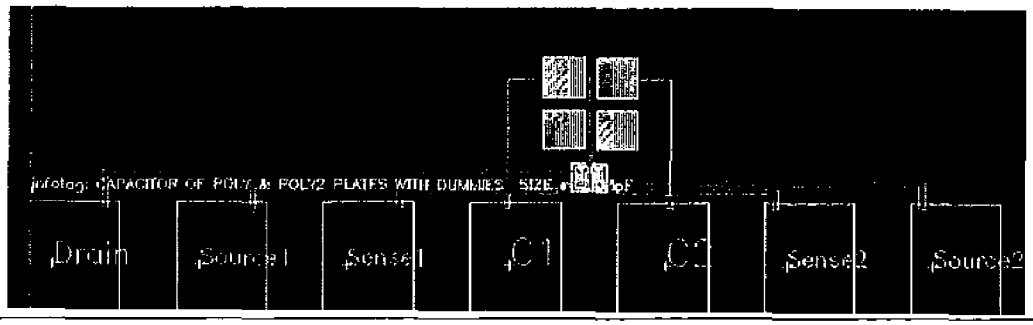
[1] C. Kortekaas, "On-chip Quasi-Static Floating-gate Capacitance Measurement Method", Proceedings of 1990 ICMTS, Vol. 3, March 1990, pp. 109-113.

[2] H.P. Tuinhout, H. Elzinga, J.T. Brugman, F. Postma, "Accurate Capacitor Matching Measurements Using Floating Gate Test Structures", Proceedings of 1995 ICMTS, Vol. 8, March 1995, pp. 133-137.

[3] O. Roux dit Buisson, G. Morin, F. Paillrdet, E. Mazaleyrat, "A New Characterization Method for Accurate Capacitor Matching Measurements Using Pseudo-Floating Gate Test Structures in Submicron CMOS and BICMOS Technologies", Proceedings of 1998 ICMTS, Vol. 11, March 1998, pp. 223-227.

[4] M.J.M. Pelgrom, A.C.J. Duinmaijer, A.P.G. Welbers, "Matching Properties of MOS Transistors", IEEE Journal of Solid State Circuits, Vol. 24, No. 5, pp. 1433-1440, 1989

Figure 4 : Layout of differential cap matching structure



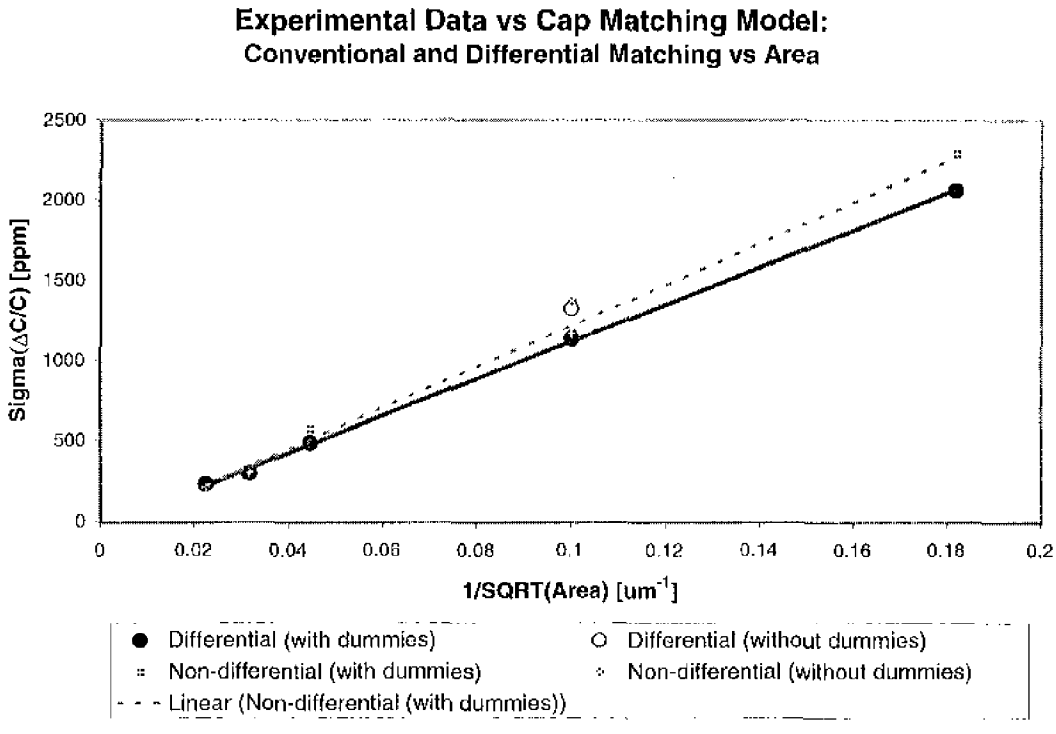


Figure 8: Experimental data: differential vs non-differential