UNIVERSITY OF CALIFORNIA, SAN DIEGO

5 GHz CMOS LNA/Receiver Design for Wireless Local Area Networks

A dissertation submitted in partial satisfaction of the requirements for the degree Doctor of Philosophy in Electrical and Computer Engineering (Electronic Circuits & Systems)

by

John S. Fairbanks

Committee in charge:

Professor Lawrence E. Larson, Chair
Professor Peter M. Asbeck
Professor Paul K. Yu
Professor Robert Bitmead
Professor Michael J. Sailor

2003
The dissertation of John S. Fairbanks is approved, and it is acceptable in quality and form for publication on microfilm:

[Signatures]

Chair

University of California, San Diego

2003
To my family — *sine non qua*

To my brother, Lee, who started me in radio engineering and science.

To the many teachers along my way who took an interest in me and made a difference.

To the memory of my father, Roger, and his family, for my craftsman like abilities.

To my love, Julia, who restored joy and confidence to a kindred soul.

and above all others,

To my mother, Mary, for her inspiration and support.
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<table>
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<tr>
<th>Year</th>
<th>Description</th>
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<tbody>
<tr>
<td>1982</td>
<td>B.A., Physics and Mathematics (Applied), University of California, San Diego</td>
</tr>
<tr>
<td>1982-1984</td>
<td>Product Engineer, Burroughs Corporation, San Diego, California</td>
</tr>
<tr>
<td>1984-1985</td>
<td>Design Engineer, TRW LSI Products Division, La Jolla, California</td>
</tr>
<tr>
<td>1986-1991</td>
<td>Staff Engineer, Hughes Aircraft Corporation, Carlsbad, California</td>
</tr>
<tr>
<td>1990</td>
<td>M.S., Physics, San Diego State University, San Diego, California</td>
</tr>
<tr>
<td>1991-1992</td>
<td>Principal Engineer, Silicon Systems, Incorporated, Tustin, California</td>
</tr>
<tr>
<td>1992-present</td>
<td>President, Fairbanks Laboratories, San Diego, California</td>
</tr>
<tr>
<td>1992-1993</td>
<td>Adjunct Faculty, Southwestern and Palomar Colleges, San Diego County, California</td>
</tr>
<tr>
<td>2001</td>
<td>P.E., Electrical Engineering, E 16362, California State Board</td>
</tr>
<tr>
<td>1997-2003</td>
<td>Research Assistant, University of California, San Diego</td>
</tr>
<tr>
<td>2002</td>
<td>C.Phil., Electrical and Computer Engineering, University of California, San Diego</td>
</tr>
<tr>
<td>2003</td>
<td>Ph.D., Electrical and Computer Engineering (Electronic Circuits &amp; Systems), University of California, San Diego</td>
</tr>
</tbody>
</table>
PUBLICATIONS


FIELDS OF STUDY

Major Field: Electrical and Computer Engineering (Electronic Circuits and Systems)

Professor Lawrence E. Larson
ABSTRACT OF THE DISSERTATION

5 GHz CMOS LNA/Receiver Design for Wireless Local Area Networks

by

John S. Fairbanks

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(Electronic Circuits & Systems)

University of California, San Diego, 2003

Professor Lawrence E. Larson, Chair

Portable, wireless, personal-communication devices continue to gain in popularity, and CMOS technology is becoming increasingly popular for the realization of key radio frequency components [6–8]. Although the intrinsic speed of scaled MOS devices is impressive, the use of CMOS devices for high-frequency applications has been limited by the “digital” orientation of the design and modelling environment. In particular, the optimum scaling, biasing, and tuning of the devices for the realization of the best high-frequency performance in a wireless environmental remains a challenge [9].

The purpose of this work is to develop some straightforward guidelines for simultaneously optimizing the linearity, noise, and dynamic range of the monolithic common-source MOS amplifier in an RF LNA, variable gain amplifier (VGA),
and mixer applications in a wireless transceiver, \textit{under the constraint of minimizing dc power dissipation.} In a sense, this extends the earlier work of Schaefer and Lee [6] on power-constrained MOS LNA design to include linearity considerations. The experimental results presented verify the utility of this technique, and point the way towards fully monolithic CMOS transceivers with improved power/noise/linearity tradeoffs.

Following a brief introduction to RF systems and radio architecture, a detailed analysis of the device modelling, both active and passive, followed by prediction in performance from theory is made. Next, the theory of high-frequency linearity is developed to include nonlinear device behavior, impedance termination matching at the fundamental, second, and third harmonic, and feedback, followed by predictions. Next, noise modelling of MOS devices with feedback is developed and then the noise performance of the common-source amplifier is predicted. Next, an analysis of power-constrained dynamic range limitations on the MOS common-source amplifier and its implications on system performance requirements is discussed, concluding with predictions on tradeoffs.

Next, the theoretical techniques developed above are applied to the design of a 5 GHz low-power, high-linearity low-noise amplifier in a digital 0.35$\mu$m CMOS process. The circuit is simulated, fabricated, and tested.

A discussion detailing the test engineering necessary to verify all of the above results is provided. After which results from each area, device modelling,
linearity, noise theory, RF optimization techniques, and circuit design are reviewed and compared to theoretical predictions.
Chapter I

Introduction and System Architecture

I.1 Introduction to System Architecture

The purpose of this chapter is to discuss the system level requirements for establishing goals in circuit design and device performance. Without reviewing and assessing these requirements, the context for the lower level achievements becomes less relevant. So, the background of system analysis relevant to high frequency circuit design and device performance is reviewed using Orthogonal Frequency Division Multiplexing (OFDM) as an example system architecture. OFDM is a system architecture applicable to Wireless Local Area Networks (WLAN) [10].
I.2 System Architecture Overview

System architecture is the means by which the information, such as a person talking, is conveyed some distance through a medium and reconstructed for a signal receiver, such as a person listening. A Radio provides a means for this communication through the atmosphere and space. Fig. I.1 shows a simple communication system as a guide for further discussion [11].

I.3 Information Modulation in an RF System

Source formatting is the process by which an analog signal is converted to a discrete signal for digital communication systems. This process is in part done through an Analog-to-Digital converter (ADC). The reverse is achieved through a digital-to-analog converter (DAC) when processing a signal through a receiver.

Modulation is a process by which information signals impressed on a car-
rier, which can be transmitted across a medium; that is, where \( A(t) \) and \( \Theta(t) \) contain the information.

\[
S(t) = A(t) \cos(\omega_c t + \theta(t))
\]  

(I.1)

Demodulation that uses the phase of the carrier is called coherent detection, and demodulation which does not use knowledge about the phase of the carrier is non-coherent detection [10].

Three common methods exist for using a fixed communication channel: Frequency Division Multiple Access (FDMA), Time Division Multiple Access (TDMA), and Code Division Multiple Access (CDMA). Briefly, the FDMA modulation scheme uses non-overlapping frequency bands. TDMA uses non-overlapping time slots. CDMA uses orthogonal coding to gain use of the entire time-frequency space. There are distinct advantages and disadvantages to each method, which will not be reviewed here but some references in the bibliography at the end of this dissertation can provide more background information. A consequence however of the choice of a scheme for using a fixed communication channel is that different methods will have different outcomes regarding a receiver’s ability to detect correctly an information signal with a certain quality level. This fact has a bearing on the system, circuit, and device performance requirements.
I.4 RF Channel Impairments

The channel referred to in Fig. I.1 is a medium through which the formatted and modulated signal propagates. The channel is subject to certain losses: Pointing loss, antennae are not aligned; Polarization loss from the EM field misalignment of the antennae; Atmospheric loss from water vapor and oxygen absorption as well as noise sources; Space loss from distance between antennae. These losses affect the overall communication system performance and affect the requirements on the circuit and device performance.

Finally a channel can have multi-path fading from the interaction of EM waves with objects in the path. Multi-path fading is important because it causes the channel to have time-varying propagation delays, attenuation factors, and Doppler shifts. Depending on instantaneous details about the channel it can appear to have flat, Rayleigh, or Rician fading [12].

I.5 RF Receiver

OFDM is a communication scheme designed to counter multi-path fading with wireless digital communication. It is a hybrid of multiple carriers, instead of one described in Section I.3 where each carrier can be amplitude and phase modulated, and Frequency Shift Keying (FSK). FSK is a signalling scheme, which can be detected either coherently or non-coherently, [11], and is described analytically by
\[ S_i(t) = \sqrt{\frac{2E}{T}} \cos(\omega_i t + \phi) \]  

(I.2)

and \( i = 1, 2, 3, \ldots, M \) and \( 0 \leq t \leq T \).

FSK allows a data set to be orthogonally transmitted per symbol. Combining OFDM with FSK allows an additional orthogonality for the information which helps reduce the inter-symbol interference (ISI) caused by multi-path, modelled by Rayleigh fading. Rayleigh fading is defined by

\[ p(z_1|s_2) = \left\{ \frac{z_1}{\sigma_0^2} \exp\left( - \frac{z_1^2}{2\sigma_0^2} \right) \right\} \]  

(I.3)

when \( z_1 \geq 0 \) and 0 otherwise. \( \sigma_0 \) represents the noise at the output of the detection, where \( z_1 \) is the output of the envelope detector in a non coherent FSK receiver.

Since the success in receiving a signal is probabilistic in nature, a probability density function describes the performance. For non-coherent FSK, the definition of the probability of a bit error is given by

\[ P_B = 0.5 \exp\left( -\frac{1}{2} \frac{E_b}{N_o} \right) \]  

(I.4)

where \( E_b \) is the energy per bit and \( N_o \) is the single-side receiver noise power spectral density \( \approx 10^{-11} \text{ W/Hz} \) relative to a 1 \( \Omega \) load. [11].

Since the successful reception of information is probabilistic, a curve exists showing the relationship between the \( E_b/N_o \) and the bit error probability, Fig.I.2.
A relationship exists between the signal to noise ratio, modulation efficiency, and energy/bit, noise power spectral, and the probability of bit error which can be expressed as

$$\frac{E_b}{N_o} = \frac{ST}{N_o} = \frac{S}{RN_o} = \frac{SW}{RN_oW} = \frac{S}{N} \left( \frac{W}{R} \right)$$  \hspace{1cm} (I.5)

where $S$ is the received power, $T$ is the bit duration time, $R = 1/T$, $N = N_oW$, and $W$ is the bandwidth. What this implies is that the quality factor of the digital communication figure of merit is proportional to the signal to noise ratio.

**I.6 System to Receiver Circuit Design Requirements**

The probability of bit error can be determined from the $E_b/N_o$ because of the relationship seen in Fig. I.2. With the $E_b/N_o$ set, which is about 15 dB for
non-coherent FSK detection, [11], performance requirements can be inferred to
set gain, noise figure, linearity in a radio circuit design. Linearity determines
strongly how much in-band distortion from intermodulation distortion and cross-
modulation distortion will contribute to the error in detection. A more complicated
demodulation receiver could use coherent detection on BPSK, QPSK, or QAM
signals, however increased complexity is required and usually more current will
be consumed. The benefit is that the receiver can usually perform better with a
lower signal-to-noise ratio.

Next, a brief description of QAM and MPSK signalling will be discussed
because, these digital modulation methods often appear in 802.11 receivers which
are employed in WLAN.

Quadrature Amplitude Modulation (QAM) is a modulation scheme which
changes the amplitude and phase of a carrier. Frequency modulation of a carrier is
not allowed in OFDM because it would destroy the orthogonality of the subcarri-
ers which offer the improvements in dealing with channel fading, amongst others.
QAM has a signal constellation which is not restricted to a circle. (A signalling
constellation is an N-dimensional plot of the possible vectors corresponding to the
possible digital signals, [13].)

In Fig. 1.3 is shown the constellation for sixteen symbol QAM. This sig-
alling can be generated with two 2-bit DAC’s and has four levels per dimension.
The symbol error rate for QAM can be approximated as shown in (I.6).
Figure I.3: 16 QAM Constellation
\[ P_e \approx 4 \left( 1 - \frac{1}{\sqrt{M}} \right) Q \left( \sqrt{\frac{3E_s}{(M - 1) N_0}} \right) \]  

(I.6)

where \( Q \) is the complementary error function and \( M \) is a scaling of the number of amplitude levels in one dimension and \( E_s = E_b(\log_2 M) \) \[11\]. More detail is available in the reference at the back of this dissertation.

MPSK is M-ary phase-shift keying which, if evaluated using two antipodal signal vectors, will have the same rectangular constellation and thus the same symbol error rate function as QAM-16 shown in I.6. This is called the QAM equivalent of MPSK, \[13\]. More generally MPSK has a symbol error rate of

\[ P_e \simeq 2Q \left( \sqrt{\frac{2E_s}{N_0}} \sin \frac{\pi}{M} \right) \]  

(I.7)

where \( M \) is the related to the number of bits, \( k = \log_2 M \) \[10\]. Finally the power spectral densities for both QAM-16 and rectangular MPSK can be represented by

\[ PSD = K \left( \frac{\sin \pi f l T_b}{\pi f l T_b} \right)^2 \]  

(I.8)

where \( l = 1 \), reciprocal of the bit rate is \( T_b \), \( f \) is the frequency, \( K \) is \( 2P l T_b \), and \( P \) is the transmitted power \[11\].
I.7 System Architecture Summary

The RF system architecture has been reviewed regarding formatting and modulation and the effects of channel losses. The use of OFDM to compensate for multipath losses was introduced. The probability of bit error as a figure of merit for receiver design was developed in connection with signal-to-noise ratio. From this signal-to-noise ratio, a radio design requirement may be set. The design requirements for an ISM radio will be discussed in the next chapter.

I.8 Dissertation Focus

This dissertation will focus on a series of theoretical and experimental areas that are necessary to predict several relevant device and circuit performances in Power Gain, linearity, Noise Figure (NF) for 5 GHz amplifier applications. These areas will lead to higher level suggestions on optimizing circuit performance with respect to system goals and device capabilities. Thus, after a start with the initial background in radio architecture and systems, device modelling of CMOS transistors from a standard digital process is reviewed. From the device modelling, some characteristics are developed for nonlinear analysis and noise modelling. Following this theoretical development is a higher level discussion of a figure-of-merit (FOM), known as Spur-Free Dynamic Range (SFDR) and its relation to system performance and impedance matching effects on Power Gain, Linearity, and Noise. Following the recommendations developed from the SFDR discus-
sions, the theory is applied to LNA circuit design. All of the results from each of these developments are reviewed in comparison to theoretically predicted values. Also some time is spent on the test engineering developed to measure each of these different types of results. The results of a few other technologies are also reviewed.

In summary, the dissertation shows Volterra analysis linearity prediction with four small-signal non-linearities in CMOS FET’s based on careful device modelling and including feedback. Also, a thorough development and prediction of NF for high-frequency device and circuit applications predicting NF as a function of geometry and bias as well as $\Gamma_{\text{opt}}$, including feedback is presented. The effect of impedance matching on the above, plus the use of SFDR in circuit optimization, is shown, followed by an application of the above techniques to Low-Noise Amplifier (LNA) circuit design.

I.9  Dissertation Organization

The dissertation consists of Ten chapters:

Chapter I: Introduction and System Architecture discusses the background of system architecture and the design goals that are derived from radio design, and concludes with this summary of the organization of this dissertation.

Chapter II: Radio Architecture deals with an ISM receiver design to examine the required performance of Power Gain, Noise Figure, and linearity. The
estimates of the Power Gain will be made with simple design models and reported results. Based upon these estimates, an ISM receiver design using a digital CMOS process will be introduced and studied.

Chapter III: Device Modelling deals with the complex mathematical and computer modelling of both devices and transistors in preparation for theoretical RF predictions and design work presented in later chapters. The use of large-signal data for deriving basic CMOS transistor modelling will be made. The use of small-signal data from S-parameters will be defined for later predictions of RF CMOS transistor performance. The use of small-signal data for deriving nonlinear polynomial expansions will be shown and will be employed to predict linearity in Chapter IV: Linearity Analysis of MOSFET’s and noise in Chapter V: Noise Analysis of CMOS FET’s. The construction of transistor models for computer simulation based on physical processes will be described and reviewed. The use of Finite Element Matrix methods to predict inductance will be reviewed, in addition to geometrical process based methods.

Chapter IV IV: Linearity Analysis of MOSFET’s deals with the nonlinear performance of a grounded-source CMOS amplifier operating in the 5 GHz region, and will be analyzed and predicted using a Volterra series. Predictions will be made over a broad range of currents, device geometries, and source and load impedances. Although algebraically complex, this technique will allow the researcher to identify the key limiting features of the nonlinear operation of CMOS
amplifiers operating in strong inversion, and pick the appropriate bias and terminating impedances to achieve the best performance. The match between prediction and measurement will be found to be good in Chapter IX: Experimental Verification of Theory.

Chapter V: Noise Analysis of CMOS FET’s covers a small-signal noise model which will be developed for 5 GHz CMOS grounded-source amplifier including feedback and will be used to predict the minimum Noise Figure and $\Gamma_{\text{opt}}$ along with other noise model parameters. The minimum Noise Figure is predicted to be 1 to 2 dB at 5.0 GHz across device geometry and bias.

Chapter VI: Optimum Design for CMOS RF Amplifiers covers the CMOS transistors, with impedance matching on both the input and output side, forming a grounded-source amplifier at 5.0 GHz. The performance will be predicted as a function of marginal stability under the condition of minimized power consumption constraint for maximum power Gain. Tuning of either the input or the output of the grounded-source amplifier will be done in consideration of maintaining amplifier stability over bias and temperature. Having accessed the region where stable matching can occur, the transistor amplifier’s performance in power Gain, $I_{\text{IP3}}$, or Noise Figure, amongst other RF characteristics as a function of source and load tuning at 5.0 GHz, will be chosen for optimal design implementation of the CMOS transistors.

Chapter VII: LNA Design covers two designs for LNA application, which
will be presented which using two different CMOS processes. Both designs will produce acceptable simulations from two different simulators regarding their design goals. These simulation predictions further will support the expanded use of CMOS in RF applications in the ISM and millimeter wave bands. Acceptable trade-offs will be made with very good performance High Frequencies in Gain, Noise Figure, and $\text{III}P_3$.

Chapter VIII: Laboratory Experiment and Test Engineering covers the DOE’s developed and discussed in prior chapters. The measurement methods to obtain the results will be presented in Chapter IX: Experimental Verification of Theory. The large-signal and small-signal measurement systems, and how they functioned, will be discussed. The many capabilities of these systems to collect and process I-V, S-parameter, RF Load-pull, and Noise Figure data into CMOS model parameters, Gain, and Noise Figure results amongst many others will be discussed. These systems comprise a significant tool into research on RF integrated circuits.

Chapter IX: Experimental Verification of Theory deals with the device modelling results for large-signal, S-parameter, and small-signal testing. The results will be shown to be consistent with physical process data. Three active transistor types: bulk, SOS, and HBT will be reviewed for performance in large-signal, S-parameter, and small-signal measurements. The predictions for passive element performance will be reviewed and good agreement will be found. The linearity of MOSFET’s will be tested against predictions and good agreement will be found.
The predictions of noise theory will be tested also against measurement and good agreement will be found. Next, the optimization of RF CMOS amplifiers will be examined in light of the trade-offs required to implement a good system receiver architecture. Lastly, the performance of an LNA will be checked against goals and simulation results and found to perform well. The overall assessment that will be drawn is that properly developed theory in conjunction simulation and analysis, and expert measurement can be highly successful in achieving system and design goals programmatically with fewer iterations and guesswork.

Chapter X: Conclusion finishes this dissertation.
Chapter II

Radio Architecture

II.1 Introduction

Portable, wireless, personal-communication devices continue to gain in popularity, and CMOS technology is becoming increasingly popular for the realization of key radio frequency components [6–8]. Although the intrinsic speed of scaled MOS devices is impressive, the use of CMOS devices for high-frequency applications has been limited by the “digital” orientation of the design and modelling environment. In particular, the optimum scaling, biasing, and tuning of the devices for the realization of the best high-frequency performance in a wireless environmental remains a challenge [9].

As an example, a typical ISM low-noise receiver shown in Fig. II.1 requires a receiver with a Noise Figure (NF) in the 5.0 GHz band of 6.0 dB, and a third-order input intercept point ($IIP_3$) of 9 dBm [14, 15]. This typically translates to low-noise amplifier (LNA) performance requirements of NF of less than 2.5 dB,
and an input intercept point of greater than 0.0 dBm [16]. At the same time, the mixer is required to have a NF of 10 dB and an input intercept point of greater than 8.0 dBm. Typical published power dissipations for these circuits are in the 30 mW to 45 mW range [17]; they often require more dc power than the entire remaining RF and mixed-signal blocks. Clearly, a technique for optimizing the dynamic range of these elements under the constraint of the lowest possible dc power is desirable.
II.2 Circuit Design Optimization

The purpose of this work is to develop some straightforward guidelines for simultaneously optimizing the NF, $IIIP_3$, and Spur-Free Dynamic Range (SFDR) of the monolithic common-source MOS amplifier in Fig. II.2 for RF LNA, variable gain amplifier (VGA), and mixer applications in a wireless transceiver, under the constraint of minimizing dc power dissipation. In a sense, this extends the earlier work of Schaefer and Lee [6] on power-constrained MOS LNA design to include linearity considerations. The experimental results presented verify the utility of this technique, and point the way towards fully monolithic CMOS transceivers with improved power/noise/linearity tradeoffs. We begin with a review of the theory of high-frequency linearity and noise modelling of MOS devices, and then conclude with an analysis of power-constrained dynamic range limitations on the MOS common-source amplifier.

II.3 Application of RF CMOS to ISM Radio

In previous studies, the RF CMOS common source amplifier has been analyzed, modelled, compared to measurement for $IIIP_3$, NF, Power Gain, matching, stability, and SFDR. Now evaluating the applicability of CMOS transistors to mobile radio design will complete the study [18]. Referring to Fig. II.3 as an example of ISM radio architecture, Table II.1 contains a partial list of the ISM radio receiver requirements, upon which assessing the design requirements needed
for each radio element in the receive chain can be made [19]. Knowing the radio element requirements in the receiver can then allow an approximate analysis of the suitability of these CMOS transistors to be evaluated [20].

Since full analysis and simulation of these circuits is an extensive effort, estimates of the Power Gain and Noise Figure based on theory will be employed

Table II.1: ISM Radio Receiver Requirements

<table>
<thead>
<tr>
<th>Component</th>
<th>Gain(Loss) dB</th>
<th>NF dB</th>
<th>$I_{11}P_3$ dBm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Circulator</td>
<td>(1.0)</td>
<td>1.0</td>
<td>$\infty$</td>
</tr>
<tr>
<td>Top Filter</td>
<td>(1.5)</td>
<td>1.5</td>
<td>$\infty$</td>
</tr>
<tr>
<td>LNA</td>
<td>10.0</td>
<td>3.0</td>
<td>-2.0</td>
</tr>
<tr>
<td>RF Filter</td>
<td>(1.0)</td>
<td>1.0</td>
<td>$\infty$</td>
</tr>
<tr>
<td>RF mixer</td>
<td>10.0</td>
<td>10.0</td>
<td>0.0</td>
</tr>
<tr>
<td>IF Filter</td>
<td>(2.0)</td>
<td>2.0</td>
<td>$\infty$</td>
</tr>
<tr>
<td>Amp</td>
<td>5.0</td>
<td>4.0</td>
<td>5.0</td>
</tr>
<tr>
<td>IF mixer</td>
<td>13.0</td>
<td>10.0</td>
<td>2.0</td>
</tr>
<tr>
<td>Amp</td>
<td>5.0</td>
<td>4.0</td>
<td>5.0</td>
</tr>
</tbody>
</table>
Figure II.3: RF Radio System
to check the applicability of these CMOS transistors to a ISM Receiver.

From the standpoint of practical design with a 0.35μm gate length common source amplifier, realizing the highest power Gain, minimum Noise Figure, and acceptable $III_P$ simultaneously in a circuit design, such as a LNA, is not going to occur without some trade offs. Most notably, some of the gain will be traded-off to improve the minimum Noise Figure of the circuit. VSWR and $III_P$ may also require some loss of gain to meet the LNA objectives for ISM.

The amplifiers in the ISM receiver chain must have at least enough power Gain to boost the signal attenuation through the filters. Based on what has been discussed for estimates so far, these CMOS transistors could be used in an amplifier in an ISM transceiver design successfully.

II.4 Summary

In summary, an ISM receiver design has been examined for required performance of power Gain, Noise Figure, and linearity. The estimates of the power Gain have been made upon simple design models and reported results. Based upon the above estimates, a ISM receiver design using the CMOS transistors introduced and studied here is practical, this however does not estimate the considerable effort necessary to achieve a working example.
Chapter III

Device Modelling

III.1 Introduction

The specific performance of an analog circuit is best analyzed for RF circuit performance such as gain, linearity, power, matching, VSWR, amongst others by working with the small-signal model of the active or passive, device or devices in the circuit. For model elements, their dimensions should be small compared to the wavelength of the operating frequency. If the wavelength is comparable to the element size, a distributed model must be used [21]. Here, the most important element of an analog circuit, the amplifier, is analyzed for the large-signal, S-parameter, and small-signal model parameters. Model performance derived from these parameters are used in turn to predict the above-mentioned circuit and later system performance characteristics in Chapters IV: Linearity, V: Noise, VI: Optimum Design for CMOS RF Amplifiers, and VII: LNA Design. Following this discussion of the amplifier, a discussion of the passive element modelling will oc-
cur. Finally, in Chapter IX: Experimental Verification of Theory, the test results will be compared to the theory developed in this Chapter III.

III.1.1 Device Theory–A Brief Background

The purpose of this section is to provide a brief background of device physics theory for the active devices. The two areas of active devices are MOSFET’s and Heterojunction Bipolar Transistors (HBT’s) and will be reviewed in brief.

Metal Oxide Semiconductor Field Effect Transistors (MOSFET’s)

The MOSFET which can be further divided into bulk and SOI transistor types has properties which are similar but different because of substrate effects. Fig. III.1 shows a simplified cross-section of the enhancement mode NMOS transistor. A similar picture could be drawn for the PMOS transistor. The two together make up the CMOS bulk process from which all digital and analog CMOS circuit design is constructed upon with some variations which will not be pursued here. The basic NMOS transistor in bulk induces a trapezoidal channel under an insulating gate driven by a $v_{GS}$ with increased $v_{DS}$; that is, $v_{DS} = v_{GS} - V_t$, where $V_t$ is the threshold voltage, and the transition is where the channel begins to pinch-off at the drain and is called $v_{DS} = v_{DSat}$. Further increases in $v_{DS}$ do not significantly change the output current and the linear relationship with increased current from increased gate voltage ceases to continue or saturates at the drain end as seen in Fig. III.1 continues to be pinched-off.
Next, some of the current-voltage equations describing the NMOS behavior will be reviewed. In current-voltage relationship seen in III.1, the linear or triode region behavior is shown, which occurs when $v_{GS} \geq V_t, v_{DS} \leq v_{GS} - V_t$

$$i_D = k'_n \left( \frac{W}{L} \right) \left[ (v_{GS} - V_t) v_{DS} - \frac{1}{2} v_{DS}^2 \right]$$  \hspace{1cm} (III.1)

The saturated current-voltage equations shown in III.2 describe the NMOS behavior in saturation where $v_{GS} \geq V_t, v_{DS} \geq v_{GS} - V_t$ [1].

$$i_D = \frac{1}{2} k'_n \left( \frac{W}{L} \right) (v_{GS} - V_t)^2 (1 + \lambda v_{DS})$$  \hspace{1cm} (III.2)

The square law name regarding CMOS I-V can be seen in the current-voltage relationship where $i \propto v^2$. The channel length modulation term is $\lambda$ and is equal to $1/V_A$. These equations are only valid in the long-channel operating region, where $L_g > 0.5 \mu m$. At shorter gate lengths, the equations are considerably

The NMOS small-signal behavior is described by several parameters of which a few are mentioned here. The transconductance is defined by III.3.

\[ g_m = \frac{\partial i_{DS}}{\partial v_{GS}} \bigg|_{v_{GS}=V_{GS}} \]  

(III.3)

The transconductance shows the small signal slope from gate voltage to drain current and composes a simple gain equation in the case of a common-source amplifier, where the gain \(-g_m r_o\) and \(r_o\) is the small-signal resistance at the drain.

The output conductance shows the small signal slope from drain to source and its reciprocal factors into the load total for determining gain and impedance matching on other RF parameters.

\[ g_o = \frac{\partial i_{DS}}{\partial v_{DS}} \bigg|_{v_{GS},v_{BS}} \]  

(III.4)

The next small-signal definition amongst others available is the \(f_T\), the frequency of unity current gain, as seen in III.5

\[ f_T \approx \frac{g_m}{2\pi (c_{gs} + c_{gd} + c_{gb})} \]  

(III.5)

where \(c_{gs}\) is the gate-source capacitance, \(c_{gd}\) is the gate-drain capacitance, and \(c_{gb}\) is the gate-bulk capacitance.

The \(f_T\) defines the frequency where \(A_i\) goes to one \((A_i = i_O/i_I)\). \(f_T\) is
a measure of the current gain of a device. This formula should include extrinsic circuit elements such as $R_g$ but does not, since they often have a small effect.

$f_{\text{max}}$ is a measure of the frequency where the power gain of a amplifying device is unity:

$$f_{\text{max}} \approx \frac{f_T}{\sqrt{4R_g (g_{sd} + \omega_T c_{gd})}} \quad \text{(III.6)}$$

where $R_g$ is the distributed gate resistance, $g_{sd}$ is the source-drain conductance, $\omega_T$ is the frequency of oscillation in radians per second at the $f_T$ transistion, $c_{gd}$ is the gate-drain capacitance [2].

The difference between $f_T$ and $f_{\text{max}}$ can be considerable. Several factors, depending on the values of $R_g$, $g_{sd}$, and $c_{gd}$. Of the two figures of merit, $f_{\text{max}}$ is the better estimator of the two for RF performance. Proper modelling is critical for an accurate estimate of $f_{\text{max}}$ [2].

**Silicon on Insulator Field Effect Transistors (SOI FET’s)**

The Silicon-on-Insulator (SOI) FET for which an example is shown in Fig. III.2 shows the general cross-section of a MOSFET on an insulator which could be formed of oxide or sapphire or other insulating material.

One of the key differences from bulk MOSFET’s and the associated equations describing I-V behavior is that the SOI transistor is completely separate from near neighbors due to the insulation from the oxide. Another feature is that the body contact of the MOSFET in SOI is floating. Thus because of charge isola-
tion, kinks may develop in the I-V plots unlike the smooth transitions seen in bulk CMOS FET’s. The advantages of the SOI FET are the lower parasitic capacitance [3]. As was seen in III.5, the reduction in capacitance increases the $f_T$.

**Heterojunction Bipolar Transistors (HBT’s)**

The cross-section for the HBT is shown in Fig. III.3. The presence of Germanium in the base gives the silicon HBT its unique characteristics.

In a Heterojunction device, Germanium added to the base decreases the bandgap at the emitter-base junction and creates a built-in electric field with the base [23]. This situation results in improved transport properties through the base and higher $f_T$ and $f_{max}$.

This concludes the brief review of device physics of MOSFET’s in bulk and on-insulator and HBT’s. Much more is available in the literature listed in the bibliography at the end of the dissertation.
III.2 Large-Signal Excitation Modelling

Large-signal transistor modelling has been used to derive complete circuit simulator models used in software programs based on SPICE. The process for creating circuit simulator model is based on acquiring several different curves describing the behavior of a transistor in its linear, saturation, and subthreshold and subthreshold saturation regions of operation. The large-signal I-V curves shown in the following Figs. III.4, III.5, III.6, and III.7 are of 0.35 μm CMOS transistors, fabricated by Agilent Technologies, in their saturation region of operation under high-field, $V_{ds} = 1.5V$. High-field was chosen because it represents the operating bias of interest in the nonlinear modeling of Section III.3.3. In the case of modeling for computer simulation, low-field, $V_{ds} = 0.1$ V or less, is the more...
common choice for extracting the linear-curve based parameters, for instance, the transistor threshold voltage. Amongst the common parameters extracted from the linear region of the transistor operation are threshold voltage, $V_t$, transconductance, $g_m$, the mobility field effect, and others. Here we shall focus on only the two parameters from the linear large-signal excitation, $V_t$, and, $g_m$.

As can be seen in Table III.1: CMOS N-channel devices of $L=0.35\mu m$ Large-signal parameters at $V_{DS}=1.5V$, the devices show similar $V_t$ extrapolated at tangency to the I-V linear curve at maximum transconductance. The transconductance is defined to be the

$$g_m = \left. \frac{\partial i_D}{\partial v_{GS}} \right|_{v_{GS}=V_{GS}}$$  \hspace{1cm} (III.7)
Figure III.5: N130μm x 0.35μm Large-Signal Current vs. Voltage, Linear Region, $V_{DS} = 1.5V$.

Table III.1: Large-Signal CMOS Parameters for L=0.35μm at $V_{DS} = 1.5V$

<table>
<thead>
<tr>
<th>Width, μm</th>
<th>$V_t$, V</th>
<th>peak $g_m$, mS</th>
<th>$g_o$, mS</th>
</tr>
</thead>
<tbody>
<tr>
<td>N50</td>
<td>0.698</td>
<td>11.3</td>
<td>1.10</td>
</tr>
<tr>
<td>N130</td>
<td>0.705</td>
<td>29.2</td>
<td>4.24</td>
</tr>
<tr>
<td>N200</td>
<td>0.694</td>
<td>44.7</td>
<td>4.00</td>
</tr>
<tr>
<td>N520</td>
<td>0.639</td>
<td>84.5</td>
<td>29.4</td>
</tr>
</tbody>
</table>

and scales linearly with increase in gate width. Only the N520 fails to completely meet the scaling expectation by about 28 percent but should have had a transconductance value closer to 116 μS.

Table III.1 shows the scaling of the instantaneous output conductance as a function of the gate bias of $V_{GS} = 1.5V$. The $g_o$ values extracted from the saturation curves and modelled via MatLab show again a scaling with increase in
Figure III.6: N200μm x 0.35μm Large-Signal Current vs. Voltage, $V_{DS} = 1.5V$

Figure III.7: N520μm x 0.35μm Large-Signal Current vs. Voltage, $V_{DS} = 1.5V$. 
gate width, excepting a fall-off in the larger N520μm transistor.

Figs. III.8, III.9, III.10, and III.11 show the N50μm x 0.35μm, N130μm x 0.35μm, N200μm x 0.35μm, and N520μm x 0.35μm transistors saturation performance under high-field, \( V_{ds} = 1.5 V \). The \( r_o \), as defined in III.4, under these conditions is extracted for use in predicting the small-signal performance of intermodulation distortion and other RF characteristics. The values for \( g_o \) as shown in Table III.1, are extracted from I-V measurement by taking the derivative of the curve describing the I-V measurement at a specified \( V_{GS} \) over a \( 1.4V \leq V_{DS} \leq 1.6V \). With several points so derived and extracted a function of \( g_o \) vs. \( V_{DS} \) can be plotted. Once plotted, a polynomial function of \( g_o \) can be fitted to the curve vs. \( V_{DS} \), and coefficients derived for linearity calculations in Chapter IV: Linearity.
Figure III.9: N130μm x 0.35μm Large-Signal Current vs. Voltage, $1.0V \leq V_{GS} \leq 3.0V$.

Figure III.10: N200μm x 0.35μm Large-Signal Current vs. Voltage, $0.0V \leq V_{GS} \leq 3.0V$. 
Figure III.11: N520µm x 0.35µm Large-Signal Current vs. Voltage, 0.3V ≤ $V_{GS}$ ≤ 1.5V.

Analysis of MOSFET’s.

The conclusion is that we have shown the Large-Signal I-V performance of four CMOS transistors in both linear and saturation regions of operation and extracted several transistor model parameters: $V_t$, $g_m$, and $g_o$.

### III.3 CMOS Small-Signal Model

#### III.3.1 Small-Signal Excitation Modelling

A small-signal nonlinear model of the grounded-source MOS transistor, containing both linear and nonlinear elements is shown in Fig. III.12. The impedance matching networks, represented by $M_s$ and $M_L$, in Fig. III.12 can be modelled in general as two-port networks. The impedance matching networks perform the
function of matching the input or output circuit impedance to the driving or load impedance by effecting a lossless transformation between the two. That is, the input circuit impedance is matched to the source impedance by the input matching network and likewise for the output. Of course, the input matching network may also perform the function of mismatching the input impedance of the circuit to the source impedance. Similarly, the output matching network can mismatch the output circuit impedance to the output load. The purposeful mismatching of the input or output of a circuit will be more fully developed in Chapter VI: Optimum Design for CMOS RF Amplifiers [22]. The reason for mismatching at source or load of a two-port amplifier is that the optimum performance of one RF parameter is often not at the same location on the Smith chart as the others. Thus, a tradeoff must be to favor one parameter, such as Power Gain, over others, such as NF.
The first discussion will be on the S-parameter measures and the second discussion on the nonlinear modelling of the CMOS transistors.

### III.3.2 S-Parameter Measurements of the Small-Signal CMOS model

A CMOS transistor model can be treated in a two-port manner where the components of the small-signal transistor model are evaluated in terms of the scattering or S-parameters in a specific region of operation, Fig. III.13. The operating region of the transistor of interest is the saturation region and the bias on the transistors evaluated is $V_{ds} = 1.5V$ and $v_{GS} = 1.0$ and $1.5V$ + small-signal rf = -10.0 dBm. The response of the S-Parameter contains four results; namely, two results show the amount of reflection from each of the ‘ports’ or input and output of the transistor, the other two show the forward and reverse transmittance at a specific impedance, $Z_o$. 

![Figure III.13: Two Port S-Parameter Measurement Model](image-url)
The S-parameters are defined as follows at a specific length from the source or generator and the load as follows:

\[ S_{11} = \left. \frac{b_1}{a_1} \right|_{a_2=0} \]  \hspace{1cm} (III.8)

\[ S_{22} = \left. \frac{b_2}{a_2} \right|_{a_1=0} \]  \hspace{1cm} (III.9)

The reflection characteristics of the two-port are given in III.8 and III.9 [22].

\[ S_{21} = \left. \frac{b_2}{a_1} \right|_{a_2=0} \]  \hspace{1cm} (III.10)

\[ S_{12} = \left. \frac{b_1}{a_2} \right|_{a_2=0} \]  \hspace{1cm} (III.11)

where the \( a_i \) and \( b_i \) are defined as follows and \( i = 1, 2 \)

\[ a_i = \frac{V_i^+}{\sqrt{Z_{oi}}} = \sqrt{Z_{oi}}I_i^+ \]  \hspace{1cm} (III.12)

and

\[ b_i = \frac{V_i^-}{\sqrt{Z_{oi}}} = \sqrt{Z_{oi}}I_i^- \]  \hspace{1cm} (III.13)

The two preceding equations are also functions of position along the waveguide but this has been suppressed for clarity, [22]. The transmission characteristics of the two-port are given in III.10 and III.11.
The results of characterizing CMOS transistors for S-parameters at the biases described above is given in Chapter IX. S-parameters are widely used to determine matching, gain, linearity, and noise RF parameters and will be discussed in greater detail in Chapter VI: Optimum Design for CMOS RF Amplifiers.

III.3.3 Modeling of the Nonlinear Elements in the Small-Signal Model

The nonlinear lumped elements of the small-signal model for the CMOS transistor can be modelled by terms which describe the performance of each element from large-signal under different biases. Also, estimates can be made of the terms describing the lumped element values by calculations based on physical process data [2, 24].

Under normal operation in the saturation region, the major sources of non-linearity are the transconductance \( g_m \), the gate-source capacitance \( C_{gs} \), the channel conductance \( g_o \) and drain-substrate capacitance \( C_{ds} \) [2]. The gate-drain capacitance \( C_{gd} \) can be considered to be a linear element [2].

We begin with an analysis of the output circuit. The transistor transconductance can be characterized by a nonlinearity of the following general form [2]

\[
    i_{gm} = (a_1 \cdot v_{gs} + a_2 \cdot v_{gs}^2 + a_3 \cdot v_{gs}^3 + \ldots) \cdot (V_{GS} - V_t) \tag{III.14}
\]

where \( i_{gm} \) is the small-signal output current and \( v_{gs} \) is the small-signal input voltage. Remembering the definitions for the gate voltage, \( v_{GS} = V_{GS} + v_{gs} \), for the
total large and small signal, likewise for \( i_{Gm} = I_{Gm} + i_{gm} \). Then the complete current relationship can be stated as follows

\[
i_{Gm} = (a_0 + a_1 \cdot vgs + a_2 \cdot vgs^2 + a_3 \cdot vgs^3 + \ldots) \cdot (V_{GS} - V_t) \quad (\text{III.15})
\]

From III.15, the relationship between large and small signal parameters used in modelling can be clearly seen. The first term in III.15 is the large-signal \( g_m \) and the rest are the small-signal terms from a polynomial expansion around a particular operation point. The drain-source current from this equation is composed of two sources one representing the small-signal contribution about a large-signal operating point. If the small-signal were turn-off, then the drain-source current would be a function of the large-signal \( g_m \) in product with \( V_{eff} \), where \( V_{eff} \) is equal to \( V_{GS} - V_t \). In the expansion of III.15, finding the small-signal curvature of the I-V relationship around a given large-signal bias is the desired goal.

Each of the Figs. III.14, III.15, III.16, and III.17 show the modelled transconductance, \( g_m \) vs. \( V_{GS} \). Coefficients were derived for each of the nonlinear elements described by polynomial expansion and fitting about a large-signal operating point in MatLab based on measured IV curves under specific bias conditions. Thus, the power series expansion given in III.14, for instance, contains both the large-signal value of transconductance, \( a_0 \), and the small-signal value of transconductance, \( a_1 \), along with higher orders, \( a_n \). This provides for prediction of the transconductance in the presence of both large-signal and small-signal excitation. The extracted coefficients are shown in Table III.2.
Figure III.14: N50μm x 0.35μm Measured and Modelled $g_m$ vs. $V_{GS}$

Table III.2: Transconductance Coefficients for Nonlinear Analysis, $g_m$

<table>
<thead>
<tr>
<th>NMOS</th>
<th>$a_0(m)$</th>
<th>$a_1(m)$</th>
<th>$a_2(m)$</th>
<th>$a_3(m)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>N50</td>
<td>9.2</td>
<td>12.4</td>
<td>-5.4</td>
<td>-14.2</td>
</tr>
<tr>
<td>N130</td>
<td>24.9</td>
<td>19.4</td>
<td>-29.2</td>
<td>18.9</td>
</tr>
<tr>
<td>N200</td>
<td>38.5</td>
<td>30.3</td>
<td>4.7</td>
<td>27.8</td>
</tr>
<tr>
<td>N520</td>
<td>102.5</td>
<td>71.0</td>
<td>25.3</td>
<td>-18.5</td>
</tr>
</tbody>
</table>
Figure III.15: N130µm x 0.35µm Measured and Modelled $g_m$ vs. $V_{GS}$
Figure III.16: N200μm x 0.35μm Measured and Modelled $g_m$ vs. $V_{GS}$
Figure III.17: N520\(\mu\text{m} \times 0.35\mu\text{m}\) Measured and Modelled \(g_m\) vs. \(V_{GS}\)
Similarly, the output conductance can be characterized as

\[ i_{ro} = (g_1 \cdot v_{ds} + g_2 \cdot v_{ds}^2 + g_3 \cdot v_{ds}^3 + \ldots) \cdot (V_{DS}) \]  

(III.16)

where the quantities \( g_1, g_2, \) and \( g_3 \) are also functions of \( v_{gs} \) and \( g_1 \) is the linear small-signal drain-source conductance. The complete small- and large-signal version is given in III.16

\[ I_{ro} + i_{ro} = (g_0 + g_1 \cdot v_{ds} + g_2 \cdot v_{ds}^2 + g_3 \cdot v_{ds}^3 + \ldots) \cdot (V_{DS}) \]  

(III.17)

In the expansion of III.17, finding the small-signal curvature of the I-V relationship around a given large-signal bias is the desired goal.

Each of the Figs. III.18, III.19, III.20, and III.21 show the modelled output conductance, \( g_o \) vs. \( V_{DS} \). Coefficients were derived for each of the nonlinear elements described by polynomial expansion and fitting about a large-signal operating point in MatLab based on measured IV curves under specific bias conditions. Thus, the power series expansion given in III.16, for instance, contains both the large-signal value of output conductance, \( g_0 \), and the small-signal value of output conductance, \( g_1 \), along with higher orders, \( g_n \). This provides for prediction of the output conductance in the presence of both large-signal and small-signal excitation. The extracted coefficients are shown in Table III.3.

The output capacitor can be characterized by

\[ i_{cs} = c_1 \frac{dv_{ds}}{dt} + \frac{c_2}{2} \frac{dv_{ds}^2}{dt} + \frac{c_3}{3} \frac{dv_{ds}^3}{dt} + \ldots \]  

(III.18)
Figure III.18: N50\(\mu \text{m} \times 0.35\mu \text{m}\) Measured and Modelled \(g_o\) vs. \(V_{DS}\)

Table III.3: Output Conductance, \(g_o\)

<table>
<thead>
<tr>
<th>NMOS</th>
<th>(g_0)</th>
<th>(g_1)</th>
<th>(g_2)</th>
<th>(g_3)</th>
</tr>
</thead>
<tbody>
<tr>
<td>N50</td>
<td>1.1</td>
<td>-3.52</td>
<td>2.25</td>
<td>-0.7</td>
</tr>
<tr>
<td>N130</td>
<td>4.2</td>
<td>-6.98</td>
<td>3.25</td>
<td>-50.5</td>
</tr>
<tr>
<td>N200</td>
<td>4.0</td>
<td>-4.82</td>
<td>7.25</td>
<td>270.9</td>
</tr>
<tr>
<td>N520</td>
<td>29.4</td>
<td>-16.45</td>
<td>52.4</td>
<td>424.2</td>
</tr>
</tbody>
</table>
Figure III.19: N130\textmu m x 0.35\textmu m Measured and Modelled $g_o$ vs. $V_{DS}$
Figure III.20: N200μm x 0.35μm Measured and Modelled $g_o$ vs. $V_{DS}$
Figure III.21: N520µm x 0.35µm Measured and Modelled $g_o$ vs. $V_{DS}$
Figure III.22: N50μm x 0.35μm Modelled $c_{DS}$ vs. $v_{DS}$
Table III.4: Output Capacitance, $c_{DS}$

<table>
<thead>
<tr>
<th>NMOS</th>
<th>$c_0(f)$</th>
<th>$c_1(f)$</th>
<th>$c_2(f)$</th>
<th>$c_3(f)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>N50</td>
<td>21.7</td>
<td>-15.65</td>
<td>91.10</td>
<td>5.28</td>
</tr>
<tr>
<td>N130</td>
<td>83.1</td>
<td>-40.69</td>
<td>236.9</td>
<td>13.73</td>
</tr>
<tr>
<td>N200</td>
<td>100.0</td>
<td>-62.6</td>
<td>364.4</td>
<td>21.12</td>
</tr>
<tr>
<td>N520</td>
<td>207.0*</td>
<td>-162.8</td>
<td>947.5</td>
<td>424.2</td>
</tr>
</tbody>
</table>

The Fig. III.22 shows the modelled output capacitance, $c_{DS0}$ vs. $v_{DS}$. Coefficients were derived for each of the nonlinear elements described by polynomial expansion and fitting about a large-signal operating point in MatLab based on measured CV curves under specific bias conditions. Thus, the power series expansion given in III.18, for instance, contains both the large-signal value of output capacitance, $c_0$, and the small-signal value of output capacitance, $c_1$, along with higher orders, $c_n$. This provides for prediction of the output capacitance in the presence of both large-signal and small-signal excitation. The extracted coefficients are shown in Table III.4. The relationship between $c_{DS0}$ and III.18 is that of the capacitance value of a MOS capacitor at a given large-signal bias. Of course, no large-signal current flows to contribute to the overall small-signal current in III.18, but the value of the ‘large-signal’ capacitance changes in a MOS capacitor as a function of the large-signal bias. The measure of the capacitance is found by tying an rf oscillator to a slow large-signal or dc ramp. In the expansion of III.18, finding the small-signal curvature of the C-V relationship around a given large-signal bias is the desired goal.
The input capacitor current can be modelled by

\[ i_{cs} = c_{g1} \frac{dv_{gs}}{dt} + \frac{c_{g2}}{2} \frac{dv_{gs}^2}{dt} + \frac{c_{g3}}{3} \frac{dv_{gs}^3}{dt} \]  

(III.19)

The Figs. III.23, III.24, III.25, III.26 shows the modelled input capacitance, \( c_{gs0} \) vs. \( V_{GS} \). Coefficients were derived for each of the nonlinear elements described by polynomial expansion and fitting about a large-signal operating point in MatLab based on measured CV curves under specific bias conditions. Thus, the power series expansion given in III.19, for instance, contains both the large-signal value of input capacitance, \( c_{g0} \), and the small-signal value of input capacitance, \( c_{g1} \).
Figure III.24: N130μm x 0.35μm Modelled $c_{GS}$ vs. $V_{GS}$
Figure III.25: N200 μm x 0.35 μm Modelled $C_{GS}$ vs. $V_{GS}$
Figure III.26: N520\(\mu\)m x 0.35\(\mu\)m Modelled \(c_{GS}\) vs. \(V_{GS}\)
along with higher orders, $c_{gn}$. This provides for prediction of the input capacitance in the presence of both large-signal and small-signal excitation. The extracted coefficients are shown in Table III.5. The relationship between $c_{GS0}$ and III.19 is that of the capacitance value of a MOS capacitor at a given large-signal bias. Of course, no large-signal current flows to contribute to the overall small-signal current in III.19, but the value of the 'large-signal' capacitance changes in a MOS capacitor as a function of the large-signal bias. The measure of the capacitance is found by tying an rf oscillator to a slow large-signal or dc ramp for large area capacitors. For small capacitance found in the gates of MOSFET's, Y-parameters derived from measured S-parameters of the MOSFET’s were used following a deembedding process for pad effects. The properly scaled values of capacitance as a function of area were compared between the measured MOSFET’s and physical process data, using a CV meter. The body and source of the MOSFET’s is strongly connected through substrate contacts, thus the two are combined in this study. In the expansion of III.19, finding the small-signal curvature of the C-V relationship around a given large-signal bias is the desired goal.

<table>
<thead>
<tr>
<th>NMOS</th>
<th>$c_{g0}(f)$</th>
<th>$c_{g1}(f)$</th>
<th>$c_{g2}(f)$</th>
<th>$c_{g3}(f)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>N50</td>
<td>50.9</td>
<td>15.15</td>
<td>-52.0</td>
<td>41.8</td>
</tr>
<tr>
<td>N130</td>
<td>132.7</td>
<td>42.9</td>
<td>141.8</td>
<td>110.8</td>
</tr>
<tr>
<td>N200</td>
<td>204.3</td>
<td>-491</td>
<td>628</td>
<td>632</td>
</tr>
<tr>
<td>N520</td>
<td>681.3</td>
<td>169.5</td>
<td>564.0</td>
<td>442</td>
</tr>
</tbody>
</table>
This concludes the development of the nonlinear description of the CMOS small-signal model. The coefficient of the polynomial expansions describing the nonlinear performance of the CMOS small-signal model have derived using Mat-Lab from measured large-signal IV or CV data and physical process data. These predicted and derived descriptions for the nonlinear behavior of the CMOS small-signal model will be used to predict RF characteristics including linearity and noise whose detailed theoretical development is shown in Chapters IV and V.

### III.4 Computer Simulation of Small-Signal Model

The designs for this research program were completed in the Hewlett-Packard’s, now Agilent Technologies’ (AT), 0.35μm CMOS 14TB process administered through MOSIS at the University of Southern California, and fabricated at AT’s wafer foundry in California, USA, with one exception. The AT supplied an HSPICE BSIM3v1 model based on University of California, Berkeley geometrically enhanced SPICE or BSIM model. The CAD software package used in the design and simulation of the devices and circuits of this research program reported in this dissertation was Cadence Spectre, excepting one application in Pspice.

#### III.4.1 CMOS Transistor Simulation Model

In the beginning of the research program, it was desired to use Cadence’s Spectre RF software design tools based on BSIM3v3 to exploit the nonlinear
Figure III.27: The Converted Cadence Spectre Transistor Model of AT’s HSPICE BSIM3v3
Figure III.28: 2nd Part of The Converted Cadence Spectre Transistor Model of AT’s HSPICE BSIM3v3

Figure III.29: IBM SOS Transistor Simulation Model

estimation software. Thus a transistor model based upon the physical wafer process, in which the design would be carried out, was required. Equivalent models were created to provide for this need as seen in Figs. III.27 and III.28 from Pspice BSIM3v1. The main difference between the HSPICE version and the Cadence Spectre versions are that Cadence model in general does not support dimensionally segregated model files. Certain other coefficients in Cadence version of BSIM3v3 lack temperature dependence as well. The result makes HSPICE a more device specific transistor model than what Cadence provides.

Pspice was used to simulate a millimeter wave CMOS LNA at 26 to 28 GHz with models provided by IBM’s 0.15μm wafer foundry in Burlington, Vermont. A
copy of the models is shown in Fig. III.29. The complete discussion of the design based on these transistor simulation models is found in Chapter VII: LNA Design and the performance results are found in Chapter IX: Experimental Verification of Theory.

III.4.2 RF CMOS Simulation Techniques

While the I-V large-signal simulation of the transistor was successful in Cadence, the RF or small-signal simulation performance at 5.0 GHz was not. That is, the simulator was able to provide correct I-V curves for the circuits and approximately correct values for Power Gain but could not give reasonable values for NF and intermodulation distortion. Thus simulation experiments were conducted to try to improve the transistor simulation by adding additional components to bring the simulation predictions in line with measured results. This attempt did not prove successful because of a lack of control offered by Cadence software over the model and nonlinear calculations. Because the RF simulation linearity predictions were significantly different than the calculated and measured values continued work in attempting to improve the performance of Cadence for 5.0 GHz RF CMOS simulation was stopped in favor of direct theoretical calculation and measurement. The conclusion was that, without direct control of the modelling of nonlinear elements in the simulation schematic, little improvement could be realized further using Cadence RF Spectre tools in this application.

The comparison of measured and simulated results for $|S_{21}|$ shows poor
Figure III.30: ADS Transistor Simulation Schematic showing additional elements added for improved RF modeling
The comparison, in Fig. III.32, of measured and simulated results is improved.

However, a different simulator was used called ADS: Advanced Development System, which was based on the former AT’s Libra and MDS. The ADS schematic with the additional circuit components is shown in Fig. III.30 was used to further understand how much of an improvement in RF simulation could be realized. The results in predicting S-parameter performance versus actual measured data is shown in Fig. III.31. An improvement is realized with additional external components to the transistor in the schematic for simulation as seen in Fig. III.32. The transistor is simulated using the model file described in Subsection III.4.1.
Figure III.32: Polar plot of $|S_{21}|$ ADS Transistor Simulation Prediction after Model Enhancement.
III.4.3 Passive Element Simulation

The design of RF integrated circuits requires the use of resonating elements formed as inductors and capacitors. The prediction of the performance of inductors of different shapes was desired to predict the proper matching, quality factor, and noise of circuit designs. To this end, inductors were designed with layout tools from Tanner’s L-Edit in top-level metal, level four, of AT’s 0.35\(\mu\)m CMOS 14TB process, Fig. III.33. The layout file was imported to Sonnet’s Electromagnetic Simulator for prediction of inductance. The attempt to run the electromagnetic simulation on a Sun/Solaris Ultra 1 as seen in Fig. III.34 failed because of the required memory capacity for the matrix element partitioning of the inductor was exceeded significantly. Changes to the partitioning size did result in a reduced memory requirement and thus a lowered estimated run-time but also a significant increase in the error of the current density desired for inductance predictions. The run time estimates were in weeks of time.

The use of another electromagnetic simulator, Fast Henry, was also unsuc-
Figure III.34: Sonnet Run File for Spiral Inductance Prediction
cessful. The problem of Finite Element Method (FEM) in predicting small inductances from large integrated circuit metal area creates for both programs very large matrix sets, which require large computer resource to store and calculate. The software programs, Sonnet and Fast Henry, were created for macro-level and board-level simulations of inductance amongst other physical parameters. However, the problem of adapting the algorithms in these two programs to integrated circuit level simulations on desk-top computers is more demanding.

Thus the inductance of spiral metal layouts is predicted from geometrical formula in III.20. The results of the inductor and capacitor designs is compared to the predictions of III.20 in Chapter IX: Experimental Verification of Theory.

\[ L \approx \frac{45\mu_0n^2a^2}{22r - 14a} \quad \text{(III.20)} \]

The \( r \) is the outer radius of the spiral, \( a \) is the mean radius of the spiral, \( \mu_0 \) is the permeability of free space, \( n \) is the number of turns. This formula produces an estimate of 5 nH for the seven-turn inductor and 2 nH for the three-turn inductor [25].

### III.5 Device Design of Experiment

In order to check the validity of the theoretical predictions made in this chapter, passive and active circuit elements are designed. The first experiment designed was to evaluate resonant passive elements for the Quality Factor and
Table III.6: Design of Experiment II: Inductors

<table>
<thead>
<tr>
<th>Inductor</th>
<th>7-turn</th>
<th>3-turn</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Metal 1</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>N-well</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Metal 1/N-well</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>

performance as a function of design layout geometry, DOE II. The different categories of inductors composed an experiment, where the effects of shielding of the inductor from the eddy currents in the conductive substrate via metal 1 and n-well, could be checked.

One metal plate capacitor is included in this DOE II. The inductors and capacitor were measured and will be reported on in Chapter IX: Experimental Verification of Theory.

In DOE III additional inductors, shown in Table III.8, of seven- and three-turn were added to the test transistors listed in Table III.7. Also four MOS capacitors, improved calibration structures, and an LNA were added to the layout design. The transistor set of DOE III make up a design of experiment over gate structure by varying gate width and finger number. One common-gate design is included.

The inductor set of DOE III is different than DOE II where the shielding effectiveness of lower process layers to top level metal is studied. In this process metal four is the top level metal and shielding it to eddy currents in the lossy substrate of bulk CMOS is desired. The different categories of inductors composed an ex-
Table III.7: Test Transistor Geometry

<table>
<thead>
<tr>
<th>Device</th>
<th>Gate Finger Width in $\mu$m</th>
<th>Number of Fingers</th>
</tr>
</thead>
<tbody>
<tr>
<td>N50</td>
<td>5</td>
<td>10</td>
</tr>
<tr>
<td>N200</td>
<td>20</td>
<td>10</td>
</tr>
<tr>
<td>N130</td>
<td>5</td>
<td>26</td>
</tr>
<tr>
<td>N520</td>
<td>20</td>
<td>26</td>
</tr>
</tbody>
</table>

Table III.8: Design of Experiment III: Inductors

<table>
<thead>
<tr>
<th>Inductor</th>
<th>7-turn</th>
<th>3-turn</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>N-well</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Fractured N-well</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Fractured Poly/N-well</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Fractured Metal 1/N-well</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Fractured Poly</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Fractured Metal 1</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>

experiment, where the effects of shielding of the inductor from the eddy currents in the conductive substrate via polysilicon and n-well, could be checked. What is unknown and difficult to predict is the benefit of shielding the top-level metal from the lossy substrate to improve the Q of the inductors designed in this process. This is shown in Table III.8.

The capacitor set of DOE III is designed four MOS capacitors of increasing area to determine the scaling of capacitance as a function of junction area.

Transformers, inductors, and calibration structures are designed in DOE V with power amplifier designs in the Agilent Technologies (AT) 0.55$\mu$m CMOS process. The purpose of including transformers in DOE V was to determine their performance for use in a mixer design.
Table III.9: Test Capacitor Geometry

<table>
<thead>
<tr>
<th>Device</th>
<th>Area in $\mu m^2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOS1</td>
<td>630</td>
</tr>
<tr>
<td>MOS2</td>
<td>1206</td>
</tr>
<tr>
<td>MOS3</td>
<td>2440</td>
</tr>
<tr>
<td>MOS4</td>
<td>5040</td>
</tr>
</tbody>
</table>

Table III.10: Design of Experiment V: Inductors

<table>
<thead>
<tr>
<th>Inductor</th>
<th>3-turn</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate</td>
<td>✓</td>
</tr>
<tr>
<td>Poly, Fine Mesh</td>
<td>✓</td>
</tr>
<tr>
<td>Poly, Medium Mesh</td>
<td>✓</td>
</tr>
<tr>
<td>Poly, Finger narrow wide</td>
<td>✓</td>
</tr>
<tr>
<td>Poly, Finger wide with center taps</td>
<td>✓</td>
</tr>
<tr>
<td>N-well mesh</td>
<td>✓</td>
</tr>
<tr>
<td>No center tap</td>
<td>✓</td>
</tr>
</tbody>
</table>

The DOE V allows determination of the efficacy of different shielding for inductors in the Agilent Technologies (AT) 0.55 $\mu m$ CMOS process as described in Table VIII.5.

The transformer DOE provides a means of measuring the scaling as a function of transformer turns ratio as seen in Table VIII.6.

Table III.11: Design of Experiment V: Transformers

<table>
<thead>
<tr>
<th>Transformers over Poly, Medium Mesh</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>XTRM1</td>
<td>1:1</td>
</tr>
<tr>
<td>XTRM2</td>
<td>1:3</td>
</tr>
<tr>
<td>XTRM3</td>
<td>1:5</td>
</tr>
</tbody>
</table>
III.6 Summary

The mathematical and computer modelling of both devices and transistors has been reviewed in preparation for theoretical RF predictions and design work presented in later chapters. The use of large-signal data for deriving basic CMOS transistor modelling has been made. The use of small-signal data from S-parameters has been defined for later predictions of RF CMOS transistor performance. The use of small-signal data for deriving nonlinear polynomial expansions has been shown and will be employed to predict linearity in Chapter IV: Linearity and noise in Chapter V: Noise. The construction of transistor models for computer simulation based on physical processes has been described and reviewed. The attempt to use Finite Element Matrix methods to predict inductance has been reviewed, followed by geometrical prediction of spiral inductors.

The text of this chapter, in part, is a reprint of the material as it appears in our published papers in *IEEE Conferences* [SiRF03, Germany; IEDM99, USA] and in preparation for *Conferences and Transactions on Microwave Theory and Techniques*. The dissertation author was the primary investigator and primary and secondary author of these papers.
Chapter IV

Linearity Analysis of MOSFET’s

IV.1 Introduction

Intermodulation distortion is the key limitation on the dynamic range performance of a small-signal amplifier under large-signal conditions. Our goal here is to predict the nonlinear behavior, particularly third-order intermodulation distortion, as a function of device design, biasing, and impedance termination. The results can then be used in conjunction with the noise model of the device to optimize the dynamic range of an RF receiver [26, 27].

The intermodulation distortion is the result of a weakly nonlinear small-signal problem, in which the situation of multiple small-signal excitations is studied. The excitations are in-band and therefore nonfilterable. Understanding how to predict the presence of the nonlinearity improves the overall design objectives of making better radio receivers by increasing the Spur-Free Dynamic Range (SFDR). In-band unwanted distortion arises from many sources which can gener-
ally be referred to as spurious. The effect of the presence of spurious responses is to desensitize the receiver to a desired signal [28].

The many ways in which spurious responses are accounted for through coincidence and congruence of intermodulation frequencies is an extensive calculation which will not be shown here. Coincidence occurs when undesired intermodulation coincides with an IF output. Congruence occurs when undesired intermodulation occurs at the same value of an IF. These two mechanisms yield a reduction in IF selectivity and RF sensitivity for which an accounting method can generate a trouble list of interference modes [29].

A way of reducing the likelihood of such problems is to understand linearity as a figure of merit (FOM) based on the two-toned test. This test measures the response of an amplifier at its output to two slightly separated tones of equal magnitude at its input. The two tones at the input will re-appear at the output with harmonics of the two tones based on weakly nonlinear behavior of the amplifier. The separation of the fundamental tones from the odd harmonics at the output is the measure of the linearity of an amplifier. An amplifier is the basic circuit element of the all analog/RF design, it arises in LNA’s, VGA’s, Mixer’s, and buffers, amongst other examples.

If the combination of closely separated frequencies is examined, odd multiples will appear close to the fundamental, such as \( f_1 \) and \( f_2 \), whose odd-order intermodulation products (IMP), are \( 2f_2 - f_1 \) and \( 2f_1 - f_2 \). Even-order IMP are far
A powerful technique for analyzing the weakly nonlinear small-signal problem is a Volterra Analysis [26]. Volterra analysis does not make requirements on the circuit model to have separable memoryless nonlinear elements and frequency-sensitive linear components, as in power series analysis. The Volterra analysis could be compared to a transfer function where the phase and amplitude are changed as a result of the application of the function. Or, nonlinear circuit analysis could be used where the circuit components have nonlinear expressions for which the coefficients of the polynomial expansion of the nonlinearity can be determined. This analysis is used in the following sections of this chapter and could be applied a KCL or a KVL analyses of a circuit [26, 28]. The nonlinear circuit components can be resistive, reactive, or a combination. The basic model is shown in Fig. IV.1.

Volterra Analysis has in recent years been applied at 5 GHz to Si BJT’s
in [27] using a $g_m$ nonlinearity, and in Si CMOS [30, 31] by using four nonlin-
ear small-signal model components. Additional analyses, using Volterra anal-
ysis and multiple non-linear small-signal model components, based on SiGe or
GaAS FET’s are yet to be performed and reported. Intermodulation Distortion has
largely been reported in other circuit constructions in the literature by measure-
ment and without prior analysis and simulation. This work in part is the next step
in expanding markedly the robust application of theoretical constructs in Volterra
Analysis to ISM-band RF circuits operating under the constraint of minimized
power dissipation.

Finally, while the general solution for a two-port network in this situation is
very complex, a careful application of Volterra Series Analysis under narrowband
conditions with attention to the harmonics of the impedance values will yield ac-
curate results. We shall first examine the case where the effect of shunt feedback
is missing, $C_{gd} = 0$, in Section IV.2, and then examine the more general case of
including shunt feedback, $C_{gd}$, on linearity in Section IV.3, and finally we shall
compare the theoretical predictions to measurement in Chapter IX: Experimental
Verification of Theory.
IV.2 Grounded-Source Nonlinear Transfer Function of Output Circuit

Using the nonlinear element description of Chapter III in Sec. III.3.3, and the Volterra formalism [26] for the output voltage in terms of the input voltage at the gate yields

\[ v_{ds} = H_1 \circ v_{gs} + H_2 \circ v_{gs}^2 + H_3 \circ v_{gs}^3 + \ldots \]  

(IV.1)

and solving for the first order nonlinear transfer function yields

\[ H_1(\omega_n) = \frac{-a_1}{g_1 + y_L(\omega_n) + j\omega_n c_1} \]  

(IV.2)

where \( y_L \) is the load impedance in Fig. IV.2. The load impedance is determined by the matching network, \( M_L \), and \( R_{LOAD} \).

The second order transfer function is
The third-order nonlinear transfer function is more involved. Solving for KCL in the small-signal model Fig. IV.2 yields:

\[
\begin{align*}
H_2(\omega_a, \omega_b) &= - \frac{\left( a_2 + g_2 \ast \{ H_1(\omega_a)H_1(\omega_b) \} + \frac{a_2}{2} j(\omega_a + \omega_b) \{ H_1(\omega_a)H_1(\omega_b) \} \right)}{g_1 + c_1 j(\omega_a + \omega_b) + y_L(\omega_a + \omega_b)} \\
&= - \frac{\left( a_2 + \{ g_2 + \frac{a_2}{2} j(\omega_a + \omega_b) \} \ast \{ H_1(\omega_a)H_1(\omega_b) \} \right)}{g_1 + c_1 j(\omega_a + \omega_b) + y_L(\omega_a + \omega_b)} \\
&= - \frac{\left( a_2 + \left[ \{ g_2 + \frac{a_2}{2} j(\omega_a + \omega_b) \} \ast \{ \frac{a_2}{g_1 + y_L(\omega_a) + c_1 j(\omega_a + \omega_b) + y_L(\omega_a + \omega_b) \} \} \right] \right)}{g_1 + c_1 j(\omega_a + \omega_b) + y_L(\omega_a + \omega_b)} \\
&= 0 \quad (IV.4)
\end{align*}
\]

\[
\begin{align*}
a_3 \ast v_{gs}^3 + \\
g_1 \ast \{ H_3 \circ v_{gs}^3 \} + \\
g_2 \ast \{ H_1 \circ v_{gs} + H_2 \circ v_{gs}^2 \}^2 + \\
g_3 \ast \{ H_1 \circ v_{gs} \}^3 + \\
c_1 \frac{d}{dt} \{ H_3 \circ v_{gs}^3 \} + \\
\frac{c_2}{2} \frac{d}{dt} \{ H_1 \circ v_{gs} + H_2 \circ v_{gs}^2 \}^2 + \\
\frac{c_3}{3} \frac{d}{dt} \{ H_1 \circ v_{gs} \}^3 + \\
y_L \{ H_3 \circ v_{gs}^3 \} = 0
\end{align*}
\]
which can be expanded to be

\[ a_3 * v_{gs}^3 + \]

\[ g_1 * \left\{ H_3(\omega_a, \omega_b, \omega_c) \circ v_{gs}^3 \right\} + \]

\[ 2g_2 * \left\{ H_1(\omega_a)H_2(\omega_b, \omega_c) \circ v_{gs}^3 \right\} + \]

\[ g_3 * \left\{ H_1(\omega_a)H_1(\omega_b)H_1(\omega_c) \circ v_{gs}^3 \right\} + \]

\[ c_1 j (\omega_a + \omega_b + \omega_c) \left\{ H_3(\omega_a, \omega_b, \omega_c) \circ v_{gs}^3 \right\} + \]

\[ c_2 j (\omega_a + \omega_b + \omega_c) \left\{ H_1(\omega_a)H_2(\omega_b, \omega_c) \circ v_{gs}^3 \right\} + \]

\[ \frac{c_3}{3} j (\omega_a + \omega_b + \omega_c) \left\{ H_1(\omega_a)H_1(\omega_b)H_1(\omega_c) \circ v_{gs}^3 \right\} + \]

\[ y_L (\omega_a + \omega_b + \omega_c) \left\{ H_3(\omega_a, \omega_b, \omega_c) \circ v_{gs}^3 \right\} = 0 \] (IV.5)

where [26]

\[ \frac{1}{3} \left[ H_1(\omega_a)H_2(\omega_b, \omega_c) + H_1(\omega_b)H_2(\omega_a, \omega_c) + H_1(\omega_c)H_2(\omega_a, \omega_b) \right] \] (IV.6)

which can be further simplified to be

\[ \{ g_1 + c_1 j (\omega_a + \omega_b + \omega_c) + y_L (\omega_a + \omega_b + \omega_c) \} \left\{ H_3(\omega_a, \omega_b, \omega_c) \right\} = \]

\[ a_3 + 2g_2 + \left\{ H_1(\omega_a)H_2(\omega_b, \omega_c) \right\} + g_3 + \left\{ H_1(\omega_a)H_1(\omega_b)H_1(\omega_c) \right\} \]

\[ + c_2 j (\omega_a + \omega_b + \omega_c) \left\{ H_1(\omega_a)H_2(\omega_b, \omega_c) \right\} \]

\[ + \frac{c_3}{3} j (\omega_a + \omega_b + \omega_c) \left\{ H_1(\omega_a)H_1(\omega_b)H_1(\omega_c) \right\} \] (IV.7)

and finally

\[ H_3(\omega_a, \omega_b, \omega_c) = \]
\[
\begin{align*}
&\left\{ a_3 + 2g_2 \left\{ H_1(\omega_a)H_2(\omega_b, \omega_c) \right\} + g_3 \left\{ H_1(\omega_a)H_1(\omega_b)H_1(\omega_c) \right\} \\
&+ e_2 j (\omega_a + \omega_b + \omega_c) \left\{ H_1(\omega_a)H_2(\omega_b, \omega_c) \right\} \\
&+ \left( g_3 + \frac{a_3}{3} j (\omega_a + \omega_b + \omega_c) \right) \left\{ H_1(\omega_a)H_1(\omega_b)H_1(\omega_c) \right\} \\
&\right\} \\
&\left\{ g_1 + e_1 j (\omega_a + \omega_b + \omega_c) + y_L (\omega_a + \omega_b + \omega_c) \right\}
\end{align*}
\] (IV.8)

which can be simplified to be

\[
H_3(\omega_a, \omega_b, \omega_c) =
\left\{ a_3 + 2g_2 \left( 2g_2 + e_2 j (\omega_a + \omega_b + \omega_c) \right) \right\} \left\{ H_1(\omega_a)H_2(\omega_b, \omega_c) \right\} \\
+ \left( g_3 + \frac{a_3}{3} j (\omega_a + \omega_b + \omega_c) \right) \left\{ H_1(\omega_a)H_1(\omega_b)H_1(\omega_c) \right\} \\
\right\} \\
\left\{ g_1 + e_1 j (\omega_a + \omega_b + \omega_c) + y_L (\omega_a + \omega_b + \omega_c) \right\}
\] (IV.9)

where the permutation of \( H_1(\omega_a) \) and \( H_2(\omega_b, \omega_c) \) was defined in IV.6 [26].

### IV.2.1 Grounded-Source Nonlinear Transfer Function of Input Circuit

Next, we analyze the input circuit which consists of the linear input source \( y_s \), and the nonlinear capacitance \( C_{gs} \), as shown in Fig. IV.2. The current through the input capacitor can be expressed by

\[
i_{c_{gs}} = c_{g1} \frac{dv_{gs}}{dt} + c_{g2} \frac{dv_{gs}^2}{2} \frac{dt}{dt} + c_{g3} \frac{dv_{gs}^3}{3} \frac{dt}{dt}
\] (IV.10)

Now, using the Volterra formalism for the gate voltage in terms of the source current yields

\[
v_{gs} = G_1 \circ i_s + G_2 \circ i_s^2 + G_3 \circ i_s^3
\] (IV.11)
and solving at the input node yields

\[-i_s + c_{g1} \frac{dv_{gs}}{dt} + \frac{c_{g2}}{2} \frac{dv_{gs}^2}{dt} + \frac{c_{g3}}{3} \frac{dv_{gs}^3}{dt} + y_s v_{gs} = 0 \quad \text{(IV.12)}\]

Now, expanding [IV.12]

\[-i_s + c_{g1} \frac{d}{dt} \left( G_1 \circ i_s + G_2 \circ i_s^2 + G_3 \circ i_s^3 \right) + \frac{c_{g2}}{2} \frac{d}{dt} \left( G_1 \circ i_s + G_2 \circ i_s^2 + G_3 \circ i_s^3 \right)^2 + \frac{c_{g3}}{3} \frac{d}{dt} \left( G_1 \circ i_s + G_2 \circ i_s^2 + G_3 \circ i_s^3 \right)^3 + y_s \left( G_1 \circ i_s + G_2 \circ i_s^2 + G_3 \circ i_s^3 \right) = 0 \quad \text{(IV.13)}\]

Now, we can equate terms to find the Volterra G coefficients. Equating first-order terms, we obtain

\[-i_s + c_{g1} \frac{d}{dt} \left( G_1 \circ i_s \right) + y_s \left( G_1 \circ i_s \right) = 0 \quad \text{(IV.14)}\]

which implies that

\[-1 + c_{g1} j \omega_a \left( G_1 \right) + y_s \left( G_1 \right) = 0 \quad \text{(IV.15)}\]

or

\[G_1(\omega_a) = \frac{1}{y_s(\omega_a) + c_{g1} j \omega_a} \quad \text{(IV.16)}\]

Equating second-order terms, we get

\[c_{g1} \frac{d}{dt} \left( G_2 \circ i_s^2 \right) + \frac{c_{g2}}{2} \frac{d}{dt} \left( G_1 \circ i_s \right)^2 + y_s \left( G_2 \circ i_s^2 \right) = 0 \quad \text{(IV.17)}\]
and
\[
c_{g1} \frac{d}{dt} \left\{ G_2(\omega_a, \omega_b) \circ i_s^2 \right\} + \frac{c_{g2}}{2} \frac{d}{dt} \left\{ G_1(\omega_a)G_1(\omega_b) \circ i_s^2 \right\} + \\
y_s \left\{ G_2(\omega_a, \omega_b) \circ i_s^2 \right\} = 0 \tag{IV.18}
\]
which further implies that
\[
c_{g1}j(\omega_a + \omega_b) \left\{ G_2(\omega_a, \omega_b) \circ i_s^2 \right\} + \\
\frac{c_{g2}}{2} j(\omega_a + \omega_b) \left\{ G_1(\omega_a)G_1(\omega_b) \circ i_s^2 \right\} + \\
y_s(\omega_a + \omega_b) \left\{ G_2(\omega_a, \omega_b) \circ i_s^2 \right\} = 0 \tag{IV.19}
\]
which implies that
\[
c_{g1}j(\omega_a + \omega_b) + y_s(\omega_a + \omega_b) \left\{ G_2(\omega_a, \omega_b) \right\} = \\
-\frac{c_{g2}}{2} j(\omega_a + \omega_b) \left\{ G_1(\omega_a)G_1(\omega_b) \right\} \tag{IV.20}
\]
which finally implies that
\[
G_2(\omega_a, \omega_b) = -\frac{c_{g2}}{2} j(\omega_a + \omega_b) \left\{ G_1(\omega_a)G_1(\omega_b) \right\} \\
\left\{ c_{g1}j(\omega_a + \omega_b) + y_s(\omega_a + \omega_b) \right\} \left\{ y_s(\omega_a) + c_{g1}j\omega_a \right\} \left\{ y_s(\omega_b) + c_{g1}j\omega_b \right\} \tag{IV.21}
\]
This can be further reduced to
\[
G_2(\omega_a, \omega_b) = \\
-\frac{c_{g2}}{2} j(\omega_a + \omega_b) \\
\left\{ c_{g1}j(\omega_a + \omega_b) + y_s(\omega_a + \omega_b) \right\} \left\{ y_s(\omega_a) + c_{g1}j\omega_a \right\} \left\{ y_s(\omega_b) + c_{g1}j\omega_b \right\} \tag{IV.22}
\]
Equating third-order terms yields:
\[
c_{g1} \frac{d}{dt} \left\{ G_3 \circ i_s^3 \right\} + \\
\]
\[
\frac{c_g2}{2} \frac{d}{dt} \left\{ G_1 \circ i_s + G_2 \circ i_s^2 \right\}^2 + \\
\frac{c_g3}{3} \frac{d}{dt} \left\{ G_1 \circ i_s \right\}^3 + \\
y_s \left\{ G_3 \circ i_s^3 \right\} = 0
\] (IV.23)

which can be expanded to be

\[
\begin{align*}
&c_g1j \left( \omega_a + \omega_b + \omega_c \right) \left\{ G_3(\omega_a, \omega_b, \omega_c) \circ i_s^3 \right\} + \\
&c_g2j \left( \omega_a + \omega_b + \omega_c \right) \left\{ G_1(\omega_a)G_2(\omega_b, \omega_c) \circ i_s^3 \right\} + \\
&\frac{c_g3}{3} j \left( \omega_a + \omega_b + \omega_c \right) \left\{ G_1(\omega_a)G_1(\omega_b)G_1(\omega_c) \circ i_s^3 \right\} + \\
y_s \left( \omega_a + \omega_b + \omega_c \right) \left\{ G_3(\omega_a, \omega_b, \omega_c) \circ i_s^3 \right\} = 0
\end{align*}
\] (IV.24)

which can be further simplified to be

\[
\begin{align*}
\{ G_3(\omega_a, \omega_b, \omega_c) \} &= \\
&\left\{ \begin{array}{c} \\
\left[ \begin{array}{c} c_g1j \left( \omega_a + \omega_b + \omega_c \right) \left\{ G_3(\omega_a, \omega_b, \omega_c) \right\} + \\
c_g2j \left( \omega_a + \omega_b + \omega_c \right) \left\{ G_1(\omega_a)G_2(\omega_b, \omega_c) \right\} + \\
\frac{c_g3}{3} j \left( \omega_a + \omega_b + \omega_c \right) \left\{ G_1(\omega_a)G_1(\omega_b)G_1(\omega_c) \right\} \\
c_g1j \left( \omega_a + \omega_b + \omega_c \right) + y_s \left( \omega_a + \omega_b + \omega_c \right) \end{array} \right\} \\
\end{array} \right\} \\
\end{align*}
\] (IV.25)

which, when expanded yields

\[
\{ G_3(\omega_a, \omega_b, \omega_c) \} =
\]
IV.2.2 Total Nonlinear Transfer Function

Next, we calculate the complete transfer function without $C_{gd}$ feedback.

Now, the total transfer function $K$ is the product of the two transfer functions $H$ and $G$. So,

\[ v_{ds} = H_1 \circ \{ G_1 \circ i_s + G_2 \circ i_s^2 + G_3 \circ i_s^3 \} + \]

\[ H_2 \circ \{ G_1 \circ i_s + G_2 \circ i_s^2 + G_3 \circ i_s^3 \}^2 + \]

\[ H_3 \circ \{ G_1 \circ i_s + G_2 \circ i_s^2 + G_3 \circ i_s^3 \}^3 \]  \hspace{1cm} (IV.27)

or

\[ v_{ds} = K_1 \circ i_s + K_2 \circ i_s^2 + K_3 \circ i_s^3 + \cdots \]  \hspace{1cm} (IV.28)

Equating first order terms we get

\[ v_{ds} = H_1 \circ \{ G_1 \circ i_s \} \]  \hspace{1cm} (IV.29)
This is the first-order transfer function.

Now equating the second-order terms we get

\[ v_{ds} = H_1 \circ \{ G_2 \circ i_a^2 \} + H_2 \circ \{ G_1 \circ i_s \}^2 \]  

(IV.31)

which leads to

\[ K_2(\omega_a, \omega_b) \circ i_s^2 = H_1(\omega_a + \omega_b) \circ \{ G_2(\omega_a, \omega_b) \circ i_s^2 \} + H_2(\omega_a, \omega_b) \circ \{ G_1(\omega_a)G_1(\omega_b) \circ i_s^2 \} \]  

(IV.32)

and finally

\[ K_2(\omega_a, \omega_b) = H_1(\omega_a + \omega_b)\{ G_2(\omega_a, \omega_b) \} + H_2(\omega_a, \omega_b)\{ G_1(\omega_a)G_1(\omega_b) \} \]  

(IV.33)

which, yields

\[ K_2(\omega_a, \omega_b) = \left\{ \begin{array}{c}
\frac{a_1}{2} \frac{c_2}{j} (\omega_a + \omega_b) \\
\{ g_1 + y_L(\omega_a + \omega_b) + c_1 j(\omega_a + \omega_b) \} \\
\{ c_{g1} j(\omega_a + \omega_b) + y_s(\omega_a + \omega_b) \} \\
\{ y_s(\omega_a) + c_{g1} j\omega_a \} \{ y_s(\omega_b) + c_{g1} j\omega_b \}
\end{array} \right\} - \]
which can be somewhat simplified to be

\[ K_2(\omega_a, \omega_b) = \left\{ \begin{array}{l}
\{a_1\} \frac{c_{g2}}{2} j(\omega_a + \omega_b)
\end{array} \right\}

\begin{align*}
&\left( a_2 + \frac{\{g_2 + \frac{c_{g2}}{2} j(\omega_a + \omega_b)\} a_1^2}{\{g_1 + y_L(\omega_a) + c_1 j\omega_a\}} \right) * \\
&\{y_s(\omega_a) + c_{g1} j\omega_a\} * \\
&\{y_s(\omega_b) + c_{g1} j\omega_b\}
\end{align*}

(IV.34)
Now equating third-order terms, 

\[ v_{ds} = H_1 \circ \left\{ G_3 \circ i_s^3 \right\} + H_2 \circ \left\{ G_1 \circ i_s + G_2 \circ i_s^2 \right\}^2 + H_3 \circ \left\{ G_1 \circ i_s \right\}^3 \]  

(IV.36)

This then becomes

\[ v_{ds} = H_1 (\omega_a + \omega_b + \omega_c) \circ \left\{ G_3 (\omega_a, \omega_b, \omega_c) \circ i_s^3 \right\} + 
\]

\[ H_2 (\omega_a, \omega_b + \omega_c) \circ 2 \left\{ G_1 (\omega_a) G_2 (\omega_b, \omega_c) \circ i_s^3 \right\} + 
\]

\[ H_3 (\omega_a, \omega_b, \omega_c) \circ \left\{ G_1 (\omega_a) G_1 (\omega_b) G_1 (\omega_c) \circ i_s^3 \right\} \]  

(IV.37)

\[ K_3 (\omega_a, \omega_b, \omega_c) = H_1 (\omega_a + \omega_b + \omega_c) \circ \left\{ G_3 (\omega_a, \omega_b, \omega_c) \right\} + 
\]

\[ H_2 (\omega_a, \omega_b + \omega_c) \circ 2 \left\{ G_1 (\omega_a) G_2 (\omega_b, \omega_c) \right\} + 
\]

\[ H_3 (\omega_a, \omega_b, \omega_c) \circ \left\{ G_1 (\omega_a) G_1 (\omega_b) G_1 (\omega_c) \right\} \]  

(IV.38)

Next,

\[ K_3 (\omega_a, \omega_b, \omega_c) = H_1 (\omega_a + \omega_b + \omega_c) \{ G_3 (\omega_a, \omega_b, \omega_c) \} + 
\]

\[ \frac{2}{3} H_2 (\omega_a, \omega_b + \omega_c) \{ G_1 (\omega_a) G_2 (\omega_b, \omega_c) \} + \]

\[ \frac{2}{3} H_2 (\omega_b, \omega_a + \omega_c) \{ G_1 (\omega_b) G_2 (\omega_a, \omega_c) \} + \]

\[ \frac{2}{3} H_2 (\omega_c, \omega_a + \omega_b) \{ G_1 (\omega_c) G_2 (\omega_a, \omega_b) \} + \]

\[ H_3 (\omega_a, \omega_b, \omega_c) \{ G_1 (\omega_a) G_1 (\omega_b) G_1 (\omega_c) \} \]  

(IV.39)

At this point, the algebra is extremely complex. To simplify the analysis, we assume that we are doing a two-tone intermodulation distortion test; so that, 

\[ \omega_a = \omega_1, \omega_b = \omega_1, \text{ and } \omega_c = -\omega_2 \text{ and } |\omega_1| \approx |\omega_2|. \]
Since the sum of frequency in first two $H_2$ terms of IV.39 produce zero for the second term of $H_2$, and thus the transfer functions become independent of frequency or dc or large-signal values, not in the frequency band of prediction, the $G_2$ terms go to zero. Then, with two of the three $H_2$ terms in IV.39 collapsing with the above substitutions, we get,

\[
K_3(\omega_1, \omega_1, -\omega_2) = H_1(\omega_1) \{G_3(\omega_1, \omega_1, -\omega_2)\} + 2/3H_2(-\omega_2, 2\omega_1) \{G_1(-\omega_2)G_2(\omega_1, \omega_1)\} + H_3(\omega_1, \omega_1, -\omega_2) \{G_1(\omega_1)^2G_1(-\omega_2)\} \tag{IV.40}
\]

where from IV.9 and substituting in the above,

\[
H_3(\omega_1, \omega_1, -\omega_2) = \left\{\frac{a_3 + (2g_2 + c_2 j(\omega_1)) * \{H_1(\omega_1)H_2(\omega_1, -\omega_2)\}}{\{g_1 + c_1 j(\omega_1) + y_L(\omega_1)\} + (g_3 + \frac{a_2}{2} j(\omega_1)) * \{H_1(\omega_1)H_1(\omega_1)H_1(-\omega_2)\}} \right\} \tag{IV.41}
\]

and

\[
H_2(\omega_1, \omega_1) = \frac{\left[a_2 (g_1 + y_L(\omega_1) + c_1 j\omega_1)^2 + a_1^2 \left[g_2 + \frac{a_2}{2} j(2\omega_1)\right]\right]}{\left[g_1 + c_1 j(2\omega_1) + y_L(2\omega_1)\right] (g_1 + c_1 j(\omega_1) + y_L(\omega_1))^2} \tag{IV.42}
\]

and

\[
H_2(\omega_1, -\omega_2) = \frac{-a_2 \{\left[g_1 + y_L(\omega_1) + c_1 j\omega_1\right] \{g_1 + y_L(-\omega_2) + c_1 j\omega_2)\}] + a_1^2 \left[g_2\right]}{g_1 \left[\left(g_1 + y_L(\omega_1) + c_1 j\omega_1\right) \{g_1 + y_L(-\omega_2) + c_1 j\omega_2\}\right]} \tag{IV.43}
\]
and

\[ H_2(-\omega_2, 2\omega_1) = \]
\[
\begin{bmatrix}
  a_2 (g_1 + y_L(-\omega_2) - c_1 j\omega_1) \\
  (g_1 + y_L(2\omega_1) + c_1 j2\omega_1)
\end{bmatrix}
+ a_1^2 \left[ g_2 + \frac{c_2}{2} j\omega_1 \right]
\]
\[
[ g_1 + c_1 j(2\omega_1) + y_L(2\omega_1) ]^* \\
(g_1 + c_1 j(\omega_1) + y_L(\omega_1))(g_1 - c_1 j(\omega_2) + y_L(-\omega_2))
\]

(IV.44)

and with

\[ H_1(\omega_1) H_2(\omega_1, -\omega_2) = \]
\[
\frac{1}{3} \left[ 2H_1(\omega_1) H_2(\omega_1, -\omega_2) + H_1(-\omega_2) H_2(\omega_1, \omega_1) \right]
\]

(IV.45)

A fairly complete derivation of \( H_i \) where \( i = 1, 2, 3 \) Volterra transfer functions for the output have been derived. Now, we need to calculate \( G_2 \) and \( G_3 \) with \( \omega_1 \) and \( \omega_2 \) substituted in. The \( G_i \), where \( i = 1, 2, 3 \) Volterra Transfer functions represent the input nonlinearities, as follows:

\[
G_2(\omega_1, \omega_1) = \frac{-c_{g2} j(\omega_1)}{\{ c_{g1} j(2\omega_1) + y_s(2\omega_1) \} \{ (y_s(\omega_1) + c_{g1} j\omega_1)^2 \}}
\]

(IV.46)

\[
\{ G_3(\omega_1, \omega_1, -\omega_2) \} = 
\]
and so the final transfer function, with many of the above derived equations, substituted into IV.40 is

\[
\begin{aligned}
\left\{ \frac{-2/3}{c_{g2}j(\omega_1)} \right\}^2 +
\left\{ \frac{c_{g3}j(\omega_1)}{3} \right\} \left\{ \{c_{g1}j(2\omega_1) + y_s(2\omega_1)\} \right\}
\left\{ y_s(-\omega_2) - c_{g1}j\omega_2 \right\} \left\{ c_{g1}j(2\omega_1) + y_s(2\omega_1) \right\}
\left\{ y_s(\omega_1) + c_{g1}j\omega_1 \right\}^3
\end{aligned}
\]

(IV.47)

which can be further simplified to

\[
\{ G_3(\omega_1, \omega_1, -\omega_2) \} =
\begin{aligned}
\left\{ \frac{-2/3}{c_{g2}j(\omega_1)} \right\}^2 +
\left\{ \frac{c_{g3}j(\omega_1)}{3} \right\} \left\{ \{c_{g1}j(2\omega_1) + y_s(2\omega_1)\} \right\}
\left\{ y_s(-\omega_2) - c_{g1}j\omega_2 \right\} \left\{ c_{g1}j(2\omega_1) + y_s(2\omega_1) \right\} *
\left\{ y_s(\omega_1) + c_{g1}j\omega_1 \right\}^3
\end{aligned}
\]

(IV.48)

and so the final transfer function, with many of the above derived equations, substituted into IV.40 is

\[
K_3(\omega_1, \omega_1, -\omega_2) =
\begin{aligned}
\left\{ \frac{-a_1}{g_1 + y_L(\omega_1) + c_{1}j\omega_1} \right\}
\left\{ \frac{-1/3}{c_{g2}j(\omega_1)} \right\}^2 +
\left\{ \frac{c_{g3}j(\omega_1)}{3} \right\} *
\left\{ \{c_{g1}j(2\omega_1) + y_s(2\omega_1)\} \right\}
\left\{ y_s(-\omega_1) - c_{g1}j\omega_1 \right\} \left\{ c_{g1}j(2\omega_1) + y_s(2\omega_1) \right\} *
\left\{ y_s(\omega_1) + c_{g1}j\omega_1 \right\}^3
\end{aligned}
\]
which can be further expanded to

\[
K_3(\omega_1, \omega_1, -\omega_2) =
\frac{1}{g_1 + y_L(\omega_1) + c_1 j \omega_1}
\left\{ \frac{a_2 (g_1 + y_L(-\omega_2) - c_1 j \omega_1) (g_1 + y_L(2 \omega_1) + c_1 j 2 \omega_1) +}{a_1^2 \left[ g_2 + \frac{\omega}{2} j \omega_1 \right]} \right. \nonumber
\]

\[2/3 \nonumber\]

\[
\left\{ \begin{array}{c}
[g_1 + c_1 j (2 \omega_1) + y_L(2 \omega_1)] (g_1 + c_1 j (\omega_1) + y_L(\omega_1)) * \\
(g_1 - c_1 j (\omega_2) + y_L(-\omega_2)) \\
\end{array} \right. \right\} + 
\left\{ \begin{array}{c}
\frac{1}{y_s(-\omega_2) - e_{g1} j \omega_2} \\
\{c_{g1} j (2 \omega_1) + y_s(2 \omega_1)\} y_s(\omega_1) + c_{g1} j \omega_1 \\
\end{array} \right. \right\} + 
\left\{ \begin{array}{c}
a_3 + (2 g_2 + c_2 j (\omega_1)) * \{H_1(\omega_1) H_2(\omega_1, -\omega_2)\} \\
+ (g_3 + \frac{\omega}{2} j (\omega_1)) * \{H_1(\omega_1) H_1(\omega_1) H_1(-\omega_2)\} \\
g_1 + c_1 j (\omega_1) + y_L(\omega_1) \\
\end{array} \right. \right\} + 
\left\{ \begin{array}{c}
\left( \frac{1}{y_s(\omega_1) + c_{g1} j \omega_1} \right)^2 \left( \frac{1}{y_s(-\omega_2) - c_{g1} j \omega_2} \right) \\
(\omega_1) \right. \right\}
\]
\[
\left\{\begin{array}{l}
\frac{1}{y_s(-\omega_2) - c_gj\omega_2} \\
y_s(2\omega_1) + y_s(2\omega_1) + c_gj\omega_1^2
\end{array}\right\} + \\
\left\{\begin{array}{l}
a_3 + (2g_2 + c_2j(\omega_1)) * \\
\frac{1}{3} \left[ 2H_1(\omega_1) H_2(\omega_1, -\omega_2) + H_1(-\omega_2) H_2(\omega_1, \omega_1) \right] \\
+ (g_3 + \frac{c_3}{3} j(\omega_1)) * \left( \frac{-a_1}{g_1 + y_L(\omega_1) + c_1j\omega_1} \right)^2 * \\
\frac{-a_1}{g_1 + y_L(-\omega_2) - c_1j\omega_2} \\
\{g_1 + c_1j(\omega_1) + y_L(\omega_1)\}
\end{array}\right\}
\]

(IV.50)

which is expanded finally to

\[
K_3(\omega_1, \omega_1, -\omega_2) = \\
\left\{\begin{array}{l}
\frac{-a_1}{g_1 + y_L(\omega_1) + c_1j\omega_1}
\end{array}\right\} *
\]

(IV.51)
\[
\begin{align*}
&\left\{ \left[ -\frac{1}{3} \right] \left\{ c_2 j(\omega_1) \right\}^2 + \left\{ \frac{c_3}{3} j(\omega_1) \right\} * \right\} - \\
&\left\{ \left[ c_{g1} j(2\omega_1) + y_s(2\omega_1) \right] \right\} + \\
&\left\{ y_s(-\omega_1) - c_{g1} j\omega_1 \right\} \left\{ c_{g1} j(2\omega_1) + y_s(2\omega_1) \right\} * \\
&\left\{ y_s(\omega_1) + c_{g1} j\omega_1 \right\}^3 \\
&\left\{ a_2 (g_1 + y_L(-\omega_2) - c_{1} j\omega_1) (g_1 + y_L(2\omega_1) + c_{1} j2\omega_1) \right\} + \\
&\frac{a_1^2 \left[ g_2 + \frac{g_1}{2} j\omega_1 \right]}{g_1 + c_1 j(2\omega_1) + y_L(2\omega_1) (g_1 + c_1 j(\omega_1) + y_L(\omega_1))} \left( g_1 - c_1 j(\omega_2) + y_L(-\omega_2) \right) \\
&\left\{ \left\{ \frac{1}{y_s(-\omega_2) - c_{g1} j\omega_2} \right\} - \frac{-c_2}{2} j(2\omega_1) \right\} + \\
&\left\{ \left\{ c_{g1} j(2\omega_1) + y_s(2\omega_1) \right\} * \right\} - \\
&\left\{ y_s(\omega_1) + c_{g1} j\omega_1 \right\}^2
\end{align*}
\]
The transfer function is dependent on all nonlinear modelling terms derived in Chapter III. Also, the transfer function depends on the matching and harmonics of matching termination impedances. These facts about the third-order transfer function have implications which will be discussed in Section IV.4.

This is the complete third-order transfer function with all terms present.

The transfer function is dependent on all nonlinear modelling terms derived in Chapter III. Also, the transfer function depends on the matching and harmonics of matching termination impedances. These facts about the third-order transfer function have implications which will be discussed in Section IV.4.
IV.2.3 Third-Order Intermodulation Distortion in Volterra Transfer Form

Now, the ratio of the third-order transfer function to the first-order is third-order intermodulation distortion defined as [26, 28, 32]

\[ IMD_3 = \frac{3 |K_3(\omega_1, \omega_1, -\omega_2)|}{4 |K_1(\omega_2)||K_1(\omega_1)|^2 s_o^2} \] (IV.53)

The output \( IMD_3 \) can be rewritten in terms of input power from the relation

\[ s_o^2 \cong |K_1(\omega_2)|^2 * s_i^2 \] (IV.54)

to

\[ IMD_3 = \frac{3 |K_3(\omega_1, \omega_1, -\omega_2)|}{4 |K_1(\omega_2)|} s_i^2 \] (IV.55)

Now \( IIIP_3 \) is the third order input intermodulation intercept point and can be computed from the following:

\[ IIIP_3 = \frac{IMD_3}{2} + P_\Delta \] (IV.56)

where \( P_\Delta \) is the input power, \( S_i \), at the \( IMD_3 \) [29]. The relationship between these last two equations will be discussed more completely in Chapter VI: Optimum Design for CMOS RF Amplifiers. Now, the \( IMD_3 \) is the ratio of the third-order non-linear transfer function or Volterra Kernel to the first order non-linear transfer function. The intermodulation distortion is a predict by a ratio of non-linear transfer functions at a specific input signal power. These non-linear transfer functions contain the the terms describing the non-linear small-signal circuit elements and the matching impedance terms. These two groups of terms determine
completely the prediction of $III P_3$ for a MOSFET. An assertion yet to be proven is that the theory and technique is sufficiently general to be applied to any amplifier or circuit containing non-linear elements and predict the $III P_3$ performance. However, in this research only CMOS has been used to verify the predictive power of the non-linear transfer function analysis of Volterra Series.

IV.3 The Effect of Shunt Feedback on Linearity

Next the effect of $C_{gd}$ on the linearity will be developed via a modified small-signal model taking into account the changes caused by linear feedback. We begin by examining Fig. IV.3 where the small-signal model has been restructured into a shunt-shunt feedback model. The linear feedback comes from $C_{gd}$ and its contribution to the current in the input and output loop circuits has been distributed from the structure of Fig. III.12 [32]. The next step is to associate the feedback model of Fig. IV.3 with a closed-loop block diagram system where components can be grouped and divided into linear and nonlinear contribution to the amplifier output. Once the association is made then the nonlinear analysis of Sec. IV.2 can be modified to include the effect of linear feedback on the form of the final transfer functions. The last step before defining the modification of the equations for inclusion of feedback is to transform the circuit of Fig. IV.3 into the closed loop block diagram of Fig. IV.4. From the construction of Fig. IV.4, the circuit components responsible for the different contributions to the output can be seen
Figure IV.3: Shunt-Shunt Feedback Model for Linearity

Figure IV.4: Closed-Loop Block Diagram for Linearity Feedback System
clearly.

The feedback terms of the circuit, $\beta$, can be identified from Fig. IV.4,

$$\beta_1(\omega_1) = \beta_1 = -j\omega_1 c_{pd}$$  \hspace{1cm} (IV.57)

where

$$\beta_2(\omega_1, \omega_1) = 0$$  \hspace{1cm} (IV.58)

and where

$$\beta_3(\omega_1, \omega_1, -\omega_2) = 0$$  \hspace{1cm} (IV.59)

Next the gain reduction factor is found

$$R(\omega_1) = \frac{1}{1 + K_1(\omega_1)\beta_1(\omega_1)}$$  \hspace{1cm} (IV.60)

With these definitions, the overall Volterra Kernels can be expressed with linear feedback. Starting with first order, expressions for the modified Volterra Kernels can be stated [32], where the overall transfer function is of this form:

$$v_{ds} = Q_1(\omega_a) \circ i_s + Q_2(\omega_a, \omega_b) \circ i_s^2 + Q_3(\omega_a, \omega_b, \omega_c) \circ i_s^3 + \cdots$$  \hspace{1cm} (IV.61)

Thus for the two-toned case,

$$Q_1(\omega_1) = \frac{K_1(\omega_1)}{[1 + K_1(\omega_1)\beta(\omega_1)]}$$  \hspace{1cm} (IV.62)

and

$$Q_2(\omega_1, \omega_1) = (R(\omega_1))^2 R(2\omega_1) K_2(\omega_1, \omega_1)$$  \hspace{1cm} (IV.63)
and

\[ Q_3(\omega_1, \omega_1, -\omega_2) = (R(\omega_1))^3 \left[ K_3(\omega_1, \omega_1, -\omega_2) \right. \]
\[ - \frac{2 K_2(\omega_1, \omega_1) K_2(\omega_1, 2\omega_1)}{K_1(2\omega_1)} ] R(3\omega_1) \]

(IV.64)

Some expansion and substitution of terms will be required to create the final form of the Volterra Kernels with linear feedback. The following derivation relies on the results of Sec. IV.2.

\[ Q_3(\omega_1, \omega_1, -\omega_1) = \]
\[ \left[ 1 + \frac{-\alpha_1}{\{g_1 + y_1(\omega_1) + j\omega_1 c_1\} \{y_s(-\omega_2) - j\omega_1 c_{g1}\}} \right]^{-3} \]
\[
\left\{ \frac{-a_1}{g_1 + y_L(\omega_1) + c_1 j \omega_1} \right\} + \left\{ \left[ -\frac{1}{3} \right] \left\{ c_{y_j2}(\omega_1) \right\}^2 + \left\{ \frac{c_{y_j2}}{g_1} j(\omega_1) \right\} \left\{ \left\{ c_{y_j1}(2\omega_1) + y_j(2\omega_1) \right\} \right\} \right\} + \frac{2}{3} \left\{ \frac{a_2(g_1 + y_L(\omega_1) + c_1 j \omega_1)(g_1 + y_L(\omega_1) + c_1 j \omega_1) + a_2^2(g_2 + \frac{2}{g_1} j(2\omega_1))}{g_1 + y_L(2\omega_1) + y_L(\omega_1)(g_1 + c_1 j(\omega_1) + y_L(\omega_1))(g_1 - c_1 j(2\omega_1) + y_L(-\omega_2))} \right\} + \left\{ \frac{1}{3} \left\{ \frac{-a_1}{g_1 + y_L(\omega_1) + c_1 j \omega_1} \right\}^2 + \frac{1}{3} \left\{ \frac{a_2(g_1 + y_L(\omega_1) + c_1 j \omega_1)^2 + a_2^2\left( g_2 + \frac{2}{g_1} j(2\omega_1) \right)}{g_1 + c_1 j(2\omega_1) + y_L(2\omega_1)(g_1 + c_1 j(\omega_1) + y_L(\omega_1))} \right\} \right\} + \left\{ \left( g_3 + \frac{2}{3} j(\omega_1) \right) * \left( \frac{-a_1}{g_1 + y_L(\omega_1) + c_1 j \omega_1} \right)^2 * \frac{-a_1}{g_1 + y_L(\omega_1) + c_1 j \omega_1} \right\} \right\} = \left\{ \left( \frac{1}{y_j(\omega_1) + c_1 j \omega_1} \right)^2 \left( \frac{1}{y_j(-\omega_2) - c_1 j \omega_2} \right) \right\}.
\]
Updating the prior reference to $IMD_3$ with the feedback Volterra Kernels to

$$IMD_3 = \frac{3|Q_3(j\omega_1, j\omega_1, -j\omega_2)|}{4|Q_1(j\omega_1)|} s_i^2$$ \hspace{1cm} (IV.66)$$

From IV.66 linearity performance can now be predicted from all four sources of nonlinearity in the small-signal model shown in Fig. III.12 with known values for the terminating impedances at $j\omega_1$, $2j\omega_1$, and $3j\omega_1$. The feedback form of nonlinear transfer function of Volterra Series includes terms from the formulation of the feedback analysis which reduce the prediction of $IMD_3$. The second term in IV.65, estimates the effect of second-order interacting with the first order to produce an additional third-order intermodulation component. In this particular form of the $Q_3$, a hazard exists that the theory may over predict the first-second order interaction and swamp the third-first order ratio for a predictions of $IMD_3$. The
feedback theory presumes that the amplifier is large-signal biased at an operating point and has an impedance match tuning that has Power Gain. If this condition is not met, then the predictive value of the theory is lost because a device that is “off” does not have significant gain and hence its intermodulation distortion is not important.

**IV.4 Predictions of Linearity**

Using the modelling results of Chapter III: CMOS Modelling, as well the prior sections of this Chapter IV: Linearity, the following estimates of linearity are made per device geometry and bias.

As an example, Table IV.1 shows the predicted $III/3$ for the 50 $\mu$m x 0.35 $\mu$m FET. Table IV.2 shows the load matching impedance terms and harmonics of the load matching terms. Table IV.3 shows the source matching impedance terms and harmonics of the source matching terms.
### Table IV.2: N50µm x 0.35µm Load Terminating Impedances for Measured $III P_3$

| Term. Imped. | $|\Gamma_1|$ | $\angle \Gamma_1^0$ | $|\Gamma_2|$ | $\angle \Gamma_2^0$ | $|\Gamma_3|$ | $\angle \Gamma_3^0$ |
|--------------|-------------|-----------------|-------------|-----------------|-------------|-----------------|
| $T_L(1)$     | 0.647       | 258.6           | 0.815       | 239             | 0.806       | 64.8            |
| $T_L(2)$     | 0.647       | 258.6           | 0.815       | 239             | 0.806       | 64.8            |
| $T_L(3)$     | 0.28        | 256.4           | 0.466       | 180.4           | 0.484       | 322.6           |
| $T_L(4)$     | 0.685       | 217.6           | 0.849       | 166.5           | 0.878       | 323.7           |
| $T_L(5)$     | 0.320       | 314.3           | 0.801       | 3.3             | 0.822       | 251.3           |
| $T_L(6)$     | 0.632       | 314.3           | 0.801       | 3.3             | 0.822       | 251.3           |
| $T_L(7)$     | 0.563       | 85.8            | 0.810       | 281.7           | 0.841       | 310.7           |
| $T_L(8)$     | 0.653       | 154.3           | 0.853       | 51.9            | 0.839       | 149.7           |
| $T_L(9)$     | 0.559       | 341.8           | 0.751       | 60.3            | 0.783       | 332.0           |

### Table IV.3: N50µm x 0.35µm Source Terminating Impedances for Measured $III P_3$

| Term. Imped. | $|\Gamma_1|$ | $\angle \Gamma_1^0$ | $|\Gamma_2|$ | $\angle \Gamma_2^0$ | $|\Gamma_3|$ | $\angle \Gamma_3^0$ |
|--------------|-------------|-----------------|-------------|-----------------|-------------|-----------------|
| $T_S(1)$     | 0.465       | 199.6           | 0.704       | 31.6            | 0.733       | 280.6           |
| $T_S(2)$     | 0.688       | 178.1           | 0.867       | 11.6            | 0.881       | 262.2           |
| $T_S(3)$     | 0.668       | 178.1           | 0.867       | 11.6            | 0.881       | 262.2           |
| $T_S(4)$     | 0.410       | 231.7           | 0.639       | 90.4            | 0.648       | 7.7             |
| $T_S(5)$     | 0.410       | 231.7           | 0.639       | 90.4            | 0.648       | 7.7             |
| $T_S(6)$     | 0.660       | 146.3           | 0.864       | 310.5           | 0.894       | 175.5           |
| $T_S(7)$     | 0.335       | 195.8           | 0.561       | 12.8            | 0.609       | 247.0           |
| $T_S(8)$     | 0.335       | 195.8           | 0.561       | 12.8            | 0.609       | 247.0           |
| $T_S(9)$     | 0.495       | 179.0           | 0.751       | 60.3            | 0.778       | 228.7           |
Table IV.4: N130 x 0.35μm Theoretically Predicted $III P_3$ dBm at VDS=1.5V

<table>
<thead>
<tr>
<th>Term. Imped.</th>
<th>Vgs Bias</th>
<th>$III P_3$ Predicted</th>
<th>$I_{DS}$ mA</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{130}(1)$</td>
<td>1.5 V</td>
<td>18.0</td>
<td>21.8</td>
</tr>
<tr>
<td>$T_{130}(3)$</td>
<td>1.5 V</td>
<td>18.6</td>
<td>20.6</td>
</tr>
<tr>
<td>$T_{130}(6)$</td>
<td>1.5 V</td>
<td>15.6</td>
<td>22.0</td>
</tr>
<tr>
<td>$T_{130}(7)$</td>
<td>1.5 V</td>
<td>14.0</td>
<td>22.0</td>
</tr>
</tbody>
</table>

Table IV.5: N130μm x 0.35μm Load Terminating Impedances for Measured $III P_3$

| Term. Imped. | $|\Gamma_1|$ | $\angle \Gamma_1^0$ | $|\Gamma_2|$ | $\angle \Gamma_2^0$ | $|\Gamma_3|$ | $\angle \Gamma_3^0$ |
|--------------|-------------|---------------------|-------------|---------------------|-------------|---------------------|
| $T_L(1)$     | 0.717       | 231.8               | 0.846       | 203.5               | 0.846       | 16.4                |
| $T_L(3)$     | 0.392       | 111.1               | 0.714       | 331.3               | 0.741       | 331.3               |
| $T_L(6)$     | 0.717       | 231.8               | 0.846       | 203.5               | 0.846       | 16.4                |
| $T_L(7)$     | 0.717       | 231.8               | 0.846       | 203.5               | 0.846       | 16.4                |

Now for the N130μm x 0.35μm device the following predictions are made as shown in Table IV.4.

Where the following load and source terminating impedances of Tables IV.5 and IV.6 were used in the predictions of linearity in Table IV.4 as shown:

Now for the N200μm x 0.35μm device the following predictions are made

Table IV.6: N130μm x 0.35μm Source Terminating Impedances for Measured $III P_3$

| Term. Imped. | $|\Gamma_1|$ | $\angle \Gamma_1^0$ | $|\Gamma_2|$ | $\angle \Gamma_2^0$ | $|\Gamma_3|$ | $\angle \Gamma_3^0$ |
|--------------|-------------|---------------------|-------------|---------------------|-------------|---------------------|
| $T_S(1)$     | 0.020       | 291.7               | 0.063       | 287.3               | 0.114       | 151.8               |
| $T_S(3)$     | 0.020       | 291.7               | 0.063       | 287.3               | 0.114       | 151.8               |
| $T_S(6)$     | 0.557       | 141.0               | 0.805       | 290.2               | 0.839       | 143.2               |
| $T_S(7)$     | 0.556       | 184.1               | 0.799       | 10.9                | 0.830       | 255.9               |
Table IV.7: N200 x 0.35μm Theoretically Predicted $III_P^3$ dBmat VDS=1.5V

<table>
<thead>
<tr>
<th>Term. Imped.</th>
<th>Vgs Bias</th>
<th>$III_P^3$ Predicted</th>
<th>$I_{DS}$ mA</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{200}(2)$</td>
<td>1.5 V</td>
<td>17.1</td>
<td>25.0</td>
</tr>
<tr>
<td>$T_{200}(4)$</td>
<td>1.5 V</td>
<td>11.8</td>
<td>28.2</td>
</tr>
<tr>
<td>$T_{200}(6)$</td>
<td>1.5 V</td>
<td>11.8</td>
<td>28.9</td>
</tr>
</tbody>
</table>

Table IV.8: N200μm x 0.35μm Load Terminating Impedances for Measured $III_P^3$

| Term. Imped. | $|\Gamma_1|$ | $\angle\Gamma_1^0$ | $|\Gamma_2|$ | $\angle\Gamma_2^0$ | $|\Gamma_3|$ | $\angle\Gamma_3^0$ |
|--------------|------------|-------------------|------------|-------------------|------------|-------------------|
| $T_L(2)$     | 0.458      | 50.1              | 0.758      | 206.4             | 0.758      | 193.2             |
| $T_L(4)$     | 0.719      | 274.3             | 0.851      | 305.0             | 0.860      | 168.8             |
| $T_L(6)$     | 0.719      | 274.3             | 0.851      | 305.0             | 0.860      | 168.8             |

as shown in Table IV.7.

Where the following load and source terminating impedances of Tables IV.8 and IV.9 were used in the predictions of linearity in Table IV.7 as shown:

Table IV.9: N200μm x 0.35μm Source Terminating Impedances for Measured $III_P^3$

| Term. Imped. | $|\Gamma_1|$ | $\angle\Gamma_1^0$ | $|\Gamma_2|$ | $\angle\Gamma_2^0$ | $|\Gamma_3|$ | $\angle\Gamma_3^0$ |
|--------------|------------|-------------------|------------|-------------------|------------|-------------------|
| $T_S(2)$     | 0.020      | 291.7             | 0.063      | 287.3             | 0.114      | 151.8             |
| $T_S(4)$     | 0.020      | 291.7             | 0.063      | 287.3             | 0.114      | 151.8             |
| $T_S(6)$     | 0.601      | 230.8             | 0.822      | 108.2             | 0.834      | 44.4              |
Table IV.10: Test Transistor Geometry

<table>
<thead>
<tr>
<th>Device</th>
<th>Gate Finger Width in μm</th>
<th>Number of Fingers</th>
</tr>
</thead>
<tbody>
<tr>
<td>N50</td>
<td>5</td>
<td>10</td>
</tr>
<tr>
<td>N200</td>
<td>20</td>
<td>10</td>
</tr>
<tr>
<td>N130</td>
<td>5</td>
<td>26</td>
</tr>
<tr>
<td>N520</td>
<td>20</td>
<td>26</td>
</tr>
</tbody>
</table>

IV.5 MOSFET Design of Experiment

A DOE, III, is created in part from test transistors listed in Table VIII.2 to determine the effectiveness of the linearity theory on microwave CMOS FET’s. The transistor set of DOE III make up a design of experiment over geometry by varying gate width and finger number. One common-gate design is included.

IV.6 Summary

The nonlinear performance of a grounded-source CMOS amplifier operating in the 5 GHz region has been analyzed and the predicted using a Volterra series analysis. Predictions have been made over a broad range of currents, device geometries, and source and load impedances. Although algebraically complex, this technique allows the user to identify the key limiting features of the nonlinear operation of CMOS amplifiers operating in strong inversion, and pick the appropriate bias and terminating impedances to achieve the best performance.

The effects of variations in the load impedance at the fundamental and harmonic frequencies (2ω, 3ω) on $I_{III}P_3$ can be seen from examination of IV.65.
The numerator contains a sum of the third-order transconductance term ($a_3$), the third-order output impedance terms ($g_3, c_3$), amongst others, and the permutation of the second-order and first-order responses ($H_1$ and $H_2$). The sum of these terms are altered by the magnitude and phase of the termination impedance at the output and its second-harmonic frequency termination. Variations in phase at that frequency and its harmonic can affect the $\text{IIIP}_3$. Similarly, the magnitude and phase of the output terminating impedance at $3\omega$ can affect the $\text{IIIP}_3$. Through the $C_{gd}$ feedback and interaction with the second- or third-order nonlinearity at the input the $\text{IIIP}_3$ can also vary. The result is that the $\text{IIIP}_3$ is a complex function of the output and input terminating impedances at fundamental and harmonic frequencies of $2\omega$ and $3\omega$ [33]. This interaction between output and input nonlinearity is qualitatively different from the bipolar transistor case, where the output impedance network is highly linear, and the $C_{be}$ is smaller.

Experimental results described in Chapter IX will verify the utility of the theoretical predictions contain in this chapter.

The text of this chapter, in part, is a reprint of the material as it appears in our published papers in IEEE Conferences [SiRF03, Germany; IEDM99, USA] and in preparation for Conferences and Transactions on Microwave Theory and Techniques. The dissertation author was the primary investigator and primary and secondary author of these papers.
Chapter V

Noise Analysis of CMOS FET’s

V.1 Introduction

In this Section, an improved expression for the minimum Noise Figure and $\Gamma_{opt}$ are derived for the MOSFET, and compared to experimental results. In the previous work, Noise Figure predictions have been obtained for the MOSFET including the circuit contributions, induced gate noise, correlated and uncorrelated, and the drain current but excluding the gate resistance and feedback [34–36]. Later work has included the gate and substrate resistances [37] but still lacks the Noise Figure predictions including feedback based on $C_{gd}$ [6, 25, 38, 39]. Additional work has suggested that shot noise through thin oxide could also contribute to the Noise Figure [39]. For these devices, the gate oxide is sufficiently thick, 7 nm, to significantly reduce a Fowler-Nordheim Tunneling contribution under the power-constrained biases. The new expression for the minimum Noise Figure and $\Gamma_{opt}$ will include both gate and substrate resistances and $C_{gd}$ feedback. The Noise
Figure V.1: Two-Port Noise Model

Figure and $\Gamma_{opt}$ predictions are then compared to measured devices.

V.2 Noise Figure Analysis

The small-signal equivalent noise sources in the MOSFET, can be placed at the input of the MOSFET with a noiseless amplifier and load following, as seen in Fig. V.1 [22]. A more detailed noise model is considered in Fig. V.2. Along with the drain noise current, two gate noise currents are also induced, one correlated with the drain, the other uncorrelated. Finally the polysilicon gate and substrate resistances appear separately. The Noise Factor for an amplifier is defined as

$$F = \frac{Total\ Input\ Noise}{Total\ Input\ Noise\ due\ to\ the\ Source} \quad (V.1)$$

The Noise Factor can then be specified in terms of currents where $i_{nt}$ is the total input noise current from all sources and $i_{ns}$ is the input noise current due to the

$$F = \frac{i_{nt}^2}{i_{ns}^2} \quad (V.2)$$
source admittance only. The current is given by

\[ i_{nt} = i_{ns} + i_{gr} + i_{sub} + i_{g} + i_{in} + Y_s e_n \]  

(V.3)

where \( i_{ns} \) is the source noise current, \( i_{gr} \) is the noise current due to the polysilicon gate resistance, \( i_{sub} \) is the input current due to the substrate resistance, \( i_{g} \), is the gate noise current, \( i_{in} \), is the equivalent input noise current due to the drain, \( Y_s \), is the source admittance, and \( e_n \), is the equivalent input noise voltage due to the drain.

The noise power is proportional to the mean square of the noise current. So,

\[
\overline{i_{nt}^2} = (i_s + i_{gr} + i_{sub} + i_{g} + i_{in} + Y_s e_n)^2 = i_s^2 + i_{gr}^2 + i_{sub}^2 + (i_g + i_{in} + Y_s e_n)^2
\]  

(V.4)

where \( i_{gr} = 4kTY_{gr} \Delta f \) and \( Y_{gr} = \omega^2 C_{gs}^2 R_g \). Separation of the noise power terms can be made because the first three terms on the right are uncorrelated to the

Figure V.2: MOSFET Equivalent Circuit Noise Model
others. Now, the gate noise current, \( i_g \), is composed of two terms, both induced by the drain current; one is correlated with the drain current, and the other is not correlated.

\[
i_g = i_{gnc} + i_{gc}
\]  

(V.5)

The correlated gate current can be expressed in terms of the correlation admittance, \( Y_c \) as follows:

\[
i_c = Y_c e_n
\]  

(V.6)

where \( Y_c \) is defined as

\[
Y_c \equiv G_c + jB_c = \frac{i_c}{e_n} = \frac{i cg_m}{i_{nd}}
\]  

(V.7)

where \( i_c = i_{in} + i_{gc} \) and \( g_m \) is the gate transconductance. The drain current noise is defined as [10]

\[
\overline{i_{nd}^2} = 4kTg_{do}\gamma \Delta f
\]  

(V.8)

where \( k \) is the Boltzmann constant which equals \( 1.38 \times 10^{-23} \text{ J/} ^\circ \text{K} \), \( T \) is the absolute temperature in degrees Kelvin, \( \Delta f \) is the noise bandwidth usually taken at 1 Hz, and \( g_{do} \) is the drain conductance defined as

\[
g_{do} = \left. \frac{\partial I_d}{\partial V_{ds}} \right|_{V_{ds}=0}
\]  

(V.9)

From the drain current noise, the equivalent gate noise, \( e_n \), can be defined as

\[
\overline{e_n^2} = \frac{4kTg_{do}\gamma \Delta f}{g_m^2} = \frac{\overline{i_{nd}^2}}{g_m^2}
\]  

(V.10)
which represents the reflected drain current in the gate. The quantity $\gamma$, represents the increased thermal noise over long-channel devices from the hot-electron effect, which arises from the short-channel geometry under high field [34]. The value of $\gamma$ is discussed in more detail in Section V.4.1.

The amount of correlation between the induced gate noise arising from the drain noise is described by the quantity, $c$ [34].

$$c = \frac{\overline{\overline{i_{ng}i_{nd}}}^2}{\left(\overline{i_{ng}i_{ng}} \cdot \overline{i_{nd}i_{nd}}\right)^{1/2}}$$ \hspace{1cm} (V.11)

The three quantities that define $c$ are the cross-correlation gate induced drain-driven current integral, and the normalized drain and gate integrals. The correlation $|c|$ is taken at 0.395 [34].

The gate noise can be defined in terms of $c$ as

$$\frac{\overline{i_g^2}}{4kT\delta f} = g_g(1 - |c|^2) + g_g|c|^2$$ \hspace{1cm} (V.12)

where $g_g$ is the gate conductance defined as [34]

$$g_g = \frac{\omega^2 C_{gs}^2}{5g_{do}}$$ \hspace{1cm} (V.13)

The quantity, $\delta$, represents the increase in gate induced noise capacitively coupled from the channel under a rapidly varying potential [25]. The value of $\gamma$ is discussed in more detail in Section V.4.1.

Returning to the correlation admittance, based on the above definitions, it has been shown [25] that

$$Y_c = \frac{i_{in} + i_{gc}}{e_n} = j\omega C_{gs} + \frac{i_{gc}}{e_n} = j\omega C_{gs} + g_m \frac{i_{gc}}{i_{nd}}$$ \hspace{1cm} (V.14)
where \( i_{in} \) is the equivalent input noise current and \( i_{gc} \) is induced correlated gate noise current. The last term above can be multiplied by drain and gate noise currents to produce \( c \), the correlation coefficient previously defined.

\[
g_{m} \frac{i_{gc}}{i_{nd}} = g_{m} \frac{\frac{1}{2} i_{nd}^{*} t_{nd}}{i_{nd}^{*} \cdot i_{nd}} = g_{m} \frac{\frac{1}{2} i_{nd}^{*}}{i_{nd}^{*} \cdot i_{nd}} = g_{m} - \frac{i_{g}^{*}}{i_{nd}^{*} \cdot i_{nd}^{*}} \sqrt{\frac{\gamma}{\chi_{nd}}} \sqrt{\frac{\gamma}{\chi_{ng}}} \quad \text{(V.15)}
\]

which can be reduced to

\[
g_{m} \frac{i_{gc}}{i_{nd}} = g_{m} - \sqrt{\frac{\gamma}{\chi_{nd}}} \sqrt{\frac{\gamma}{\chi_{ng}}} = g_{m}c \sqrt{\frac{\gamma}{\chi_{nd}}} \quad \text{(V.16)}
\]

Upon, substituting in V.8 and V.10, and reducing, the correlation admittance is given finally by

\[
Y_{c} = j\omega C_{gs} + j\omega C_{gs} \frac{g_{m} c}{g_{do}} |c| \sqrt{\frac{\delta}{5\gamma}} \quad \text{(V.17)}
\]

where, \( \alpha \), defines the ratio of gate transconductance to drain conductance, \( g_{m} v / g_{do} \), and equals approximately 0.85. The uncorrelated conductance is shown as

\[
G_{u} = \frac{\gamma_{2}}{4kT\Delta f} = \frac{\delta \omega^{2} C_{gs}^{2} (1 - |c|^{2})}{5g_{do}} \quad \text{(V.18)}
\]

The correlated susceptibility is identified based on the above

\[
B_{c} = \omega C_{gs} (1 + \alpha |c| \sqrt{\frac{\delta}{5\gamma}}) \quad \text{(V.19)}
\]

Collecting appropriate terms allows the Noise Factor to be completely expressed as follows

\[
F = 1 + \frac{R_{gr}}{R_{s}} + \frac{G_{u}}{G_{s}} + \frac{R_{n}}{G_{s}} [(G_{s} + G_{c})^{2} + (B_{s} + B_{c})^{2}] \quad \text{(V.20)}
\]
where $R_n$ is defined as

$$R_n = \frac{e^2}{4kT \Delta f} = \frac{g_{do} \gamma}{g_{in}}$$  \hspace{1cm} (V.21)

To minimize the Noise Factor expression, $B_s$ is set to $-B_c$. The expression is then differentiated with respect to $G_s$ and set to zero [14]. The result is that $G_s$ and $B_s$ are as follows

$$G_{opt} = G_s = \sqrt{G_c^2 + \frac{G_u}{R_n}}$$  \hspace{1cm} (V.22)

and

$$B_{opt} = B_s = -B_c$$  \hspace{1cm} (V.23)

$y_{opt}$ is defined as follows where $Y_o$ is 20mS:

$$y_{opt} = \frac{G_{opt} + jB_{opt}}{Y_o}$$  \hspace{1cm} (V.24)

where $y_{opt}$ is the normalized admittance. $\Gamma_{opt}$ is calculated as shown in [22].

$$\Gamma_{opt} = \frac{1 - y_{opt}}{1 + y_{opt}}$$  \hspace{1cm} (V.25)

The minimum Noise Factor can then be expressed as

$$F_{min} = 1 + \frac{R_{gr}}{R_s} + \frac{R_{sub}}{R_s} + 2R_n(G_{opt})$$  \hspace{1cm} (V.26)

Since no thermal component is taken in $G_{opt}$, $G_c$ is zero.

**V.3 Minimum Noise Figure with Feedback**

In developing the modification to the above results for a two-port network including lossless feedback, two observations are important. First, the feedback is
entirely reactive and thus adds no noise to the minimum Noise Figure. Second, the feedback is a single element, which means the modification to include feedback, can be made more simply than the general feedback case [40]. In modifying the two-port case of Fig. V.1 to include feedback, the single element shunt model is chosen because it completes the modelling of the grounded-source amplifier. The generalized shunt feedback Noise Figure for a two-port is as follows [40]:

\[
\begin{align*}
F_{S,H}^f &= F_{\text{min}} + \frac{R_n}{G_s} |Y_s - Y_{opt}|^2 - 1 + \frac{R_n}{G_s} \times \left\{ |\psi_1|^2 + 2\text{Re} \left[ \left( \frac{F_{\text{min}} - 1}{2R_n} - Y_{opt}^* \right) \times (\psi_1 - Y_s) \right] - |Y_s|^2 \right\} + \\
&\quad \left( F_{\text{min}} + \hat{R}_n \right) \left| Y_s - \hat{Y}_{opt} \right|^2 + \hat{R}_n \times \left\{ |\psi_2|^2 + 2\text{Re} \left[ \left( \frac{F_{\text{min}} - 1}{2R_n} - \hat{Y}_{opt}^* \right) \times (\psi_2 - Y_s) \right] - |Y_s|^2 \right\}.
\end{align*}
\]

(V.27)

Fortunately, a great simplification can be made for a single element shunt feedback as shown:

\[
\begin{align*}
F_{S,H}^f &= F_{\text{min}} + \frac{R_n}{G_s} |Y_s - Y_{opt}|^2 + \frac{R_n}{G_s} \times \left\{ |\psi_1|^2 + 2\text{Re} \left[ \left( \frac{F_{\text{min}} - 1}{2R_n} - Y_{opt}^* \right) \times (\psi_1 - Y_s) \right] - |Y_s|^2 \right\}.
\end{align*}
\]

(V.28)

\(\psi_1\) is defined as follows:

\[
\psi_1 = E_1 + Y_s D_1
\]

(V.29)
where $E_1$ and $D_1$ are defined as

$$E_1 = Y_f \frac{y_{21} + y_{11}}{y_{21} + Y_f} \quad \text{(V.30)}$$

$$D_1 = \frac{y_{21}}{y_{21} - Y_f} \quad \text{(V.31)}$$

The $Y_f$ term is the admittance of $C_{gd}$ and equals $jwC_{gd}$, the feedback term. The next step on the way to a solution is the differentiation of V.28 with respect to $G_s$ and the setting of its derivative to zero to find the minimum.

$$\frac{\partial F_{\text{SHUNT}}}{\partial G_s} = -\frac{R_n}{G_s^2} \left\{ (G_s - G_{\text{opt}})^2 + (B_s - B_{\text{opt}})^2 + |\psi_1|^2 \right\}$$

$$+ \frac{2R_n}{G_s} \left\{ (G_s - G_{\text{opt}}) + D_1 + \left( \frac{F_{\text{min}} - 1}{2R_n} - G_{\text{opt}} \right) \Re (D_1) - G_s \right\} = 0$$

\text{(V.32)}

Since the solution results in a dual quadratic in $G_{\text{opt}}$ and $B_{\text{opt}}$, only relative scaling can be determined while maintaining algebraic equality in V.33.

$$G_{\text{opt}}^2 - 2 \left( G_s + \Re (\psi_1 - Y_s) \right) G_{\text{opt}} - 3G_s^2 + \frac{F_{\text{min}} - 1}{2R_n} G_s + B_{\text{opt}}^2$$

$$- 2 \left( B_s - \Im (\psi_1 - Y_s) \right) B_{\text{opt}} + |\psi_1|^2 + \frac{F_{\text{min}} - 1}{R_n} \Re (\psi_1 - Y_s) = 0$$

\text{(V.33)}

With V.33, it is possible to scale the no-feedback theoretical predictions for $G_{\text{opt}}$ and $B_{\text{opt}}$ so that the effects of feedback can be observed on $\Gamma_{\text{opt}}$. 
V.4 Minimum Noise Figure Predictions without and with Feedback

V.4.1 Noise Theory Predictions without feedback

Table V.1 shows the results calculated from the above Noise Figure theory by size and bias without feedback via $C_{gd}$. Upon substituting the parameters from above, the theoretical predictions are be found, listed in Table V.1. At high field $\gamma$ is taken at 2.0 in saturation and 1.5 near triode [25]. At high field, $\delta$ is taken at 4.0 in saturation and 3.0 near triode [25]. These quantities are higher than derived in the long channel case to accommodate short channel behavior including impact ionization and hot carrier effects. The substrate resistance is taken from S-parameters and earlier work [41]. The gate resistance is based on physical process data and earlier work [37].

V.4.2 Noise Theory Predictions with feedback

The change in $\Gamma_{opt}$ is shown below in Table V.2.

Upon inspection of Table V.2, $\Gamma_{opt}$ is seen to shorten in radius slightly and double in angle approximately with feedback when compared to theoretical predictions based on no feedback.
Table V.1: Noise Theory Predictions at 5 GHz with $\Gamma_{opt}$ and without Feedback

<table>
<thead>
<tr>
<th>Parameter</th>
<th>N200</th>
<th>N200</th>
<th>N50</th>
<th>N50</th>
<th>N130</th>
<th>N130</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{ds}(V)$</td>
<td>1.5</td>
<td>1.5</td>
<td>1.5</td>
<td>1.5</td>
<td>1.5</td>
<td>1.5</td>
</tr>
<tr>
<td>$V_{gs}(V)$</td>
<td>1.5</td>
<td>1.0</td>
<td>1.5</td>
<td>1.0</td>
<td>1.5</td>
<td>1.0</td>
</tr>
<tr>
<td>$I_{ds}(mA)$</td>
<td>28.0</td>
<td>17.0</td>
<td>9.8</td>
<td>6.0</td>
<td>28.0</td>
<td>10.0</td>
</tr>
<tr>
<td>$R_g(\Omega)$</td>
<td>5.7</td>
<td>5.7</td>
<td>1.4</td>
<td>1.4</td>
<td>0.6</td>
<td>0.6</td>
</tr>
<tr>
<td>$R_{sub}(\Omega)$</td>
<td>14.0</td>
<td>14.0</td>
<td>9.0</td>
<td>9.0</td>
<td>3.0</td>
<td>3.0</td>
</tr>
<tr>
<td>$C_{gs}(fF)$</td>
<td>206.7</td>
<td>194.0</td>
<td>44.6</td>
<td>51.0</td>
<td>103.0</td>
<td>104.0</td>
</tr>
<tr>
<td>$g_m(mS)$</td>
<td>63.0</td>
<td>51.0</td>
<td>14.0</td>
<td>11.0</td>
<td>36.0</td>
<td>30.0</td>
</tr>
<tr>
<td>$F$</td>
<td>1.68</td>
<td>1.64</td>
<td>1.48</td>
<td>1.51</td>
<td>1.32</td>
<td>1.29</td>
</tr>
<tr>
<td>$NF(dB)$</td>
<td>2.25</td>
<td>2.15</td>
<td>1.71</td>
<td>1.78</td>
<td>1.19</td>
<td>1.12</td>
</tr>
<tr>
<td>$G_{opt}(mS)$</td>
<td>10.0</td>
<td>6.0</td>
<td>2.0</td>
<td>2.0</td>
<td>5.0</td>
<td>3.0</td>
</tr>
<tr>
<td>$B_{opt}(mS)$</td>
<td>-8.0</td>
<td>-7.0</td>
<td>-2.0</td>
<td>-2.0</td>
<td>-4.0</td>
<td>-4.0</td>
</tr>
<tr>
<td>$r(\Gamma_{opt})$</td>
<td>0.4</td>
<td>0.6</td>
<td>0.8</td>
<td>0.8</td>
<td>0.6</td>
<td>0.7</td>
</tr>
<tr>
<td>$\theta(\Gamma_{opt})$</td>
<td>52.1</td>
<td>43.7</td>
<td>9.8</td>
<td>11.2</td>
<td>23.5</td>
<td>23.0</td>
</tr>
</tbody>
</table>

Table V.2: Two-Port Noise Figure Predictions at 5.0 GHz with $\Gamma_{opt}$ and Feedback.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>N200</th>
<th>N200</th>
<th>N50</th>
<th>N50</th>
<th>N130</th>
<th>N130</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{ds}(V)$</td>
<td>1.5</td>
<td>1.5</td>
<td>1.5</td>
<td>1.5</td>
<td>1.5</td>
<td>1.5</td>
</tr>
<tr>
<td>$V_{gs}(V)$</td>
<td>1.5</td>
<td>1.0</td>
<td>1.5</td>
<td>1.0</td>
<td>1.5</td>
<td>1.0</td>
</tr>
<tr>
<td>$I_{ds}(mA)$</td>
<td>28.0</td>
<td>17.0</td>
<td>9.8</td>
<td>6.0</td>
<td>28.0</td>
<td>10.0</td>
</tr>
<tr>
<td>$R_g(\Omega)$</td>
<td>5.7</td>
<td>5.7</td>
<td>1.4</td>
<td>1.4</td>
<td>0.6</td>
<td>0.6</td>
</tr>
<tr>
<td>$R_{sub}(\Omega)$</td>
<td>14.0</td>
<td>14.0</td>
<td>9.0</td>
<td>9.0</td>
<td>3.0</td>
<td>3.0</td>
</tr>
<tr>
<td>$C_{gs}(fF)$</td>
<td>206.7</td>
<td>194.0</td>
<td>44.6</td>
<td>51.0</td>
<td>103.0</td>
<td>104.0</td>
</tr>
<tr>
<td>$g_m(mS)$</td>
<td>63.0</td>
<td>51.0</td>
<td>14.0</td>
<td>11.0</td>
<td>36.0</td>
<td>30.0</td>
</tr>
<tr>
<td>$F$</td>
<td>1.68</td>
<td>1.64</td>
<td>1.48</td>
<td>1.51</td>
<td>1.32</td>
<td>1.29</td>
</tr>
<tr>
<td>$NF(dB)$</td>
<td>2.25</td>
<td>2.15</td>
<td>1.71</td>
<td>1.78</td>
<td>1.19</td>
<td>1.12</td>
</tr>
<tr>
<td>$G_{opt}(mS)$</td>
<td>3.2</td>
<td>3.0</td>
<td>0.69</td>
<td>0.79</td>
<td>1.6</td>
<td>1.62</td>
</tr>
<tr>
<td>$B_{opt}(mS)$</td>
<td>-7.9</td>
<td>-7.4</td>
<td>-1.7</td>
<td>-1.9</td>
<td>-3.9</td>
<td>-4.0</td>
</tr>
<tr>
<td>$r(\Gamma_{opt})$</td>
<td>0.76</td>
<td>0.77</td>
<td>0.93</td>
<td>0.93</td>
<td>0.86</td>
<td>0.86</td>
</tr>
<tr>
<td>$\theta(\Gamma_{opt})$</td>
<td>43.9</td>
<td>41.3</td>
<td>9.7</td>
<td>11.1</td>
<td>22.4</td>
<td>22.6</td>
</tr>
<tr>
<td>$C_{gd}(fF)$</td>
<td>95.0</td>
<td>78.4</td>
<td>23.0</td>
<td>18.6</td>
<td>64.0</td>
<td>48.0</td>
</tr>
<tr>
<td>$r(\Gamma_{opt})(fb)$</td>
<td>0.69</td>
<td>0.72</td>
<td>0.88</td>
<td>0.83</td>
<td>0.79</td>
<td>0.77</td>
</tr>
<tr>
<td>$\theta(\Gamma_{opt})(fb)$</td>
<td>69.7</td>
<td>56.4</td>
<td>18.4</td>
<td>27.8</td>
<td>35.4</td>
<td>40.0</td>
</tr>
</tbody>
</table>
V.5 Summary

A small-signal noise model has been developed for 5 GHz CMOS grounded-source amplifier and used to predict the minimum Noise Figure and $\Gamma_{\text{opt}}$ along with other noise model parameters. The minimum Noise Figure is predicted to be 1 to 2 dB at 5.0 GHz across device geometry.

The trends in minimum Noise Figure are followed by gate design; that is, gate width design correlates to Noise Figure. So, in comparing the N50 with N130 transistor, the N130 transistor has lower Noise Figure in part because it has a greater number of the same parallel gate widths than the N50 transistor of the same design. In comparing the N200 transistor with the N50 transistor, the minimum Noise Figure is lower on the N50 than on the N200 because the N50 has a narrower gate width than the N200, even though both have the same number of gate width branches.

It is seen that an increase in capacitance in the device model at the input to the amplifier from the feedback will require an increase in inductance to reactively match the same condition for minimum Noise Figure. In other words, a further upwards rotation of the matching phasor in $\Gamma_{\text{opt}}$ is expected from a non-feedback minimum Noise Figure prediction. This expected trend in $\Gamma_{\text{opt}}$ was observed in the predictions as the capacitance increased at the gate by device geometry from N50 to N130.

These predictions will be compared and verified via measurements dis-
Figure V.3: Smith Chart Showing Noise and Available Gain Circles

cussed in Chapter IX: Experimental Verification of Theory. An example Smith chart with NF and Available Power Gain circles is shown in Fig.V.3. The blue circles are NF and the red are Gain. The green circle is stability.

The text of this chapter, in part, is a reprint of the material as it will appears in our papers in *IEEE Transactions on Microwave Theory and Techniques, Solid-State Circuits, or Electron Devices*. The dissertation author was the primary investigator and primary author of this paper.
Chapter VI

Optimum Design for CMOS RF Amplifiers

VI.1 Introduction to Optimum RF Design Techniques

RF/analog design is based on linear amplifiers, for which grounded-source amplifiers are widely used. Thus, determining methods of predicting the optimum design for RF/analog amplifiers, under the constraint of minimum power dissipation, is a very utilitarian goal. To this purpose so far, the third-order input intermodulation intercept point $III_P^3$ in Chapter IV and Noise Figure in Chapter V of the grounded-source amplifier have been analyzed and predicted, demonstrating the applicability of CMOS for super high frequency (5.0 GHz) RF applications. An implicit design condition for RF circuits in the above analyses is the impedance match [42]. An impedance match has been included as an element in the prior theory of linearity, Chapter IV, and minimum Noise Figure, Chapter V, for the CMOS grounded-source amplifier.
In consideration of other RF design attributes; namely, power Gain, VSWR, stability, impedance matching or tuning also plays a very large role. Of these RF design attributes, stability and power consumption also set a boundary on the type of matching available to achieve optima in the other RF amplifier design attributes.

We next predict the stability and power Gain, Minimum Detectable Signal, MDS, and Spur-Free Dynamic Range, SFDR, as a function Linearity, Noise Figure, Bandwidth, and power consumption are developed and predicted in obtaining optimum CMOS RF amplifier design. With the above definitions of optimum amplifier design developed, the relationship with termination matching impedances to key system parameter requirements, such as signal-to-noise, S/N, developed in Chapter I: Introduction and System Architecture, and SFDR, can be understood in terms of RF/analog circuit design requirements.

VI.2 Optimizing CMOS Amplifier Stability

Stability of an amplifier design can be determined by calculating the K and Δ factors in VI.1 and VI.2 based on scattering parameters, S-parameters [22].

\[
K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \quad \text{(VI.1)}
\]

\[
\Delta = S_{11}S_{22} - S_{12}S_{21} \quad \text{(VI.2)}
\]

For the conditions where \( K > 1 \) and \( \Delta < 1 \), the amplifier is unconditionally stable and the stability circles will not cross the Smith chart boundary. For MOS-
FET’s unconditional stability is rare; thus, matching for MOSFET’s frequently involves marginally stability, where \( K < 1 \) or \( \Delta > 1 \), [22].

To begin the matching process, the radius and center of the stability circle for the amplifier input or output relative to the Smith chart must be calculated, for the load side this is defined in VI.3 and VI.4 [22].

\[
\begin{align*}
  r_L &= \frac{|S_{12}S_{21}|}{|S_{22}|^2 - |\Delta|^2} \quad \text{(VI.3)} \\
  C_L &= \frac{(S_{22} - \Delta S_{11}^*)^*}{|S_{22}|^2 - |\Delta|^2} \quad \text{(VI.4)}
\end{align*}
\]

where \( r_L \) is the radius and \( C_L \) is the center load-side stability circle.

For the source side the above definitions change to what is shown in VI.5 and VI.6 [22].

\[
\begin{align*}
  r_S &= \frac{|S_{12}S_{21}|}{|S_{11}|^2 - |\Delta|^2} \quad \text{(VI.5)} \\
  C_S &= \frac{(S_{11} - \Delta S_{22}^*)^*}{|S_{11}|^2 - |\Delta|^2} \quad \text{(VI.6)}
\end{align*}
\]

where \( r_S \) is the radius and \( C_S \) is the center source-side stability circle.

For a marginally stable input or output, matching for any other RF attribute must be chosen so as not to produce instability in the amplifier, which would then lead to oscillation.
VI.3 Optimization of Impedance Termination Matching for CMOS Amplifiers

Having predicted and examined the stability of the RF CMOS grounded-source amplifier, the reflection coefficients at the input and output reference planes are developed for further use in optimizing and predicting RF CMOS design.

VI.3.1 Optimum Source Matching of CMOS Amplifiers

Beginning with the input side of the amplifier chain, source reflection coefficient, $\Gamma_s$, is a function of the input tuner position and in general is a complex solution to a quasi-TEM resonant cavity. For any given position of the input tuner the equivalent $R+jX$ value is known, thus source impedance can be found from the definition in VI.7, [21, 22, 43].

$$\Gamma_s = \frac{Z_s - Z_0}{Z_s + Z_0}$$

(VI.7)

where $Z_s$ is the source impedance and $Z_0$ is the characteristic line impedance, often 50 $\Omega$.

The Input Gamma, $\Gamma_{IN}$, is a function of the input impedance of the MOS-FET, which is based on $C_{gd}$, $C_{gs}$, $R_g$, and $g_m$ and is calculated using, measured S-parameters from Table VI.1 as seen in VI.8 [22, 43].

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L}$$

(VI.8)
Examining the Source-Pull Figs. VI.1, and VI.2 stability circles at two biases are present, $V_{GS} = 1.0V$ and $V_{GS} = 1.5V$, as well as $\Gamma_s$ and $\Gamma_{in}$, at two biases. Now, both the stability circles and the $\Gamma$'s are calculated based on the equations given VI.8, VI.7, VI.5, and VI.6. The equations in turn are based on S-parameters displayed in VI.1 and acquired with a Vector Network Analyzer (VNA), described in Sections III.3.2 and VIII.4.1. S-parameters of a device or circuit under test vary with the operating bias applied, the RF power applied, and the tuning used. The results shown in Figs. VI.2 and VI.1 have been constructed in the manner described. When source and load are matched several condition are obtained: Maximum power is delivered with power loss minimized, Signal-to-noise is improved, Amplitude and phase errors are reduced. Optimizing all of these goals simultaneously is not necessary in every design situation or even obtainable but they should be kept in consideration.

For a source and load to be matched, the reactive parts of the complex impedance should be of opposite sign. Now, this is a challenge at high frequency because source and load impedances are both complex; that is, they have a real and imaginary components which are difficult to precisely control and vary with bias, frequency, power level, as well as the match. In the current situation of Figs. VI.1, and VI.2 $\Gamma_s$ is not conjugately matched with the $\Gamma_{in}$. The power level of the high-frequency S-parameter measurement is quite low, about $P_{rf,i} = -25dBm$, and with no reflection control or tuning. S-parameters are a function of RF power
level, device bias, frequency, and tuning. In the current case, only frequency and
device dc bias are controlled. It should be the case that the $\Gamma_s$ is from a measure-
ment that is under similar conditions as those used to determine $\Gamma_{in}$. However at
the time of these measurements for $\Gamma_{in}$, the S-parameters available could not be
obtained under conditions similar to the conditions $\Gamma_s$ was obtained. The condi-
tions for $\Gamma_s$ are those of controlled tuning and RF power levels of -10 dBm to 0
dBM, and the conditions for $\Gamma_{in}$ were RF power levels of -25 dBm and below with
no tuning. Therefore, it is reasonable that the conjugate match line up of $\Gamma_{in}$ is
not as close to $\Gamma_s$ as would be desired because of a measurement limitation in the
case of $\Gamma_{in}$.

The $\Gamma_s$ is based on a location where the Power Gain is high and at different
RF power and tuning conditions from those under which the S-parameters were
measured for $\Gamma_{in}$. At the time of the S-parameter measure no higher RF power
measurement was possible to match the conditions of the other RF measurements,
such as Power Gain. Should these last two issues, power level and reflection
control, be corrected, the $\Gamma_s$ and $\Gamma_{in}$ might be better positioned on the Source-pull
Smith chart. But given the deficiencies of the measurement, it is hard to drawn
much more from it other than as an example of the calculation of $\Gamma_s$ and $\Gamma_{in}$
for the different MOSFET’s under the different measurement conditions available
[21, 25].

Because these are marginally stable amplifiers, choices for tuning must be
Figure VI.1: Measured and Modelled N50μm x 0.35μm Source-Pull $\Gamma_{IN}$ vs. $\Gamma_S$ at $V_{ds}=1.5V$ and Freq.=5.0 GHz with Stability Circles.
Figure VI.2: Measured and Modelled N200μm x 0.35μm Source-Pull $\Gamma_{IN}$ vs. $\Gamma_S$ at $V_{ds}=1.5V$ and Freq.=5.0 GHz and with Stability Circles.
restricted to achieve stability and maximum power Gain simultaneously but the choices may not be conjugate matches for maximum power Gain as defined in Section VI.4.

Next, the stability of the twenty-six fingered N130μm x 0.35μm, as a function of current density, can be seen in Fig. VI.3, where the N130μm x 0.35μm is seen to be also a marginally stable amplifier.

In summary, the source side matching, for the CMOS transistors described above, shows that achieving maximum power Gain using a conjugate match might make the amplifier unstable. Also, the Γ’s from above are based on low RF power S-parameters. Γ’s at higher RF power levels may well be different than those shown in Figs. VI.2, VI.3, and VI.1. Thus, while these examples are not the most desirable, the conclusion is still that matching must be made to ensure stability before other RF design attributes are optimized.

VI.3.2 Load Side Matching

Next looking at the output side of the amplifier chain, the Load Gamma, Γ, is a function of the output tuner position and in general is also a complex solution to a quasi-TEM resonant cavity. For any given position of the output tuner, the equivalent R+jX value is known, thus load impedance can be found from the definition in VI.9 [22].
Figure VI.3: Measured and Modelled N130 Source-Pull $\Gamma_{IN}$ vs. $\Gamma_S$ at $V_{ds}=1.5V$ and Freq.=5.0 GHz with Stability Circles.
\[ \Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0} \]  \hspace{1cm} (VI.9)

where \( Z_L \) is the load impedance and \( Z_0 \) is the characteristic line impedance, often \( 50 \, \Omega \).

The output Gamma, \( \Gamma_{out} \), is a function of the output impedance of the MOSFET, which is based on \( g_m \), \( C_{gd} \), \( C_{ds} \), \( C_{db} \), \( r_o \), and \( \Gamma_S \) and is calculated using, measured S-parameters in VI.10 [22].

\[ \Gamma_{out} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \]  \hspace{1cm} (VI.10)

Turning to Figs. VI.4, and VI.5 for the N50\( \mu \)m x 0.35\( \mu \)m and N200\( \mu \)m x 0.35\( \mu \)m transistor amplifiers respectively, both ten-fingered gate amplifiers, the N200\( \mu \)m x 0.35\( \mu \)m shows a larger radius stability circle on the output than seen on the input.

Next, looking at the N130 transistor amplifier in Fig. VI.6, which represent an increase in gate finger number from the previous pair of transistor amplifiers to twenty-six, also has marginally stability.

A discussion similar to that above about \( \Gamma_S \) and \( \Gamma_{in} \) could be made regarding \( \Gamma_L \) and \( \Gamma_{out} \) for the Load-side, thus it will not be repeated. The \( \Gamma_L \) was again chosen from points on the Load-pull Smith chart where high Power Gain occurred under similar conditions to those described above regarding Source-pull Smith chart above, for matching.
Figure VI.4: Measured and Modelled N50µm x 0.35µm Load-Pull $\Gamma_{OUT}$ vs. $\Gamma_L$ at $V_{ds}=1.5$V and Freq.=5.0 GHz with Stability Circles.
Figure VI.5: Measured and Modelled N200µm x 0.35µm Load-Pull $\Gamma_{OUT}$ vs. $\Gamma_L$ at $V_{ds}$=1.5V and Freq.=5.0 GHz with Stability Circles.
Figure VI.6: Measured and Modelled N130 Load-Pull $\Gamma_{OUT}$ vs. $\Gamma_L$ at $V_{ds}=1.5V$ and Freq.=5.0 GHz with Stability Circles.
In summary for the load side matching, for all transistors, marginally stability means choosing tuning or matching of the input and output for the best power Gain as described in Section VI.4 under the constraint of stability.

**VI.4 Power Gain Theory of CMOS Amplifiers**

Next, we predict the Power Gain as a function of the $\Gamma_{in}$, $\Gamma_{out}$, $\Gamma_{Source}$, and $\Gamma_{Load}$, developed in Section VI.3, and then reviewed together with the predictions of the stability developed in Section VI.2.

Prediction of impedance matching for power Gain begins with examining Fig. II.2. The circuit of Fig. II.2 consists of an input matching block with impedance $Z_S$, a transistor amplifier with an input impedance, $Z_{in}$, and an output impedance, $Z_{out}$, and an output matching block with impedance $Z_L$ in addition to a source and a load.

For power Gain, just as for other RF design attributes, tuning or matching of an amplifier is a function of frequency; thus, $Z_S(\omega, 2\omega, 3\omega)$ and $Z_L(\omega, 2\omega, 3\omega)$, tune the input and output to the fundamental frequency and the second and third harmonics of the fundamental frequency for which the fundamental power Gain, $P_0$, and the first and second harmonics of power Gain, $P_1$, and $P_2$ can be defined. We shall deal only with the fundamental power Gain in three common forms in this discussion.
VI.4.1 Transducer Gain

The transducer power Gain of an amplifier is based on S-parameters and input and output tuning or impedance matching. The transducer power Gain is defined in VI.11 [21, 22]

\[
G_T = \frac{1 - |\Gamma_s|^2}{|1 - \Gamma_{1N}\Gamma_s|^2} S_{21}^2 \frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2}
\] (VI.11)

where \(\Gamma_{in}\) is defined in VI.8. Transducer power Gain is a measure of the ratio of power delivered to the load from the two-port network over the power available from the source of the two-port network. This definition of Transducer Power Gain depends on both \(\Gamma_s\) and \(\Gamma_L\). The Transducer Power Gain definition is commonly used for Power Gain.

VI.4.2 Operating Power Gain

The Operating Gain is defined in VI.12 [22]

\[
G_{op} = \frac{1}{1 - |\Gamma_{in}|^2} S_{21}^2 \frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|}
\] (VI.12)

The Operating Power Gain is a measure of the ratio of the power delivered to the load, from over the two-port network, over the power input to the two-port network. Now this Operating Power Gain definition is independent of \(\Gamma_s\) and some active circuits very much depend on source tuning. Also, this definition does predict what the Power Gain is with a specific input power when it reaches
the load. This definition of Power Gain is useful to researchers and engineers working in power amplifier (PA) design.

VI.4.3 Available Power Gain

The Available Power Gain is defined in VI.13 [22].

\[ G_A = \frac{1 - |\Gamma_S|^2 |S_{21}|^2}{|1 - S_{11}\Gamma_s|^2 |S_{21}|^2} \frac{1}{1 - |\Gamma_{OUT}|^2} \]  
(VI.13)

The Available Power Gain is the ratio of Power available from the two-port network over the Power available from the source of the two-port network. This definition of Power Gain is dependent on \( \Gamma_S \) but many amplifiers are dependent on load tuning as well. This definition of Power Gain is used in Noise Figure calculations and other cascaded calculations and should not be confused with Insertion Power Gain. Insertion Power Gain is frequently what is measured on the laboratory bench, where less concern is shown over what the matching conditions might be under which the Power Gain measurement is being made. Thus Insertion Gain (Loss) is defined as the gain realized across a boundary in a transmission path from the insertion of a device, active or passive:

\[ G_T = 10 \log \left( \frac{P_f}{P_i} \right) \]  
(VI.14)

where \( P_f \) is the Gain in the network immediately after insertion of the device and \( P_i \) is the network immediately before insertion of the device.
In conclusion, four Power Gain definitions and their dependencies have been reviewed. Each has a role in the theoretical predictions and calculation for optimum CMOS RF amplifier design strategies but they are each different and will yield different answers, even though the underlying conditions and S-parameter are similar. This will be seen next.

### VI.4.4 RF Power Gain Predictions

With the above definitions of power Gain, the amplifier’s power Gain as a function of tuning in relation to stability under the condition of constrained power dissipation can be predicted and examined. The RF power Gains are predicted for the 5.0 GHz CMOS transistors under two gate biases, $V_{gs} = 1.0$ V, $B_1$, and 1.5 V, $B_2$, with $V_{ds} = 1.5$ V from the Scattering Parameters made at $RF_{in}$ of $-25.0$ dBm as seen in Table VI.1. $\Gamma_L$ and $\Gamma_S$ values were taken at $RF_{in}$ of $-10.0$ and 0.0 dBm [21].

The S-Parameters were acquired at low RF Power, -25 dBm, thus the predic-
Table VI.2: Calculated Power Gain, dB, at 5.0 GHz based on Optimum Load-side Matching

<table>
<thead>
<tr>
<th>Trans. bias</th>
<th>Trans. Gain</th>
<th>Oper. Gain</th>
<th>Avail. Gain</th>
<th>$I_{DS}$ mA</th>
</tr>
</thead>
<tbody>
<tr>
<td>N200, B1</td>
<td>4.657</td>
<td>11.394</td>
<td>7.39</td>
<td>15.0</td>
</tr>
<tr>
<td>N200, B2</td>
<td>2.1</td>
<td>6.896</td>
<td>7.025</td>
<td>26.0</td>
</tr>
<tr>
<td>N50, B1</td>
<td>-7.32</td>
<td>6.435</td>
<td>5.10</td>
<td>4.0</td>
</tr>
<tr>
<td>N50, B2</td>
<td>-5.9</td>
<td>5.62</td>
<td>5.014</td>
<td>9.8</td>
</tr>
<tr>
<td>N130, B1</td>
<td>3.088</td>
<td>9.52</td>
<td>11.597</td>
<td>9.0</td>
</tr>
</tbody>
</table>

...tions made for power Gain can be different from what has been measured and will be discussed in the Chapter IX, where comparisons of theory and measurement will be made.

Examining the prediction of the Load side Power Gain, the trend of greater Power Gain, regardless of Power Gain definition, with greater CMOS transistor gate width is observed in Table VI.2. Also, the prediction of slightly less Power Gain with an increase in gate bias is seen. This occurs because of the decline or flatten of $g_m$ as bias increases. The calculated values of Table VI.2 are constructed by choosing optimum values in $\Gamma_L$ for Power Gain with the Source matching fixed under Load-pull Testing. By using optimum values, the highest Power Gains can be found, remembering that the Power Gain predictions are based on S-parameters taken at a much lower input power and without tuning. This partially explains the rather low level of predicted performance. An unproven assertion is that if the S-parameters were measured under conditions similar to the Power Gain measures, then the match between prediction and measurement would be better.
The Transducer Power Gain is a measure of the ratio of available power from the source to delivered power in the load. [22], and is low because of the S-parameters. The S-parameters were measured at low RF power, unlike the actual Power Gain measures of the RF CMOS transistors. Transducer Power Gain depends on both input and output tuning.

The grounded-source CMOS amplifier is better described by the Operating Power Gain because of the definition more closely matches the condition of a power delivered to the load over a specific input power. This prediction will be evaluated in Chapter IX. Operating Power Gain is dependent on the amplifier and the output tuning.

The Available Power Gain is defined to be the ratio of the power available from the network over power available from the source. Thus, the definition of Available Power Gain is consistent with Noise Figure (NF) evaluation where the evaluation of noise figure is based on the input network and the amplifier performance, excluding the load tuning [21]. Also, the noise input power level used in Noise Figure Theory is very low. This is consistent with predictions of Available Power Gain based on low RF power Scattering parameters.

In Table VI.3, the Power Gain peeks in the N130\(\mu\)m x 0.35\(\mu\)m transistor and shrinks slightly with increases in gate bias. The reason for the Power Gain falling off as the gate bias increases occurs because of the flattening slightly of the slope of transconductance, \(g_m\), with increase gate bias [2]. The calculated values
Table VI.3: Calculated Power Gain, dB, at 5.0 GHz based on Optimum Source-side Matching

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>N200, B1</td>
<td>-0.952</td>
<td>8.713</td>
<td>4.89</td>
</tr>
<tr>
<td>N200, B2</td>
<td>-0.306</td>
<td>7.943</td>
<td>4.535</td>
</tr>
<tr>
<td>N50, B1</td>
<td>-9.965</td>
<td>7.321</td>
<td>1.19</td>
</tr>
<tr>
<td>N50, B2</td>
<td>-6.29</td>
<td>7.134</td>
<td>3.085</td>
</tr>
<tr>
<td>N130, B1</td>
<td>0.771</td>
<td>13.732</td>
<td>4.52</td>
</tr>
<tr>
<td>N130, B2</td>
<td>1.67</td>
<td>14.439</td>
<td>4.162</td>
</tr>
</tbody>
</table>

of Table VI.3 are constructed by choosing optimum values for Power Gain with the Load matching fixed with the Load matching fixed under Source-pull Testing. By using optimum values, the highest Power Gains can be found, remembering that the Power Gain predictions are based on S-parameters taken at a much lower input power and without tuning. This partially explains the rather low level of predicted performance. An unproven assertion is that if the S-parameters were measured under conditions similar to the Power Gain measures, then the match between prediction and measurement would be better.

VI.5 Optimization of Spur-Free Dynamic Range in RF CMOS Amplifiers

Successful RF/analog design depends on design choice for stability in conjunction with next best choices for $I_{1dB}$, minimum Noise Figure, and Bandwidth using the CMOS transistors as grounded-source amplifiers. The key element of
stability for RF CMOS design has been developed in Section VI.2. So far in examining the $III P_3$, minimum Noise Figure, Power Gain, and Stability of CMOS transistors as grounded-source amplifiers, the tuning or impedance matching for the best choice of each of these RF attributes is different. Thus, the optimum capability for each RF attribute to be realized simultaneously in one application is not achievable [44,45]. The first example of this difference was shown in Section VI.4, where the trade-off of stability over tuning for optimum Power Gain was predicted and examined.

Now, a broader trade-off of combined RF attributes versus constrained power consumption, will be developed, using a widely known figure-of-merit called the Spur Free Dynamic Range, $SFDR$, in the context of four RF trade-offs; namely, $III P_3$, Noise Figure, Bandwidth, and Stability. Remembering that the grounded-source CMOS transistor is marginally stable, tuning or matching choices to optimize other RF design attributes can have the unintended effect of causing the amplifier to oscillate. Keeping in view that any matching choices for optimizing other RF design attributes must be chosen to ensure stability first, we next develop the predictions for a combined figure-of-merit (FOM), Spur Free Dynamic Range, $SFDR$ for the RF CMOS grounded-source amplifier to improve predictions in optimum design practice.
VI.5.1 Optimum Dynamic Range Scaling

The optimum dynamic range scaling can now be predicted as a function of current density, transistor size, match, Power Gain, minimum Noise Figure, maximum $I_{N}I_{P3}$, and greatest SFDR. The definition of spur free dynamic range, $SFDR$, is stated in VI.15 and relates three RF attributes together at once; namely, $I_{N}I_{P3}$, Noise Figure, and Bandwidth [29].

$$SFDR = \frac{2}{3}(I_{N}I_{P3} - MDS)$$ (VI.15)

$SFDR$ is seen to depend on $I_{N}I_{P3}$ and MDS. The definition of Minimum Detectable Signal (MDS) is stated where $B$ represents bandwidth and is set to 200 MHz [29].

$$MDS = -174 + NF + 10 \times \log(B)$$ (VI.16)

MDS depends on Noise Figure and bandwidth; thus, $SFDR$ depends on $I_{N}I_{P3}$ and Noise Figure. These two quantities together make $SFDR$ a source-side matching dependent figure-of-merit in evaluating a system level RF CMOS microwave amplifier design parameter.

In Fig. VI.7, $SFDR$ is shown to extend from the minimum detectable signal to the point in input power where the $IMD_3$ begins to rise above the noise floor. $SFDR$ is an FOM for optimizing an RF design. It is important because it provides a means by which to understand the consequences of RF design trade-
offs in terms such as gain, $III P_3$, and NF, of a system level performance related to overall carrier-to-noise (C/N). SFDR then provides a tool for understanding the optimization choices in RF design practices relative to the overall system requirements. Choices can be made to increase the MDS, which provides greater sensitivity, but at the expense of linearity. On the other hand, increasing $III P$ can increase the ability of the RF receiver to handle larger signals without in-band nonfilterable distortion. Several cautions exist with the use of SFDR as a system level parameter in its current guise. First, while the theory for predicting $III P_3$
in Chapter IV, and minimum Noise Figure in Chapter V, and Power Gain in this chapter have been developed, with the exception of Noise Figure, the position on the Smith charts of the maximum $\Pi IP_3$ or Power Gain is not directly predicted for the required matching termination, only their magnitudes relative to a given or chosen $\Gamma$ or matching termination. Expanding the theory for $\Pi IP_3$ and Power Gain to accurately predict magnitude and matching termination position is a basis for further research. Given the limitations of the above theory, a second caution is made; namely, that the position of the maximum SFDR is not known relative to the minimum Noise Figure, maximum $\Pi IP_3$, or Power Gain. Next, the third caution about the predictive usefulness of SFDR is made; that is, with the ambiguity of relative matching termination or $\Gamma$ positions on the Smith charts for each best choice parameter in SFDR, different optimization strategies could be produced which favor one component against the others of the SFDR formulation. The fourth and last caution is that a chosen optimizing strategy for SFDR may place the matching termination on the Smith chart in a location of instability for the RF CMOS amplifier circuit design.

VI.5.2 Optimum Dynamic Range Scaling Predictions

As an example of the trade-offs in SFDR between maximum $\Pi IP_3$ and minimum Noise Figure, the SFDR of four grounded-source amplifiers from the source or input side prediction are calculated in three different modes, one emphasizing the maximum $\Pi IP_3$ another emphasizing minimum Noise Figure, and
Table VI.4: SFDR of Si CMOS Grounded-Source Amplifiers, Source Side, \( V_{DS}=V_{GS}=1.5V \)

<table>
<thead>
<tr>
<th>SFDR, dB</th>
<th>N50</th>
<th>N130</th>
<th>N200</th>
<th>N520</th>
</tr>
</thead>
<tbody>
<tr>
<td>( III P_3 )</td>
<td>76.1</td>
<td>79.3</td>
<td>73.0</td>
<td>74.6</td>
</tr>
<tr>
<td>NF</td>
<td>79.1</td>
<td>78.9</td>
<td>76.3</td>
<td>73.9</td>
</tr>
<tr>
<td>Gain</td>
<td>67.3</td>
<td>69.3</td>
<td>67.0</td>
<td>73.0</td>
</tr>
</tbody>
</table>

the last emphasizing maximum Power Gain. Table VI.4 contains tabulated predictions. A bias of \( V_{GS} = 1.5V \) is used for each of the four grounded-source amplifier SFDR prediction calculations.

The bias conditions used to construct Table VI.4 were \( V_{DS} \) and \( V_{GS}=1.5V \) and optimum source-side matching with a fixed load. Then for each cell in Table VI.4, the optimum gain, NF, or \( III P_3 \) was examined relative to the optima of the others. The decrease of each in favor of the one emphasized was found and the SFDR calculation was made. For example, if the minimum NF was found at \( \Gamma_{opt} \) and the optima for Power Gain and \( III P_3 \) were elsewhere, then the loss for each of the other two parameters relative to the optima of NF was determined. This allowed the construction of each cell in Table VI.4 and the prediction of SFDR for at least one bias condition.

Upon examining the predictions, an interesting trend is discernable. The spread in difference between optimizing for maximum \( III P_3 \) or minimum Noise Figure is reduced with increasing gate finger number. For example, the N200\( \mu m \) x 0.35\( \mu m \) and N50\( \mu m \) x 0.35\( \mu m \) grounded-source amplifiers have ten gate-fingers and a 3.0 dB spread, depending on an emphasis of \( III P_3 \) or Noise Figure. The
N130\(\mu m\) x 0.35\(\mu m\) and N520\(\mu m\) x 0.35\(\mu m\) grounded-source amplifiers have twenty-six gate fingers and less than a 1.0 dB spread, depending on an emphasis of \(III P_3\) or Noise Figure. The reduction in the spread is caused by the reduction in gain in the N520\(\mu m\). Had the N520\(\mu m\) had expected gain, then the spread of large to small would have occurred.

Next, examining SFDR predictions emphasizing maximum Power Gain, a loss of 7 to 10 dB for the N200\(\mu m\) x 0.35\(\mu m\) amplifier and 9 to 12 dB for the N50\(\mu m\) x 0.35\(\mu m\) amplifier from either prior emphasis on minimum Noise Figure or \(III P_3\) is seen in Table VI.4. For the 26 gate-fingered amplifier, the loss in SFDR is 10 dB for the N130\(\mu m\) x 0.35\(\mu m\) amplifier and 0 dB for the N520\(\mu m\) x 0.35\(\mu m\) amplifier. The trend in the case of emphasizing maximum Power Gain shows a significant penalty in SFDR for ten or twenty-six gate-fingered devices. Only in the case of a moderate Power Gain grounded-source amplifier, such as the N520\(\mu m\) x 0.35\(\mu m\), is the penalty in SFDR almost eliminated. Thus, in the case of higher Power Gain amplifiers, SFDR is reduced significantly when the choice for maximum Power Gain and its associated matching termination impedance is emphasized over the matching termination impedance choices of maximum \(III P_3\) or minimum Noise Figure. This last relationship shows how strikingly the choice in microwave matching termination impedances or \(\Gamma’s\) effect the cost of optimizing one RF design attribute against others can be.
VI.5.3 SFDR RF CMOS Amplifier Design Optimization Predictions

Lastly, the predicted trade-off of Power Gain, $\Pi P_3$, and minimum Noise Figure is shown in Fig. VI.8. Here the costs in SFDR of different strategies of optimization can be seen relative to the source matching termination impedances. The trade-off in each of four RF CMOS ground-source amplifiers with different geometry are shown in the following four Fig.’s VI.8 at a $V_{GS} = 1.5V$.

VI.5.4 Summary of Optimum Dynamic Range Scaling

In summary, the maxima of Power Gain and $\Pi P_3$, and the minima of Noise Figure have been predicted and displayed relative to stability. The finding is that of these three RF design attributes, the optima do not occur at coincidental points on the source or load side of the Smith chart for these RF CMOS grounded-source amplifiers. Thus, trade-offs amongst these RF design attributes must be made because of lack of coincidence in the optima amongst them. Next, upon combining these design attributes into SFDR and examining the optimum values, the cost of the trade-off amongst the RF attributes was quantified for these RF CMOS grounded-source amplifiers. The trends of SFDR range prediction showed that a higher gate-fingered device is predicted to minimize the trade-off of maximum $\Pi P_3$ versus minimum Noise Figure and that Power Gain optimization was at the expense of maximum $\Pi P_3$ or minimum Noise Figure.
Figure VI.8: N200μm x 0.35μm SFDR vs. Maximum Power Gain, $\text{III}P_3$, and minimum Noise Figure
VI.6 Summary

In conclusion, the CMOS transistors, with matching in both the input and output side, formed a grounded-source amplifiers at 5.0 GHz. The performance was predicted as a function of marginally stability under the condition of minimized power consumption constraint for maximum Power Gain. Tuning of either the input or the output of the grounded-source amplifier must be done in consideration of maintaining amplifier stability over bias and temperature. Having accessed the region where stable matching can occur, the transistor amplifier’s performance in Power Gain, $\text{III}_P^3$, or Noise Figure, amongst other RF characteristics as a function of source and load tuning at 5.0 GHz, can be better chosen for optimal design implementation of the CMOS transistors.

The text of this chapter, in part, is a reprint of the material as it appears in our published papers in *IEEE Conferences* [SiRF03, Germany; IEDM99, USA] and in preparation for *Conferences and Transactions on Microwave Theory and Techniques*. The dissertation author was the primary investigator and primary and secondary author of these papers.
Chapter VII

LNA Design

VII.1 Introduction to LNA Design

Two Low Noise Amplifiers (LNA) for 5.0 GHz and 26.0 GHz applications were designed to implement both the system level design of Chapter I: Introduction and System Architecture and Chapter II: Radio Architecture and the circuit optimizations techniques developed in Chapter VI: Optimum Design for CMOS RF Amplifiers in CMOS with two different processes. We begin with a description of the desired performance objectives, followed by the design method, then the performance predictions, and layout of the circuits. The results from testing the built designs are reviewed in Chapter IX: Experimental Verification of Theory.

VII.2 LNA for 5.0 GHz IMS Application

The first LNA design is aimed at IMS band applications which include wireless local area network (WLAN) designs. The 5.0 GHz LNA design was fab-
ricated in Agilent Technologies (HP) 0.35µm four-level metal process through MOSIS. The design procedure will be reviewed next. The AT 0.35µm wafer fabrication process is labelled as the CMOS10 Silicon Technology. This process is a high density digital 0.35µm CMOS process targeted for ASIC designs and features a 0.35µm minimum gate length device optimized for 3.3 V operations with high current drive. High density is achieved through use of a tight pitch, planarized interconnect system that allows four levels of metallized interconnect. Self-aligned silicidation of the polysilicon and diffusion regions provide low gate contact and diffusion resistances [46].

VII.2.1 5.0 GHz LNA Design Goals

The design of an LNA is complicated by the simultaneous requirements of a RF front-end amplifier. First, the LNA must achieve low noise in its design while having adequate Gain, and acceptable power consumption. Second, the LNA must have reasonable intermodulation performance. Of lesser concern but still important are the operating bandwidth and amount of die area consumed to accomplish the design. Many other RF parameters exist which can also be of concern but will not be specifically addressed here. The Table VII.1 shows the design goals for a 5.0 GHz LNA from Table II.1 of Chapter I: Introduction and System Architecture.
Table VII.1: IMS LNA 5.0 GHz Design Goals

<table>
<thead>
<tr>
<th>Design Goal</th>
<th>5.0 GHz LNA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain, dB</td>
<td>10.0</td>
</tr>
<tr>
<td>NF dB</td>
<td>5.0</td>
</tr>
<tr>
<td>$IIIP_3$ dBm</td>
<td>10.0</td>
</tr>
<tr>
<td>Die Area mm²</td>
<td>500.0</td>
</tr>
<tr>
<td>Power Cons. mW</td>
<td>20.0</td>
</tr>
</tbody>
</table>

VII.2.2 Design, Simulation, and Layout of 5.0 GHz LNA

The design topology used in this design is a single-ended cascode structure with inductive matching for improved Noise Figure. Interdigitation of the gate reduces Noise Figure without an increase in power consumption. The resistance of the gate is reduced because of the breaking down of the gate into smaller pieces that are made in parallel. This reduces phase errors as well as gate resistance. The cascode structure provides higher output impedance while reducing the Miller effect. An output grounded-source buffer drives the load. The design is seen in Fig.VII.1. The best matching to achieve Operating Gain, Noise Figure, and $IIIP_3$ do not occur simultaneously as has been discussed in Chapter VI: Optimum Design for CMOS RF Amplifiers. As a result of the conclusions of Chapter VI, a choice for matching is made to optimize the Operating Gain over $IIIP_3$. Also of importance is the design of the MOSFET’s to minimize noise sources in order to reduce the Noise Figure of the LNA.

Simulations were then performed to find the best Gain as a function of device gate width under the constraint of minimum power dissipation; that is,
Figure VII.1: Pspice Simulation Schematic of 5.0 GHz LNA

Figure VII.2: Pspice Simulation of 5.0 GHz LNA
Figure VII.3: L-edit Layout of 5.0 GHz LNA

$V_{DS}=1.5$ V and $V_{GS}=1.0$ V. The predictions of Gain at 12.0 dB and Noise Figure at 1.2 dB are shown in Fig.VII.2 at 5.0 GHz and $V_{DS} = 1.5V$.

The layout of the design was performed in L-edit and is shown in Fig.VII.3. The design of the inductors and their simulation was covered in Chapter VI.

The test results and performance of this design will be reviewed in Chapter IX.

The design of an LNA in an RF circuit requires the trade-off of many important characteristics: Power Gain, NF, and linearity amongst others [30]. This situation forces choices in the design of RF circuits. In the LNA design, the most
important RF characteristics are low-noise, moderate gain, high linearity, and stability. Of secondary importance is power consumption and layout design size.

LNA topologies occur in many forms with common-gate and common-source designs dominating [6, 47]. The common-gate configuration has a NF minimum of approximately 3.0 dB as a disadvantage, but does not suffer from the Miller effect. The common-source with inductive degeneration has an advantage of input termination matching with no added resistive noise. However the disadvantage is larger design area for inductors and the poor inductor and capacitor quality factor. Fig. VII.4 shows the MOS cascode (common-source/gate) circuit. This provides significant gain with high input impedance and low voltage across $M_1$ [48]. The bypass capacitor attached to $M_2$ provides small-signal ground, while the inductor on the drain of $M_2$ provides large-signal bias and resonates with the capacitance of $M_2$ at the $f_o$ of 5 GHz. The cascode MOSFET, $M_2$, reduces the Miller effect of a MOSFET common-source amplifier by isolating the output capacitance from the input. By reducing the apparent input capacitance, the performance of the CMOS amplifier at high frequency is maintained. The cost with this arrangement is a small increase in noise and layout area from an additional MOSFET [25].

The Power Gain is a function of the S-Parameters of the amplifier and its impedance match tuning [49]. An optimum tuning for each RF parameter was used near $Z_s$ of 50 $\Omega$ for Power Gain, NF, and $I_{III P_3}$. The trade-off represents
Figure VII.4: LNA Cascode MOSFET Circuit Model Including Impedance Tuning.

A degradation of 1 to 2 dB for each RF characteristic relative to the others. As a simplification, the NF of the input MOSFET is considered only to guide an estimate of the upper bound expected. The Noise Factor can then be specified in terms of input currents, $F = \frac{i_{nt}^2}{i_{ns}^2}$, where $i_{nt}$ is the total input noise current from all sources and $i_{ns}$ is the input noise current due to the source admittance only. The current is given by, (V.3),

$$i_{nt} = i_{ns} + i_{gr} + i_{sub} + i_g + i_{in} + Y_s e_n$$  \hspace{0.5cm} (VII.1)

$$F_{\text{min}} = 1 + \frac{R_{gr}}{R_s} + \frac{R_{sub}}{R_s} + 2R_n(G_{opt})$$  \hspace{0.5cm} (VII.2)

where $i_{ns}$ is the source noise current, $i_{gr}$ is the noise current due to the polysilicon gate resistance, $i_{sub}$ is the input current due to the substrate resistance, $i_g$, is the induced gate noise current, $i_{in}$, is the equivalent input noise current due to the drain, $Y_s$, is the source admittance, and $e_n$, is the equivalent input noise voltage
due to the drain.

The final form of the minimum NF is seen in (V.26) where $R_n$ is the Equivalent Noise Resistance and $G_{opt}$ represents the optimum source conductance for the minimum NF [30]. The prediction is 2.1 dB of NF for a single interdigitated-gate transistor of 200 x 0.35 $\mu$m. In the trade-off of Linearity vs. Noise Figure, two concerns are primary. If a design results in poorer $IIP_3$ in favor of Noise Figure or Gain, in-band distortion will occur at the front-end of the RF receiver chain. If the Noise Figure minimum is too high in favor of linearity or gain, the receiver sensitivity may be compromised. In this design, a tradeoff between gain, $IIP_3$, and NF was made by examining the regions of the Smith chart where the optimum performances occurred.

VII.3 Millimeter wave 26.0 GHz LNA

We now describe the design of a millimeter wave LNA using the least complicated method of realize the goal in a 0.15 $\mu$m CMOS process.

VII.3.1 Design Goals for 26.0 GHz LNA

The goal of the 26.0 GHz LNA design was to provide a implementation of the RF system specification in a circuit realization under the constraint of minimum power dissipation in millimeter wavelength range using a 0.15 $\mu$m process at the Burlington, Vermont wafer fabrication facility of IBM. The design goals
Table VII.2: Design Specifications of 26.0 GHz CMOS LNA

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Bulk</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{MAX}$, dB</td>
<td>10.0</td>
</tr>
<tr>
<td>NF, dB</td>
<td>6.0</td>
</tr>
<tr>
<td>Gain, dB</td>
<td>3.0</td>
</tr>
<tr>
<td>$</td>
<td>S_{11}</td>
</tr>
<tr>
<td>$</td>
<td>S_{21}</td>
</tr>
<tr>
<td>$</td>
<td>S_{22}</td>
</tr>
<tr>
<td>$</td>
<td>S_{12}</td>
</tr>
</tbody>
</table>

for the LNA are listed in Table VII.2 as follows: a functioning 26.0 GHz LNA at 1.5V with the listed performance specifications.

VII.3.2 Design, Simulation, and Layout of 26.0 GHz LNA

A passive transmission line load, grounded-gate design was chosen to implement the LNA with a constant current source to meet the Gain requirement by minimizing the miller effect of the grounded-source design. The $f_t$ of this IBM process is approximately 90 GHz.

The LNA circuit design is shown in Fig.VII.5 for simulation in Cadence. The split passive load instead of a cascode design was used in the simulations to achieve the high frequency Gain. The input and output transmission lines were designed to match 50 Ω at 26.0 GHz.

The results of simulation show Gain of about 5.0 dB at 26.0 GHz using a 1.5 V supply and a 10 mA constant current source.

The passive transmission line LNA design was laid-out in L-edit as shown in
Figure VII.5: Cadence Simulation Schematic of 26 GHz LNA showing gain curve sweeps.

Figure VII.6: Cadence Simulation of 26 GHz LNA
Figure VII.7: L-Edit Layout of 26 GHz LNA
Fig. VII.7 and a enlarged section of the layout is shown in Fig. VII.8. The single load transmission line and two matching input and output transmission lines are visible in the layouts. These are distinctive features of millimeter wave design when contrasted with the layout of C-band inductively matched 5.0 GHz LNA layout of Fig. VII.3.

The test results of this 26.0 GHz design will be reviewed in Chapter IX: Experimental Verification of Theory.
VII.4 LNA Summary

Two designs for LNA application have been presented which used two different CMOS processes. Both designs produced acceptable simulations from two different simulators regarding their design goals and were laidout. These simulation predictions further support the expanded use of CMOS in RF applications in the ISM and millimeter wave bands. Acceptable trade-offs can be made with very good performance at Super and Extremely High Frequencies in Gain, Noise Figure, and $I_{IP3}$.

The text of this chapter, in part, is a reprint of the material as it appears in our published papers in *IEEE Conferences* [SiRF03, Germany; IEDM99, USA] and in preparation for *Conferences and Transactions on Microwave Theory and Techniques*. The dissertation author was the primary investigator and primary and secondary author of these papers.
Chapter VIII

Laboratory Experiment and Test Engineering

VIII.1 Introduction

To paraphrase two great theoretical scientists, "All good theory must be verified with careful empirical experiment," (Einstein, Feynman). Thus, we review here how the theory developed and results predicted of prior chapters were measured. In Chapter IX: Experimental Verification of Theory, we review the success of the predictions through the measurement methods described in this chapter.

The topics we shall deal with in detail in this chapter are the design of experiments (DOE), [50] for the verification of theory and predicted results, the laboratory equipment, and the measurement methods.
VIII.2  Design of Experiment

During the course of this research, several device and circuit layouts were constructed based on literature review, ingenuity, theoretical predictions, and simulations in order to create a systematic method to evaluate the efficacy of our ideas and theoretical predictions. The DOE’s have been previously identified in prior chapters but we repeat here some of the goals previously described.

VIII.2.1  Layouts Submitted for Experimental Verification

Portions of the following layouts submitted to wafer fabrication facilities have been shown in prior chapters. In Agilent Technologies (AT) 0.35μm CMOS process, available through USC’s MOSIS, two layouts were submitted. These layouts included calibration structure, inductor, transformer, capacitor, transistor and LNA circuit designs. These have been previously identified as DOE I, II, III, and IV. Only DOE’s II and III were fabricated in this process.

In AT’s 0.55μm CMOS process, one layout was submitted. This layout contained calibration structure, inductor and power amplifier circuit designs. This has been previously identified as DOE V.

In IBM’s 0.15μm CMOS process, one layout was submitted. This layout contained calibration structure, transmission line, transistor, and Extremely High Frequency LNA circuit designs. This has been previously identified as DOE VI.

Additionally, layouts were tested at the wafer level not designed in this re-
search plan from Peregrine Semiconductor, Inc. and Auburn University which consisted of passive device, transistor, and calibration structure designs.

### VIII.2.2 Design of Experiment

In order to check the validity of the theoretical predictions, the following experiments were designed. The first experiment designed was to evaluate resonant passive elements for the Quality Factor and performance as a function of design layout.

One metal plate capacitor was included in this DOE II. The transistors and LNA circuit were not functional because of a layout error. The inductors and capacitor were measured and will be reported on in Chapter IX: Experimental Verification of Theory.

In DOE III additional inductors, shown in Table VIII.3, of seven- and three-turn were added to the test transistors listed in Table VIII.2. Also four MOS capacitors, improved calibration structures, and a new LNA were added to the layout design. The transistor set of DOE III make up a design of experiment over gate structure by varying gate width and finger number. One common-gate design
Table VIII.2: Test Transistor Geometry.

<table>
<thead>
<tr>
<th>Device</th>
<th>Gate Finger Width in μm</th>
<th>Number of Fingers</th>
</tr>
</thead>
<tbody>
<tr>
<td>N50</td>
<td>5</td>
<td>10</td>
</tr>
<tr>
<td>N200</td>
<td>20</td>
<td>10</td>
</tr>
<tr>
<td>N130</td>
<td>5</td>
<td>26</td>
</tr>
<tr>
<td>N520</td>
<td>20</td>
<td>26</td>
</tr>
</tbody>
</table>

Table VIII.3: Design of Experiment III: Inductors.

<table>
<thead>
<tr>
<th>Inductor</th>
<th>7-turn</th>
<th>3-turn</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>N-well</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Fractured N-well</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Fractured Poly/N-well</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Fractured Metal 1/N-well</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Fractured Poly</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Fractured Metal 1</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>

was included as before in DOE II.

The inductor set of DOE III is different than DOE II where the shielding effectiveness of lower process layers to top level metal is studied. In this process metal four is the top level metal and shielding it to eddy currents in the lossy substrate of bulk CMOS is desired. What is unknown and difficult to predict is the benefit of shielding the top-level metal from the lossy substrate to improve the Q of the inductors designed in this process. This is shown in Table VIII.3.

The capacitor set of DOE III was changed from DOE II to include four MOS capacitors of increasing area to determine the scaling of capacitance as a function of junction area.

Transformers, inductors, and calibration structures were included in the
Table VIII.4: Test Capacitor Geometry.

<table>
<thead>
<tr>
<th>Device</th>
<th>Area in $\mu m^2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOS1</td>
<td>630</td>
</tr>
<tr>
<td>MOS2</td>
<td>1206</td>
</tr>
<tr>
<td>MOS3</td>
<td>2440</td>
</tr>
<tr>
<td>MOS4</td>
<td>5040</td>
</tr>
</tbody>
</table>

Table VIII.5: Design of Experiment V: Inductors.

<table>
<thead>
<tr>
<th>Inductor</th>
<th>3-turn</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate</td>
<td>✓</td>
</tr>
<tr>
<td>Poly, Fine Mesh</td>
<td>✓</td>
</tr>
<tr>
<td>Poly, Medium Mesh</td>
<td>✓</td>
</tr>
<tr>
<td>Poly, Finger narrow wide</td>
<td>✓</td>
</tr>
<tr>
<td>Poly, Finger wide with center taps</td>
<td>✓</td>
</tr>
<tr>
<td>N-well mesh</td>
<td>✓</td>
</tr>
<tr>
<td>No center tap</td>
<td>✓</td>
</tr>
</tbody>
</table>

DOE V with power amplifier designs in the Agilent Technologies (AT) 0.55$\mu$m CMOS process.

The DOE V allows determination of the efficacy of different shielding for inductors in the Agilent Technologies (AT) 0.55$\mu$m CMOS process as described in Table VIII.5.

The transformer DOE provides a means of measuring the scaling as a function of transformer turns ratio as seen in Table VIII.6.

Table VIII.6: Design of Experiment V: Transformers.

<table>
<thead>
<tr>
<th>Transformers over Poly, Medium Mesh</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>XTRM1</td>
<td>1:1</td>
</tr>
<tr>
<td>XTRM2</td>
<td>1:3</td>
</tr>
<tr>
<td>XTRM3</td>
<td>1:5</td>
</tr>
</tbody>
</table>
Table VIII.7: Design of Experiment V: Transmission Lines.

<table>
<thead>
<tr>
<th>Transmission Line</th>
<th>μm Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>T1</td>
<td>800</td>
</tr>
<tr>
<td>T2</td>
<td>1200</td>
</tr>
<tr>
<td>T3</td>
<td>1200</td>
</tr>
</tbody>
</table>

The last DOE VI is a series of different length transmission lines along with a pair of N- and P-transistors and Extremely High Frequency LNA. The transmission line set provides a means of determining the scaling of impedance match and propagation delay with length.

The results of these experiments will be discussed in Chapter IX: Experimental Verification of Theory

### VIII.3 DC Measurement

The large signal measurements made on test devices consisted of I-V measures on MOSFET’s presented in Chapter III: CMOS and Device Modelling. The method of measuring the MOSFET’s was through wafer probing on an Cascade. The test sample was adhesively attached to a larger substrate for vacuum retention on a 200 mm chuck. Extremely High Frequency ground-signal-ground picoprobes from GGB Industries were used to contact the layout. These probes were attached to AT 4155 Semiconductor Parametric Analyzer (SPA). The AT 4155 produces a ramped step voltage and measures the current response displayed on a screen. This data can be loaded onto the network via AT’s ICCAD software taken with
VIII.4 Small-Signal Measurement

Small-Signal measurements were made of passive components, transistors, and circuit designs. Inductors and capacitors were measured for resonating circuit design applications using Scattering Parameters (S-parameter) taken using an AT 8510C Vector Network Analyzer (VNA). Grounded-source and grounded-gate microwave transistor amplifiers were measured for S-parameters using a VNA and RF performance using a Focus Load-pull System. LNA circuit design performance measurements were made also using a Focus Load-pull System. Finally Noise measurements were made using a Focus Noise Measurement System. The
following discussion will examine the methods of acquiring the measurement data predicted in earlier chapters and reviewed against predictions in Chapter IX: Experimental Verification of Theory.

A non-apparent aspect of this part of the research is the significant mechanical delicacy of the microwave circuitry supporting the measurements. This aspect of the Test Engineering is overlooked by people seeing the results and is frequently misunderstood and greatly underestimated in its difficulty to maintain in good operating effectiveness.

**VIII.4.1 S-Parameter Measurement**

The S-parameter taken were measured on the Signatone Prober using the AT 8510C system. The theory of S-parameters was described in Chapter III: CMOS and Device Modelling. The discussion now will deal with the operation and calibration methodology of the VNA as shown in Fig. VIII.2. Other significant and common uses for the VNA are SWR, return loss, group delay, impedance, and time domain analysis through IFT of the frequency domain data.

The Vector Network analyzer contains several sections to accomplish the measure and display of S-parameter which are obtained from the basic block diagram in Fig. VIII.3. The device under test (DUT) is stimulated by the RF source from which are captured the transmitted and reflected waves for the receiver and used to create and update the display. The main blocks are the Digital processor/display, Intermediate Frequency (IF) processing, RF Test Set, and RF Oscilla-
Figure VIII.2: AT 8510C Vector Network Analyzer, [4].
tor source as shown in Fig. VIII.4. The VNA is a many component and processing system, operating from RF to digital modes.

Referring to Fig. VIII.4, the typical measurement involves several steps to accomplish the display of S-parameter. First the RF source is operated in a swept style from the lower to higher measurement frequency range. The signal couplers route the incident signal and the responses from the DUT to accomplish the first IF conversion. Digital pretuning between 50 MHz and 300 MHz of the voltage-controlled oscillator (VCO) so that one of the VCO’s harmonics mixes with the source to produce a first IF close to 20 MHz. Fine tuning is accomplished by comparison of the IF with the internal crystal frequency and sweeping the VCO to track the stimulus frequency.

The second IF is about 100 KHz for detection and data processing. To maintain phase coherence, IF signal paths are carefully matched. Much automatic
gain control (AGC) is performed to achieve optimum performance in successive frequency bins.

The measurement can use $a_1$ or $a_2$ as a reference signal and one of the remaining signals as a test signal. During a sweep, the selected input is sampled with a 0 to 10 volt sweep. The sweep voltage is applied to the reference and test detectors. From this pair, the real and imaginary components of the signal are created.

Digital signal processing is performed by the central processing unit (CPU). Many corrections are applied to gain and quadrature errors in the reference and test pairs with ratioing and storing of data arrays. Averaging is performed on the accumulated data, while error correction is applied at the end of the sequence.
before display updating.

This is a simplified discussion of the vector network processing which is somewhat more complicated and sophisticated than outlined here however the basic elements have all been present. Much more literature and texts exist on the detailed operation of a VNA and can be independently read [4].

The last significant component of test methodology is the calibration sequence or error reduction method. This procedure allows the measuring and storing of VNA responses of known standards in the memory of the VNA. Two main methods exist which can be performed either coaxially or on-wafer. Also the type of standards used fall into two main groups. One is the Thru-Reflect-Line and the other is Open-Short-Load. Others exist but these two are the very common in determining the appropriate corrections for the system and the extensions to the Test Set Reference Plane by S-parameter mathematical matrix operation. Highly repeatable and accurate S-parameter can be obtained with the use of error correction procedures. Repeatability can be obtained to better than 0.1 dB at 20 GHz.

VIII.4.2 Load-Pull Measurement System

The RF measurement system consists of many components to obtain matched and unmatched programmatic termination impedances. The motivation and implications for performing RF measurements in this manner has been discussed in previous chapters. We describe here how the Load-Pull Measurement System operates and some of its capabilities, Fig. VIII.5.
The block diagram of the Load-Pull Measurement System is shown in Fig. VIII.6. Following calibration of the microwave connections from the source and receivers via the VNA, the measurement of Gain, IMD, Harmonic tuning effects, compression point, AM/PM effects, Oscillator, Adjacent Channel Power, Pulse Measurements as a function of termination impedance can be made. The termination impedance is a function of the fundamental and 2nd and 3rd harmonics.

The basic impedance termination dependency in microwave performance is shown in Fig. VIII.7. To effect the matching and unmatching of termination impedance as seen in Fig. VIII.7 a two-port network is interspersed between the generator or source on the left side of the diagram and the DUT and another on the right side of the diagram between the DUT and the load. A generator can be any exciting source, in this case, it is provided by RF sources. The receivers in the
Figure VIII.6: Block Diagram of Load-Pull Measurement System.

Figure VIII.7: Common-source Microwave Amplifier Block Diagram.
setup are a spectrum analyzer and a power meter.

Since the general solution for a two-port network in this situation is the solution to a quasi-TEM mode resonator, another method can be employed to realize the impedance value as a function of wave-guide resonator shape or slug position. In computer-controlled system known specific impedances can be determined by measurement using a VNA instead of by calculation. These measured termination impedances can be used to determine the measured RF response as a function of predetermined impedance.

**VIII.4.3 Noise Measurement**

The Noise Measurement System consists of a computer-controlled test apparatus employing the AT 8970B Noise Figure System, the Focus source tuner, the VNA, and a Cascade microwave prober as seen in Fig. VIII.8

The AT 8970B Noise Figure System is described now because the Source Tuner, VNA, and Cascade microwave prober have previously been discussed. The Noise Figure System consists of a Noise Figure meter, a downconverting mixer, and a RF Source as a LO. The adaptation of Friis’ Formula to the Noise Measurement System is seen in Fig. VIII.9.

The noise source is an avalanche diode which in its off-state is open and in its on-state is a short circuit noise source. Typically the source is measured directly at the Noise Figure System to account for the noise of the system and source. The system consists of the amplifiers, mixers, local oscillator, and Noise
Figure VIII.8: Block Diagram of Noise Measurement System.

Figure VIII.9: Simplified Noise Measurement Schematic, [5].
Figure meter [5]. The gain of the DUT is measured directly via a VNA for Available Gain to correct the Insertion Gain used in Friis’ formula for calculating cascaded Noise Factor VIII.1. Friis’ formula presented here is truncated. Insertion Gain is the measure of power delivered to a load or measurement receiver from a source divided by the power delivered to the receiver or load without the DUT in between the receiver and source. Independent Available Gain measurement of the DUT from the VNA is necessary because the Noise Figure Meter is designed to measure Noise Figure and Insertion Gain. Friis’ formula requires Available Gain, thus the Available Gain measure must be available to an independent computer beyond the CPU of the Noise Figure System to correctly calculate the Noise Figure as a function of source impedance. The Focus Noise Measurement System accomplishes this function by combining the function of the AT Noise Measurement System, the VNA, the source tuner, the microwave circuit elements to create a DUT based value of Noise Figure and Available Gain drawn on a Smith chart.

\[ F_1 = F_{12} - \frac{F_2 - 1}{G_1} \]  

(VIII.1)

A sample graph of the output of the Noise Figure System is shown in Fig.VIII.12. The features of this source-side Smith chart are composed of constant Available Gain and Noise Figure circles, and a Stability circle. The red circles represent constant Available Gain with a maximum of 9.89 dB at \(|\Gamma_s| = 0.632\) and \(\angle \Gamma = 43.1^\circ\). The blue circles represent constant Noise Figure with a min-
Figure VIII.10: Noise Figure Measurement Test System.

Figure VIII.11: Noise Figure Measurement Test System.
Figure VIII.12: Noise Figure Measurement showing Noise and Available Gain Circles.

imum of 2.41 dB at $|\Gamma_s| = 0.323$ and $\angle\Gamma=37.8^\circ$. The green circle represents the Stability circle for this measurement.

This concludes the Noise Figure Measurement System discussion. This system is capable of representing the magnitude and position of the Available Gain and Noise Factor as function of source impedance termination. The accuracy is better than 0.1 dB in Noise Factor at 5.0 GHz.
VIII.5 Summary

In this chapter we reviewed the DOE’s developed and discussed in prior chapters. We reviewed the measurement methods to obtain the results presented in Chapter IX: Experimental Verification of Theory. We discussed the Large-signal and Small-signal measurement systems and how they functioned. We discussed the many capabilities of these systems to collect and process I-V, S-parameter, RF Load-pull, and Noise Figure data into CMOS model parameters, Gain, and Noise Figure results amongst many others. These systems comprise a significant tool into research on RF integrated circuits.

The text of this chapter, in part, is a reprint of the material as it appears in our papers in *IEEE Conferences or Transactions on Microwave Theory and Techniques*. The dissertation author was the primary investigator and primary author of these papers.
Chapter IX

Experimental Verification of Theory

IX.1 Introduction to Experimental Verification

In this chapter, we discuss in detail the results predicted in Chapters III: Device Modelling, IV: Linearity Analysis of MOSFET’s, V: Noise Analysis of CMOS FET’s, VI: Optimum Design for CMOS RF Amplifiers, and VII: LNA Design. In Chapter VIII: Laboratory Experiment and Test Engineering, the methods of obtaining results from the theoretical predictions were reviewed.

IX.2 Device Modelling Results

In this section, the results of device modelling are reviewed. We first review the active devices results for CMOS, SOS, and HBT. Next, we review the passive devices results.
Table IX.1: Measured CMOS N-channel devices of L=0.35\,\mu m Large-Signal Linear Parameters at VDS=1.5V

<table>
<thead>
<tr>
<th>Width $\mu$m</th>
<th>$V_t$ V</th>
<th>Peak $g_m$ mS</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>0.698</td>
<td>11.3</td>
</tr>
<tr>
<td>130</td>
<td>0.705</td>
<td>29.2</td>
</tr>
<tr>
<td>200</td>
<td>0.694</td>
<td>44.7</td>
</tr>
<tr>
<td>520</td>
<td>0.639</td>
<td>84.5</td>
</tr>
</tbody>
</table>

IX.2.1 Active Device Modelling Results

The active device modelling results consist of results from Chapter III: Device Modelling. These results were obtained from I-V curves and S-parameters.

CMOS Modelling Results

The large signal modelling of the I-V characteristics is displayed in Table IX.1. The $V_t$ is relatively consistent across geometry which is expected as a function of the wafer fabrication process. The transconductance, $g_m$, should however scale with increasing gate width. This trend is realized with exception of the N520\,\mu m where the expected value is 115 mS instead of the measured value of 84.5 mS, in part because of not driving the gate of a large transistor from both ends, or more simply a layout error. The results were obtained from the MOSIS HP 0.35\,\mu m wafer fabrication process.

The results of the $g_o$ modelling also show a trend following gate width, again with exception to the N520\,\mu m. The $g_o$ is derived by differentiation of I-V curves over a limited $V_{DS}$, around $V_{DS} = 1.5$ V.
Table IX.2: CMOS N-channel devices of L=0.35\mu m Large-Signal Saturation Parameters at VDS=1.5V

<table>
<thead>
<tr>
<th>Width  ( \mu m )</th>
<th>( g_o ) mS</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>1.10</td>
</tr>
<tr>
<td>130</td>
<td>4.24</td>
</tr>
<tr>
<td>200</td>
<td>4.00</td>
</tr>
<tr>
<td>520</td>
<td>29.4</td>
</tr>
</tbody>
</table>

Table IX.3: Measured 5.0 GHz CMOS Scattering Parameters at -25.0 dBm

| Trans. bias | \(|S_{11}\)| | \(\angle S_{11}\) | \(|S_{21}\)| | \(\angle S_{21}\) | \(|S_{12}\)| | \(\angle S_{12}\) | \(|S_{22}\)| | \(\angle S_{22}\) |
|-------------|-------------|----------------|-------------|----------------|-------------|----------------|-------------|----------------|
| N50,B1      | 0.957       | -13.11         | 1.04        | 164.22         | 0.054        | 77.65          | 0.9113      | -13.18         |
| N50,B2      | 0.936       | -15.02         | 1.22        | 163.16         | 0.065        | 74.68          | 0.8719      | -15.36         |
| N130,B1     | 0.893       | -39.22         | 2.39        | 147.33         | 0.122        | 52.13          | 0.787       | -40.29         |
| N130,B2     | 0.839       | -46.4          | 2.67        | 144.0          | 0.138        | 45.5           | 0.70        | -50.5          |
| N200,B1     | 0.780       | -65.31         | 3.08        | 129.75         | 0.15         | 26.252         | 0.68        | -72.05         |
| N200,B2     | 0.695       | -77.29         | 3.13        | 125.21         | 0.161        | 17.23          | 0.62        | -90.34         |

The operating region of interest in the MOSFET is the saturation region and the bias on the transistors evaluated is \( V_{ds} = 1.5V \) and \( v_{GS} = 1.0 \) and \( 1.5V \) + small-signal \( \text{rf} = 22.5 \text{ mV} \). The results of the characterizing of the CMOS transistors at the biases described above for S-parameters is given in Table IX.3.

The B1 represents the \( V_{GS} \) of 1.0 V and the B2 represents the \( V_{GS} \) of 1.5 V. The \( V_{DS} \) is 1.5 V in both cases. These S-parameter results are not predicted in advance. The results shown have been used widely to determine matching, Power Gain, linearity, and NF, amongst others and have been discussed in Chapter VI: Optimum Design for CMOS RF Amplifiers. The forward transmission, \( S_{21} \),
increases with increasing device gate width parallel to the increasing $g_m$ seen in III.2. The reverse transmittance, $S_{12}$, varies from 0.05 to about 0.16 and gives rise to the idealization of the CMOS amplifier being taken largely as a unilateral Power Gain amplifier. The reflection coefficients, $S_{11}$ and $S_{22}$, vary from 0.6 to 0.9 indicate that the input and output ports are not perfectly matched to the $Z_o$ value of 50 $\Omega$. The consequence of this fact was examined in Chapter VI.

The modeling of the 3rd-order polynomial expansion of the linear I-V curve is shown in Table IX.4. The transconductance values for the CMOS FET’s were extracted from the derivative of linear I-V curves at $g_m$’s maximum value. The transconductance values for the modelled results were extracted from a 3rd order polynomial fit. The large-signal value of the fit is the $a_0$ from the modelled I-V curve of the MOSFET. Table IX.5 shows the following differences in percentage upon comparison to the measured results. The error from the large-signal model to measured transconductance results is on average 17.1 percent. Since the $a_0$ term is not used in modelling the small-signal behavior, its an estimate of the measured transconductance value from polynomial extraction and serves as a check
Table IX.5: Transconductance, $g_m$ Differences Measured v. Modelled

<table>
<thead>
<tr>
<th>NMOS</th>
<th>$a_0(m)$, modelled</th>
<th>$a_0(m)$, measured,</th>
<th>PercentDiff.</th>
</tr>
</thead>
<tbody>
<tr>
<td>N50</td>
<td>9.2</td>
<td>11.3</td>
<td>18.5</td>
</tr>
<tr>
<td>N130</td>
<td>24.9</td>
<td>29.2</td>
<td>14.7</td>
</tr>
<tr>
<td>N200</td>
<td>38.5</td>
<td>44.7</td>
<td>13.9</td>
</tr>
<tr>
<td>N520</td>
<td>102.5</td>
<td>84.5</td>
<td>21.3</td>
</tr>
</tbody>
</table>

Table IX.6: Extracted Polynomial Output Conductance, $g_o$, Fit to Measured Data at $V_{DS}$=1.5V, $V_{GS}$=1.0V

<table>
<thead>
<tr>
<th>NMOS</th>
<th>$g_0(m)$</th>
<th>$g_1(m)$</th>
<th>$g_2(m)$</th>
<th>$g_3(m)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>N50</td>
<td>1.1</td>
<td>-3.5</td>
<td>2.2</td>
<td>-0.7</td>
</tr>
<tr>
<td>N130</td>
<td>4.2</td>
<td>-7.0</td>
<td>3.2</td>
<td>-50.5</td>
</tr>
<tr>
<td>N200</td>
<td>4.0</td>
<td>-4.8</td>
<td>7.2</td>
<td>270.9</td>
</tr>
<tr>
<td>N520</td>
<td>29.4</td>
<td>-16.4</td>
<td>52.4</td>
<td>424.2</td>
</tr>
</tbody>
</table>

for consistency in the modelling.

The Table IX.5 shows a difference in the measured and modelled values of $a_o$ because the peak value of $g_m$ from measurement occurs at other than the prediction of the $a_o$ value from the model $g_m$ whose polynomial extraction is optimized at $V_{DS}$=1.5V.

The results in Table IX.6 show the modelling of the output conductance. The large-signal output conductance was produced by taking the derivative of the I-V data around $V_{DS}$=1.5 V. The small-signal values were acquired by modelling the I-V data with polynomial expansion.

In Table IX.7, the Output Capacitance is modelled. The large-signal values were acquired by device modelling of the S-parameters, with one exception for
Table IX.7: Output Capacitance, $c_{DS}$

<table>
<thead>
<tr>
<th>NMOS</th>
<th>$c_0(f)$</th>
<th>$c_1(f)$</th>
<th>$c_2(f)$</th>
<th>$c_3(f)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>N50</td>
<td>21.7</td>
<td>-15.6</td>
<td>91.1</td>
<td>5.3</td>
</tr>
<tr>
<td>N130</td>
<td>83.1</td>
<td>-40.7</td>
<td>236.9</td>
<td>13.7</td>
</tr>
<tr>
<td>N200</td>
<td>100.0</td>
<td>-62.6</td>
<td>364.4</td>
<td>21.1</td>
</tr>
<tr>
<td>N520</td>
<td>207.0*</td>
<td>-162.8</td>
<td>947.5</td>
<td>424.2</td>
</tr>
</tbody>
</table>

Table IX.8: Output Capacitance, $C_{DS}$ Differences Measured v. Modelled

| NMOS | $c_0(f)$, modelled | $c_0(f)$, measured, | $|Diff|$ |
|------|-------------------|---------------------|--------|
| N50  | 19.9              | 21.7                | 1.8    |
| N130 | 51.7              | 83.1                | 31.4   |
| N200 | 79.6              | 100.0               | 20.4   |
| N520 | 207.0             |                      |        |

the N520$\mu$m which was determined from process data because no S-parameters were acquired. The small-signal values come from polynomial expansion of the $c_{DS}$ vs. $v_{DS}$ curves. The comparison of predicted vs. measured $c_{DS}$ performance is shown in Table IX.8. The agreement is reasonable, given that the modelled data is based on process estimates. The measured values are derived from deembedded S-parameter data, which is then modelled to produce $c_{DS}$. In Table IX.9, the modelling of gate-source capacitance is shown. The large-signal values are taken from BSIM3v3 models. The small-signal values are derived from polynomial fitting of the measured large-signal capacitance vs. voltage curves. The capacitance small-signal values were used in linearity modelling described in Chapter IV: Linearity Analysis of MOSFET’s. Table IX.10 compares the modelled vs. measured large-signal input gate-source capacitance. The differences are reasonable given
Table IX.9: Input Capacitance, $c_{GS}$

<table>
<thead>
<tr>
<th>NMOS</th>
<th>$c_{g0}(f)$</th>
<th>$c_{g1}(f)$</th>
<th>$c_{g2}(f)$</th>
<th>$c_{g3}(f)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>N50</td>
<td>50.9</td>
<td>15.2</td>
<td>-52.0</td>
<td>41.8</td>
</tr>
<tr>
<td>N130</td>
<td>132.7</td>
<td>42.9</td>
<td>141.8</td>
<td>110.8</td>
</tr>
<tr>
<td>N200</td>
<td>204.3</td>
<td>-491.0</td>
<td>628.0</td>
<td>632.0</td>
</tr>
<tr>
<td>N520</td>
<td>681.3</td>
<td>169.5</td>
<td>564.0</td>
<td>442.0</td>
</tr>
</tbody>
</table>

Table IX.10: Input Capacitance, $C_{GS}$ Differences Measured v. Modelled

<table>
<thead>
<tr>
<th>NMOS</th>
<th>$c_{G0}(f), \text{modelled}$</th>
<th>$c_{G0}(f), \text{measured}$</th>
<th>$\text{Diff.}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>N50</td>
<td>50.9</td>
<td>44.6</td>
<td>6.3</td>
</tr>
<tr>
<td>N130</td>
<td>132.7</td>
<td>103.2</td>
<td>29.5</td>
</tr>
<tr>
<td>N200</td>
<td>204.3</td>
<td>206.7</td>
<td>2.4</td>
</tr>
<tr>
<td>N520</td>
<td>681.3</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

that the modelled values are based on process estimates. The measured values are based on deembedded S-parameter values, which are then modelled to determine the capacitance.

This concludes our review of results obtained from the CMOS modelling of Chapter III: Device Modelling. The RF parameters were modelled through polynomial expansion for small-signal predictions, largely for linearity, were previously reviewed in Chapter III. We reviewed here the predicted parameters from device physics and physical process data against measured large and small signal values; namely, I-V and S-parameter data. The results agreed well with estimates from process data.
Table IX.11: Large-Signal Peregrine SOS Device Performance

<table>
<thead>
<tr>
<th>SOS</th>
<th>(V_{DS} = 0.2 \text{ V})</th>
<th>(V_{T} \text{mV, Meas.})</th>
<th>(\text{Peakg}_{mS, Meas.})</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN 500x0.5</td>
<td>0</td>
<td>-43.4</td>
<td>23.5</td>
</tr>
<tr>
<td>IP 500x0.5</td>
<td>0</td>
<td>-100.0</td>
<td>10.4</td>
</tr>
<tr>
<td>IN 250x0.5</td>
<td>0</td>
<td>-39.2</td>
<td>11.4</td>
</tr>
<tr>
<td>IP 250x0.5</td>
<td>0</td>
<td>-103</td>
<td>4.51</td>
</tr>
<tr>
<td>NL 500x0.5</td>
<td>0.3</td>
<td>283</td>
<td>19.9</td>
</tr>
<tr>
<td>PL 500x0.5</td>
<td>-0.3</td>
<td>-332</td>
<td>9.15</td>
</tr>
<tr>
<td>NL 250x0.5</td>
<td>0.3</td>
<td>274</td>
<td>9.13</td>
</tr>
<tr>
<td>RN 500x0.5</td>
<td>0.8</td>
<td>801</td>
<td>12.5</td>
</tr>
<tr>
<td>RP 500x0.5</td>
<td>-0.8</td>
<td>-691</td>
<td>7.21</td>
</tr>
</tbody>
</table>

Table IX.12: Peregrine SOS S-Parameters at 1.9 GHz

<table>
<thead>
<tr>
<th>SOS</th>
<th>(S_{11})</th>
<th>(S_{21})</th>
<th>(S_{12})</th>
<th>(S_{22})</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN 500x0.5</td>
<td>0.882</td>
<td>0.005</td>
<td>0.005</td>
<td>0.755</td>
</tr>
<tr>
<td>NL 500x0.5</td>
<td>0.817</td>
<td>3.398</td>
<td>0.114</td>
<td>0.392</td>
</tr>
<tr>
<td>RN 500x0.5</td>
<td>0.874</td>
<td>1.902</td>
<td>0.139</td>
<td>0.697</td>
</tr>
</tbody>
</table>

SOS Transistor Test Results

Devices from Peregrine Semiconductor Corporation were tested for large-signal, S-parameters, and RF gain and linearity performance. The large-signal performance of a sample of the SOS devices supplied to the Center for Wireless Communications at UCSD is shown in Table IX.11.

In Table IX.11, the large-signal performance test results are shown for several types of SOS FET’s. Table IX.12 shows the S-parameter performance of three SOS FET’s. Based on these results, only the NL FET was measured for Power Gain and Linearity. The Fig. IX.1 shows the Load-pull Gain Contour of the NL
Load-Pull Contour of Gain in Peregrine SOS NL500um by 0.5um

\( F=1.80 \text{ GHz}, \; \text{at} \; I_d=10\text{mA}, \; V_d=1.5\text{V} \)

GAIN Max=13.44 dB at 6.8+j6.1, RFIC ECE UCSD
J. S. Fairbanks, L.E. Larson

Figure IX.1: SOS Gain Load-pull Contour.
Table IX.13: Measured Peregrine SOS RF Parameters at 1.9 GHz and $V_{ds}=1.5V$

<table>
<thead>
<tr>
<th>SOS</th>
<th>Gain, $dB$</th>
<th>$III P_3$, dBm</th>
<th>$OII P_3$, dBm</th>
</tr>
</thead>
<tbody>
<tr>
<td>NL 500x0.5</td>
<td>13.44</td>
<td>9.31</td>
<td>22.75</td>
</tr>
</tbody>
</table>

SOS FET. The Fig. IX.2 shows the Load-pull $III P_3$ Contour of NL SOS FET. The intermodulation can also be shown in terms of the output intermodulation intercept point, $OII P_3$ as seen in Fig. IX.3. The Smith chart of Load-Pull of $OII P_3$ for the NL SOS FET is seen in Fig.IX.4. The Smith chart of Load-pull of $III P_3$ for NL SOS FET is seen in Fig. IX.5 The Smith chart of Load-Pull for NL SOS FET is seen in Fig.IX.6. Table IX.13 shows the summary of compara-
Contour Load-Pull Output Third-Order Intermodulation Intercept Point
Peregrine SOS, $F=1.9$ GHz, $I_d=10$ mA, $V_d=1.5$ V, $P_{in}=-17.85$ dBm

$OIP_3$ Max=20.48 dB at 15.2+j12.9, Source Impedance=91.75-91.32j
NL500um by 0.5um, RFIC ECE UCSD, JSF

Figure IX.3: SOS $OIP_3$ Load-pull Contour.
Figure IX.4: SOS $OIIIP_3$ Load-pull.
Load-Pull of Third Order Intermodulation Intercept Point
F=1.90 GHz, NL500um by 0.5um at Id=10mA, Vd=1.5V

IIP3 Max=9.31 dB at 21.7+j17.1, RFIC ECE UCSD
JSF

Figure IX.5: SOS IIP3 Load-pull.
Load-Pull of Gain in Peregrine SOS NL500um by 0.5um
F=1.90 GHz, at Id=10mA, Vd=1.5V

GAIN Max=13.44 dB at 6.8+j6.1j, RFIC ECE UCSD
JSF

Figure IX.6: SOS Gain Load-pull.


tive performance of the SOS FET for Power Gain, $IIIP_3$, and $OIIP_3$. The SOS performance is comparable to bulk in gain and $IIIP_3$.

**HBT Measurement Results**

SiGe HBT’s acquired from Auburn University were measured for large-signal, S-parameter, and RF performance. The DOE consisted of 5 process variations in the HBT. The study was designed to determine the suitability of HBT’s for RF applications. The results of the RF performance in Power Gain and $IIIP_3$ are shown in Fig.’s IX.7, IX.8, IX.9, IX.10, IX.11, IX.12, and IX.13. They represent performance of the Silicon control process (POR) and a 0.14 SiGe base mixture.
Figure IX.8: HBT Gain Load-pull.

Table IX.14: RF Parameters of IBM HBT’s at 1.9 GHz.

<table>
<thead>
<tr>
<th>HBT</th>
<th>Gain, $dB$</th>
<th>$I_{III}$, $P_3$</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiGe (POR) 0.5x20x2</td>
<td>17.31</td>
<td>2.81</td>
</tr>
<tr>
<td>SiGe (0.14) 0.5x20x2</td>
<td>19.82</td>
<td>2.89</td>
</tr>
</tbody>
</table>
Figure IX.9: HBT Gain Load-pull.
Figure IX.10: HBT $I_{IP3}$ Load-pull Contour.
Figure IX.11: HBT $I_{IP3}$ Load-pull Contour.
Figure IX.12: HBT Gain Load-pull Contour.
Figure IX.13: HBT Gain Load-pull Contour.
Table IX.15: Design of Experiment II Results: Inductor Performance

<table>
<thead>
<tr>
<th>Shielding</th>
<th>Inductance, nH</th>
<th>Q</th>
<th>Inductance, nH</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Metal 1</td>
<td>3.5</td>
<td>4</td>
<td>1</td>
<td>2.5</td>
</tr>
<tr>
<td>N-well</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Metal 1/N-well</td>
<td>3</td>
<td>4</td>
<td>2</td>
<td>7</td>
</tr>
</tbody>
</table>

Table IX.16: Design of Experiment III Results: Inductor Performance

<table>
<thead>
<tr>
<th>Shielding</th>
<th>7-turn</th>
<th>3-turn</th>
<th>7-turn</th>
<th>3-turn</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate</td>
<td>6.5</td>
<td>1.8</td>
<td>1.9</td>
<td>4.5</td>
</tr>
<tr>
<td>N-well</td>
<td></td>
<td>1.5</td>
<td>1.25</td>
<td></td>
</tr>
<tr>
<td>Fractured N-well</td>
<td>1.5</td>
<td></td>
<td>1.25</td>
<td></td>
</tr>
<tr>
<td>Fractured Poly/N-well</td>
<td>5.25</td>
<td>2.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Fractured Metal 1/N-well</td>
<td>1.5</td>
<td>2.5</td>
<td>1.5</td>
<td>1.25</td>
</tr>
<tr>
<td>Fractured Poly</td>
<td>1.5</td>
<td></td>
<td>1.25</td>
<td></td>
</tr>
<tr>
<td>Fractured Metal 1</td>
<td>9.0</td>
<td>0.1</td>
<td>5</td>
<td>1.0</td>
</tr>
</tbody>
</table>

A summary of the RF performance of the POR and 0.14 SiGe HBT’s is shown in Table IX.14. The similar sized common-emitter amplifier’s had good RF gain and acceptable $IIIP_3$ for application to RF circuit design. The results were published in articles listed at the conclusion of this chapter [51–53].

**IX.2.2 Passive Device Modelling Results**

Since the 3-turn inductor modelling showed little improvement from the different shielding strategies, only two of the 7-turn inductors were measured. The quality factor was uniformly low. The best inductors do not perform well with a lossy substrate. This limitation has performance implications with RF circuit
design. The two high inductances achieved on the 3-turn shielding experiment were the result of lower bias voltages applied to the back-gate and nwell. At low bias voltages an increase in inductance was seen however it vanished at higher bias voltages.

Additionally capacitors from DOE III and transformers from DOE V were measured but the modelling of these results showed poor performance from these passive elements.

**IX.3 Test Results for Linearity Analysis of MOSFET’s—Comparison of Theory and Results**

The CMOS MOSFET’s test results of linearity predictions made in Chapter IV is now reviewed. The results were acquired from Focus Load-pull system described in Chapter VIII.

In Table IX.17, the predictions of linearity versus bias is seen for the N50\(\mu\)m.
Table IX.18: N130\(\mu\)m\(x\)0.35\(\mu\)m Predicted vs. Measured \(III P_3\), dBm at \(V_{DS}=1.5\) V.

| Term. Imped. | \(V_{GS}\) Bias | Predicted | Measured | \(|Diff.\) |
|--------------|-----------------|-----------|-----------|-----------|
| \(T_{130}(1)\) | 1.5 V | 18.03 | 15.43 | 2.6 |
| \(T_{130}(3)\) | 1.5 V | 18.58 | 18.80 | 0.2 |
| \(T_{130}(6)\) | 1.5 V | 15.64 | 15.22 | 0.4 |
| \(T_{130}(7)\) | 1.5 V | 13.40 | 14.27 | 0.9 |

Table IX.19: N200\(\mu\)m\(x\)0.35\(\mu\)m Predicted vs. Measured \(III P_3\) dBm at \(V_{DS}=1.5\) V.

| Term. Imped. | \(V_{GS}\) Bias | Predicted | Measured | \(|Diff.\) |
|--------------|-----------------|-----------|-----------|-----------|
| \(T_{200}(3)\) | 1.5 V | 17.12 | 16.36 | 0.8 |
| \(T_{200}(6)\) | 1.5 V | 11.82 | 12.18 | 0.4 |
| \(T_{200}(8)\) | 1.5 V | 11.64 | 14.67 | 3.0 |
| \(T_{200}(9)\) | 1.5 V | 11.84 | 13.31 | 1.5 |

The modelling is optimized for the \(V_{GS}=1.5\) V bias and also shows consequently the lowest difference on average of 0.9 dBm. The other two biases show higher on average difference in measured vs. predicted values, where the average difference is 2.0 dB at \(V_{GS}=1.1\) V and 3.2 dB at \(V_{GS}=1.3\) V.

In Table IX.18, the comparison of predicted versus measured for the N130\(\mu\)m is seen. The average difference is 1.3 dB, similar to the N50\(\mu\)m device. This shows that the predictions do scale with device geometry. In Table IX.19, the comparison of predicted versus measured for the N200\(\mu\)m is seen. The average difference is 1.9 dB, a little higher than the N130\(\mu\)m case.

In the final comparison, Table IX.20 shows the performance on the linearity
Table IX.20: N520μm×0.35μm Predicted vs. Measured $I_{IIP3}$, dBm at $V_{DS}$=1.5V.

| Term. Imped. | $V_{GS}$ Bias | Predicted | Measured | $|Diff.|$ |
|--------------|-------------|-----------|----------|--------|
| $T_{520}(1)$ | 1.5 V       | 24.80     | 19.39    | 5.41   |

theory on a poorly performing device. The difference is higher than the other three transistor widths but still predicts the linearity performance with fair agreement. The significance of this is that the linearity theory is robust enough to predict a less than optimally behaving transistor.

In summary, the comparison of linearity theory developed for CMOS transistors operating in low-power RF range, shows a very good agreement across transistor geometry, bias conditions, source and load impedance conditions, and input signal levels. This shows that the linearity theory developed in Chapter IV: Linearity Theory is robust and has wide theoretical predictive capability.

### IX.4 Test Results for Noise Analysis of CMOS FET’s

The measured results for NF and $\Gamma_{opt}$ are presented in the following tables for comparison to the predicted results in Chapter V: Noise Analysis of CMOS FET's. The data was acquired using the Focus Source-pull Noise System described in the Chapter VIII: Laboratory Experiment and Test Engineering. In Table IX.21, the performance of the NF theory can be seen. The prediction is across bias with an difference of less than 0.9 dB in NF. The difference in $\Gamma_{opt}$
Table IX.21: N50\(\mu\)m Two-Port NF Prediction vs. Measured at \(V_{DS}=1.5\) V

<table>
<thead>
<tr>
<th>Parameter</th>
<th>(V_{gs}=1.5) V</th>
<th>(V_{gs}=1.0) V</th>
<th>Diff.</th>
</tr>
</thead>
<tbody>
<tr>
<td>(N F(dB))</td>
<td>1.71</td>
<td>1.3</td>
<td>1.78</td>
</tr>
<tr>
<td>(r(\Gamma_{opt})(fb))</td>
<td>0.88</td>
<td>0.8</td>
<td>0.83</td>
</tr>
<tr>
<td>(\theta(\Gamma_{opt})(fb))</td>
<td>18.4</td>
<td>20.0</td>
<td>27.8</td>
</tr>
</tbody>
</table>

Table IX.22: N130\(\mu\)m Two-Port NF Prediction vs. Measured at \(V_{DS}=1.5\) V

<table>
<thead>
<tr>
<th>Parameter</th>
<th>(V_{gs}=1.5) V</th>
<th>(V_{gs}=1.0) V</th>
<th>Diff.</th>
</tr>
</thead>
<tbody>
<tr>
<td>(N F(dB))</td>
<td>1.19</td>
<td>1.9</td>
<td>1.12</td>
</tr>
<tr>
<td>(r(\Gamma_{opt})(fb))</td>
<td>0.79</td>
<td>0.8</td>
<td>0.77</td>
</tr>
<tr>
<td>(\theta(\Gamma_{opt})(fb))</td>
<td>35.4</td>
<td>43.7</td>
<td>40.0</td>
</tr>
</tbody>
</table>

predicted vs. measured is small at both biases for the N50\(\mu\)m MOSFET. In Table IX.22, the NF theory performance is again viewed for the N130\(\mu\)m MOSFET. The prediction of the NF theory has a difference of less than 0.75 dB and less 9.0 degrees in \(\Gamma_{opt}\). This result shows that the NF theory predictions scale across MOSFET geometry as well. In the final table for this section, the NF predictions of the N200\(\mu\)m MOSFET are seen. The difference is NF is less than 0.45 dB and magnitude of \(\Gamma_{opt}\) is less than 0.15, while the difference in angle of \(\Gamma_{opt}\) is less than 28 degrees. In summary, the NF theory predicted well the NF performance

Table IX.23: N200\(\mu\)m Two-Port NF Prediction vs. Measured at \(V_{DS}=1.5\) V

<table>
<thead>
<tr>
<th>Parameter</th>
<th>(V_{gs}=1.5) V</th>
<th>(V_{gs}=1.0) V</th>
<th>Diff.</th>
</tr>
</thead>
<tbody>
<tr>
<td>(N F(dB))</td>
<td>2.25</td>
<td>2.3</td>
<td>2.15</td>
</tr>
<tr>
<td>(r(\Gamma_{opt})(fb))</td>
<td>0.69</td>
<td>0.54</td>
<td>0.72</td>
</tr>
<tr>
<td>(\theta(\Gamma_{opt})(fb))</td>
<td>69.7</td>
<td>65.2</td>
<td>56.4</td>
</tr>
</tbody>
</table>
of three MOSFET’s. This results shows that a careful application of the NF theory can yield very good predictions across geometry and bias choices.

IX.5 RF CMOS Amplifier Design Optimization Results

The strategy to design an optimum RF CMOS amplifier will depend on the understanding of the system requirements, described in Chapter I: Introduction and System Architecture, the device modelling, described in Chapter III: Device Modelling, and the RF modelling of each attribute of interest, such as Power Gain, Noise Figure, or linearity, described in Chapters III, IV, and V. The purpose of this next section is to review the optimum performance in RF characteristics as a function of current density in the active common-source amplifier and its interaction with impedance match tuning. The results shown in this section are from the Focus Microwaves Load-pull System tests and represent optima, from many (hundreds of) different tests, of each amplifier. The system implications of the RF performance of each amplifier were discussed in Chapter VI: Optimum Design for CMOS RF Amplifiers.

The maxima of Power Gain, $IIIP_3$, and the minima of Noise Figure for all MOSFET’s as a function of tuning and constrained power consumption are seen in the following Figs. IX.14 through IX.21. The stability circles are also shown for both sides of the amplifier. The significance of these Source- and Load-pull Smith
charts is that the optimum choice for each RF parameter is different in many ways. The impedance match tuning strongly affects the optimum choice for Power Gain, NF, and $IIIP_3$ but also as the current density changes the device characteristics such that the optimum impedance match tuning around the Smith chart changes. Thus, it will become evident that the desire to achieve an optimum performance, dictated by a system requirement, of an RF CMOS amplifier is a somewhat more difficult task to achieve, as described in Chapter VI: Optimum Design for CMOS RF Amplifiers for SFDR.

Starting with the N50 $\mu$m x 0.35$\mu$m grounded-source amplifier, the load side is shown in Fig. IX.14 and the source side is shown in Fig. IX.15. On the load side, the maxima of Power Gain, ranging from 4.2 dB to 8.7 dB, as a function of current density at 5.0 GHz occur in the low impedance capacitive range well away from instability on the load side. The maxima of $IIIP_3$, ranging from 7.6 to 15.9 dB, occur about 180 degrees away from the maxima of Power Gain as function of current density and in the inductive area of the Smith chart. However the $IIIP_3$ is not simply represented by the position of the maximum found in Load-pull from the fundamental frequency. $IIIP_3$ also depends on the second and third harmonic impedance match tuning as well, $(2\omega, 3\omega)$.

On the source side of the N50 $\mu$m x 0.35$\mu$m grounded-source amplifier, the maxima of Power Gain, ranges from 4.2 to 8.6 dB, and occurs in the very low impedance capacitive range also. The maxima of $IIIP_3$ occur about 180 degrees
Stability Circles at $V_{GS} = 1.0 \& 1.5$ V

Max. Gain = 7.9 dB, $J = 210$ A/$\mu$m

Max. Gain = 8.7 dB, $J = 175$ A/$\mu$m

Max. Gain = 7.7 dB, $J = 70$ A/$\mu$m

Max. Gain = 4.9 dB, $J = 35$ A/$\mu$m

Max. Gain = 6.7 dB, $J = 140$ A/$\mu$m

$IIIP_3 = 7.6$ dB, $J = 35$ A/$\mu$m

$IIIP_3 = 15.2$ dB, $J = 175$ A/$\mu$m

$IIIP_3 = 10.0$ dB, $J = 70$ A/$\mu$m

Figure IX.14: N50$\mu$m x 0.35$\mu$m Maximum Gain and Maximum $IIIP_3$ vs. Current Density, Load Side Tuning.
away in the real and inductive range of higher impedance. The minima of Noise Figure, ranges from 0.9 to 3.6 dB and occurs in the higher impedance inductive range, as seen in Fig. IX.15. As is seen in the the Figures for the N50\(\mu\)m x 0.35\(\mu\)m grounded-source amplifier, the maxima of Power Gain, \(III P_3\), and the minima of Noise Figure do not fall at the same locations on the Smith chart; thus, trade-offs must be made to effect the best performance over many RF attributes relative to system requirements.

On the load side for the N50\(\mu\)m x 0.35\(\mu\)m, the maxima of Power Gain,
ranging from 7.2 dB to 12.5 dB, as a function of current density at 5.0 GHz occur in the low impedance capacitive range, well away from instability on the load side. The maxima of $IIP_3$, ranging from 13.2 to 15.4 dB, occur about 180 degrees away from the maxima of Power Gain as function of current density and in the inductive area of the Smith chart. The source side of N200μm x 0.35μm grounded-source amplifier in Fig IX.17, the maxima of Power Gain as a function of current density occur in the low impedance capacitive range again. The maxima
Gain = 12.8, 12.4, 12.3, & 11.6 dB

J = 35, 70, 105, & 140 A/\mu m

NF = 3.72 dB, J = 70 A/\mu m

NF = 4.9 dB, J = 175 A/\mu m

NF = 5.8 dB, J = 140 A/\mu m

NF = 4.89 dB, J = 35 A/\mu m

Figure IX.17: N200\mu m x 0.35\mu m Maximum $IIIP_3$, Gain and Minimum Noise Figure vs. Current Density, Source Side Tuning.

of $IIIP_3$ occur in the inductive range about 180 degrees away from the maxima of gain. On the source side the minima of Noise Figure, ranging from 2.0 to 5.8 dB, is also present which are also present and in the high impedance inductive range inside the stability circle. Thus, some increase in Noise Figure will be required to achieve acceptable stable Power Gain as a trade-off because the optimum values for Power Gain and Noise Figure are well apart on the Smith chart. Likewise
Figure IX.18: N130 Power Gain and $IIIP_3$, Load Side Tuning.

for $IIIP_3$, the optimum value is not where the optima for Power Gain and Noise Figure occur.

On the load-side of the 26 gate-fingered N130$\mu$m x 0.35$\mu$m grounded-source amplifier is seen in Fig IX.18. The Power Gain maxima as a function of current density, ranges from 7.5 to 10 dB, occurs again in the low impedance capacitive range. The $IIIP_3$ maxima, as a function of current density, are spread and occur at more than 180 degrees from the Transducer Gain maxima. On the
source side of the N130μm x 0.35μm grounded-source amplifier as seen in Fig IX.19, the Power Gain maxima, ranging from 7.4 to 9.5 dB, as function of current density lie in the low impedance capacitive range. The $I_{IP3}$ maxima, ranging from 9.2 to 16.4 dB, lie 180 degree away in the high impedance inductive range. The Noise Figure minima, ranging from 0.9 to 2.9 dB, lie in the high impedance inductive range. Again the optima loci for each RF attribute exits at different locations; thus, trade-offs must be made against each of the other attributes as part of required design choices. In the final grounded-source amplifier, the N520μm x 0.35μm, is seen in Fig IX.20, the load side has the Power Gain maxima and ranges from 5.0 to 9.8 dB as a function of current density, lying in the high impedance capacitive range. The $I_{IP3}$ maxima, ranges from 5.0 to 9.8 dB and lies in the high impedance capacitive range. Neither optima loci occur simultaneously; thus, in a practical design trade-offs will be required. On the source side of the N520 grounded-source amplifier, is seen in Fig IX.21, the Power Gain maxima, ranges from 4.9 dB to 7.0 dB as function of current density and lies in the high impedance capacitive range. The $I_{IP3}$ maxima, ranging from 17.8 to 24.8 dB as a function of current density, lie in the lower impedance inductive range. The Noise Figure minima, ranging from 7.6 to 11.1 dB as a function of current density, lie in the high impedance inductive range. All RF optima lie at different loci; so that, trade offs will also be required to make a practical design. This MOSFET has high noise relative to the other three. In summary, the four grounded-source amplifiers
Figure IX.19: N130 Maximum Gain, $III\bar{P}_3$, and Minimum Noise Figure vs. Current Density, Source Side Tuning.
Figure IX.20: N520 Maximum Gain and $IIIP_3$ vs. Current Density, Load Side Tuning.
Figure IX.21: N520 Maximum Gain, $III_P^3$, and Minimum NF vs. Current Density, Source Side Tuning.
have been shown to have loci for optima in three RF design attributes; namely, Power Gain, $I_{III}^3$, and minimum Noise Figure, which are in different locations for different current densities. This fact requires the compromising of two other RF attributes to the benefit of one. These trade-offs are necessary in order to accomplish a practical optimum RF amplifier design.

**IX.6 LNA Design Results**

In Chapter VII: LNA Design, the ISM band 5 GHz LNA design was discussed. Here we review the results of the design. In Fig. IX.22, the results of the performance of the 5.0 GHz ISM LNA is seen. The 26.0 GHz design is still under study at the time of writing. The preliminary results show a gain on this LNA of about 3.0 dB best case. The reduced gain value is partly the result of a layout error, and will not be further discussed here. The NF shows an approximately classical behavior with current density change. The $I_{III}^3$ raises with current and then falls at high current, again in a nearly classical behavior for linearity. The rise in linearity at low bias, is a result of the lessened gain at low current, which does not amplify the fundamental Power Gain relative to the third-order intermodulation. This region at low current is not exploitable for the higher linearity because the gain is low, and therefore not useful. The Power Gain follows a similar trend for a change in current density.

The comparative performance of the ISM LNA is seen in Table IX.24. The
Figure IX.22: 5.0 GHz CMOS LNA Test Results
LNA design goals were exceeded in Supply Voltage, NF, $I_{IP_3}$, power consumption, and FOM. Only the Power Gain was slightly below desired.

Thus, in summary for the performance achieved, the maximum Power Gain is 9.0 dB and the minimum NF is 3.0 dB. The maximum $I_{IP_3}$ is 6.0 dBm. Comparative performance is seen in Table IX.25. The linearity figure of merit, (FOM), $[I_{IP_3}(dBm)-P_{dc}(dBm)-NF(dB)]$, is one of the best ever reported for a CMOS LNA in this frequency range. This linearity FOM is about 1 to 3 dB better than an exact simultaneous values of performance at a given current because the best values were used independent of current, thus introducing a small absolute error. Certainly, if the performance behavior for the relevant parameters in the linearity FOM were known from the other researchers, then an exact computation for each researcher's publication could have been made. However, this was not the case, as can be seen from Table IX.24. Thus, the assumption used, for computation purposes, was that the performance values reported to make the linearity FOM calculation, were the best achieved performance parameters independent of cur-
Table IX.25: 5.0 GHz CMOS LNA Performance Comparison

<table>
<thead>
<tr>
<th>Reference</th>
<th>[54]</th>
<th>[55]</th>
<th>[56]</th>
<th>[57]</th>
<th>[47]</th>
<th>This Work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency, GHz</td>
<td>5.2</td>
<td>5.8</td>
<td>5.25</td>
<td>5.2</td>
<td>5.2</td>
<td>5.0</td>
</tr>
<tr>
<td>Technology, $\mu m$</td>
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<td>0.25</td>
<td>0.25</td>
<td>0.25</td>
<td>0.35</td>
<td>0.35</td>
</tr>
<tr>
<td>Supply, V</td>
<td>2.0</td>
<td>2.0</td>
<td>3.0</td>
<td>1.5</td>
<td>3.3</td>
<td>2.2</td>
</tr>
<tr>
<td>Power, mW</td>
<td>7.2</td>
<td>20</td>
<td>24</td>
<td>9</td>
<td>26.4</td>
<td>11</td>
</tr>
<tr>
<td>$S_{21}, \text{ dB}$</td>
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<td>14.4</td>
<td>17</td>
<td>19.3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain, dB</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td>9.0</td>
</tr>
<tr>
<td>NF, dB</td>
<td>4.8</td>
<td>3</td>
<td>2.5</td>
<td>2.1</td>
<td>2.45</td>
<td>3.0</td>
</tr>
<tr>
<td>IIIP3, dBm</td>
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<td>-1.5</td>
<td>-6.1</td>
<td>6.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FOM, dB</td>
<td>-14</td>
<td>-17.8</td>
<td>-22.8</td>
<td>-7.4</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

rent from each researcher. In any event, the absolute values would for each case worsen, but not as much the relative values.

In summary, an ISM band LNA was design in a digital CMOS process which exceed all design goals but Power gain. This shows that digital CMOS processes can yield acceptably performing RF LNA circuit designs at 5 GHz for use in WLAN’s. This LNA circuit shows high-linearity, moderate power gain, and reasonable minimum NF for an RF front-end receiver [58].

IX.7 Summary

In conclusion, the device modelling results for large-signal, S-parameter, and small-signal testing have been shown. The results were consistent with physical process data. Three active transistor types: bluk, SOS, and HBT were reviewed for performance in large-signal, S-parameter, and small-signal measurements. The predictions for passive element performance was reviewed and good
agreement was found. The linearity of MOSFET’s was tested against predictions and good agreement was found. The predictions of noise theory were tested also against measurement and good agreement was found. Next, the optimization of RF CMOS amplifiers was examined in light of the trade-offs required to implement a good system receiver architecture. Lastly, the performance of an LNA was checked against goals and simulation results and found to perform well. The overall assessment that could be drawn is that properly developed theory in conjunction simulation and analysis, and expert measurement can be highly successful in achieving system and design goals programmatically with fewer iterations and guesswork.

The text of section two thru six of this chapter, in part, is a reprint of the material as it appears in our papers in IEEE MTTS Radio and Wireless Conference, IEEE MTTS Si RF Workshop, and IEEE Transactions on Electron Devices or Microwave Theory and Techniques. The dissertation author was the primary investigator and primary author of these papers, excepting the last where he was a contributor.
Chapter X

Conclusion

X.1 Research Summary

In summarizing the research presented in this dissertation, the main question has been to answer the central problem of how to improve and optimize CMOS LNA design practices relative to RF system architecture requirements. This question is important regardless of device technology or system requirements. Specifically, extensive theoretical modelling has been developed to predict linearity, Noise Figure (NF), and Spur-Free Dynamic Range (SFDR), amongst others. These RF characteristics are almost always important to the successful and optimal design of RF circuits. Next, the progress achieved in past chapters will be reviewed followed by a look forward at the future direction this research will take both short and longer-term.

In Chapter III: Device Modelling, the mathematical and computer modelling of both active and passive devices was reviewed in preparation for theo-
retical RF predictions and design work presented in later chapters. The use of small-signal data for deriving nonlinear polynomial expansions based on large-signal I-V’s was shown. The small-signal modelling of transistor nonlinearities is the basis for linearity predictions. Predictions were review in Chapter IX: Experimental Verification of Theory and found to be well matched.

In Chapter IV: Linearity Analysis of MOSFET’s, the nonlinear performance of a grounded-source CMOS amplifier operating in the 5 GHz region was analyzed and predicted using a Volterra series analysis. Predictions were made over a broad range of currents, device geometries, and source and load impedances. Although algebraically complex, this technique allowed the researcher to identify the key limiting features of the nonlinear operation of CMOS amplifiers operating in strong inversion, and pick the appropriate bias and terminating impedances to achieve the best performance. The match between prediction and measurement was found to be good in Chapter IX: Experimental Verification of Theory.

In Chapter V: Noise Analysis of CMOS FET’s, a small-signal noise model was developed for 5 GHz CMOS grounded-source amplifiers and used to predict the minimum Noise Figure and $\Gamma_{opt}$ along with other noise model parameters, including feedback. The minimum Noise Figure for MOSFET’s was predicted and measured with the results showing good agreement in Chapter IX: Experimental Verification of Theory.

In Chapter VI: Optimum Design for CMOS RF Amplifiers, the CMOS
transistors, with matching in both the input and output side, formed a grounded-source amplifiers at 5.0 GHz. The SFDR performance was predicted as a function of marginal stability under the condition of minimized power consumption constraint for maximum Power Gain. Tuning of either the input or the output of the grounded-source amplifier must be done in consideration of maintaining amplifier stability over bias and temperature. With an alertness to the regions where stable matching occurs, the RF amplifier’s performance in power Gain, $IIIP_3$, or NF, amongst other RF characteristics as a function of source and load tuning at 5.0 GHz, was chosen for optimal RF performance. The complete sweep of Power Gain, $IIIP_3$, and NF, as a function of current density and matching was reviewed in Chapter IX: Experimental Verification of Theory. These results guide a better understanding of the figure of merit, FOM, called SFDR and its use in optimal RF circuit design. Also, some straightforward guidelines for simultaneously optimizing Noise Figure, linearity, and dynamic range of the monolithic grounded-source MOSFET amplifier for RF low-noise amplifier (LNA), variable gain amplifier (VGA), and mixer applications in a wireless transceiver applications, under the constraint of minimizing dc power dissipation were developed.

In Chapter VII: LNA Design, two designs for LNA application were presented which used two different CMOS and SOS processes. Both designs produced acceptable simulations from two different simulators regarding their design goals, were laid out, fabricated. These simulation predictions further support the
expanded use of CMOS in RF applications in the ISM and millimeter wave bands. Acceptable trade-offs can be made with very good performance at extremely High Frequencies in Gain, Noise Figure, and $\text{IIIP}_3$. The prediction were reviewed in Chapter IX: Experimental Verification of Theory and better than expected performance was achieved on the 5 GHz LNA.

In Chapter IX: Experimental Verification of Theory, the device modelling results for large-signal, S-parameter, and small-signal testing were shown. The results were consistent with physical process data. Three active transistor types: bluk, SOS, and HBT were reviewed for performance in large-signal, S-parameter, and small-signal measurements. The predictions for passive element performance were reviewed and good agreement was found. The linearity of MOSFET’s was tested against predictions and good agreement was found. The predictions of noise theory were tested also against measurement and good agreement was found. Next, the optimization of RF CMOS amplifiers was examined in light of the trade-offs required to implement a good system receiver architecture. Lastly, the performance of an LNA was checked against goals and simulation results and found to perform well for the 5 GHz LNA. The overall assessment that could be drawn is that properly developed theory in conjunction simulation and analysis, and expert measurement can be highly successful in achieving system and design goals programmatically with fewer iterations and guesswork, and thus better RF system performance.
In Chapters I and II, RF system requirements and an ISM receiver design were examined for required performance in Power Gain, NF, and linearity. The estimates of the Gain were made upon simple design models and reported results. Based upon the above estimates, a ISM receiver design using the CMOS transistors in a digital process introduced and studied here was shown to be practical by building and testing a fundamental building block, the grounded-source amplifier.

X.2 Future Research Outlook

The future areas of research not detailed in this dissertation which need to be pursued involve linearity and power gain. Of importance to RF system performance is the reduction of in-band distortion, which cannot be filtered out. While the theory of predictions of non-linear amplifier behavior has been shown to work well, the examination of harmonic \((2\omega, 3\omega)\) tuning for additional improvement in optimization remains to be pursued in RF amplifiers operating under small-signal constraint. Also the manner in which the analytical tools developed to predict linearity in RF amplifiers could be used as a base for developing computer-based prediction tools.

On power gain, the theory that predicts the different types of gain could be expanded to include effects of bias and amplifier tuning. The current models has very limited scope in its predictions and accuracy is highly limited. The goal would be to have a scalable prediction of power gain which is accurate over a
much wider range of conditions and thus more useful as a predictive tool. Once the power theory was improved to include scalability, software tools could be developed that would then improve simulation predictions.

Lastly, a better figure-of-merit could be constructed from FOM’s such as SFDR and linearity, which has scalability and matching included in its predictions. This would assist feasibility predictions at the circuit level for system architecture analyses.
Bibliography


[40] V. Lam et al., “Exact Noise Figure of a Noisy Two-port with Feedback,” *IEE PROCEEDINGS-G*, vol. 139, no. 4, 1992.


