An S-band Low-Noise Amplifier with Self-Adjusting Bias for Improved Power Consumption and Dynamic Range in a Mobile Environment

Wei Xiong[1] and Lawrence E. Larson[2]

[1] Qualcomm Inc., 6455 Lusk Boulevard, San Diego, CA 92121
[2] Center for Wireless Communication, University of California - San Diego, La Jolla, CA 92093

Abstract — **A discrete low-noise amplifier designed to operate in a mobile wireless environment is presented. The amplifier utilizes two cascaded GaAs FETs to achieve 25dB gain and 0.9dB noise figure at 2.5GHz. An active bias control circuitry automatically and continuously adjusts drain-source currents of the FETs to maintain power consumption at 33 milliwatts in nominal small-signal conditions, and to provide elevated input IP3 and reduced noise figure during jamming. A 15dB improvement in input IP3 is achieved in large-signal operation.**

I. INTRODUCTION

With the explosive growth of wireless communications, the airwaves are rapidly being filled with signals of varying strengths and frequencies. Immunity to jamming has subsequently become a significant concern to any communication system. This is especially true for a mobile communication system, such as a cellular phone, as it is difficult to predict the jamming environment the system will be exposed to. At the same time, the need for portability, and thus long battery life, requires the system to consume as little power as possible.

In a typical wireless system, filtering before the low-noise amplifier can reject most of the jammers. However, a high rejection ratio incurs high insertion loss – a direct contributor of receiver sensitivity degradation. In addition, many close-in jammers are impossible to block given the size and cost restrictions of a mobile system. Figure 1 illustrates some of the jammers as measured by an omni-directional 2.5GHz antenna. The low-noise amplifier, therefore, must have a large dynamic range [1] – low noise figure and low intermodulation distortion. To meet these demands, the LNAs often consume the most power in a receiver; tradeoffs are usually required to balance dynamic range versus power consumption. This design circumvents these compromises by optimizing power consumption for the operating environment – a high dynamic range when the LNA is near or in compression, but low power consumption when the LNA is in small-signal operation where a large dynamic range is not necessary.

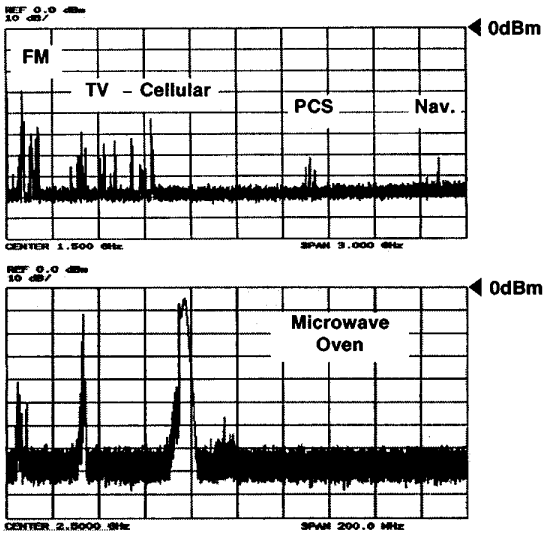

Figure 1. Typical jammers

II. CIRCUIT DESIGN

For input RF power significantly below the compression point, linearity is not a concern as the intermodulation distortion products created by the LNA are negligible. Power consumption and noise figure are the primary considerations. As the input power rises, the intermodulation products increase rapidly. Hence, it is desirable for the LNA's intermodulation intercepts, such as the third-order intercept point (IP3), to increase as the input power increases.

0-7803-5135-5/99/$10.00 © 1999 IEEE

Since linearity generally improves with increasing dc power, improving IP3 on a given device would require higher power consumption. In wireless communication systems, the LNA only occasionally experiences high input power – when a strong jammer is present. Under these circumstances, increasing the supply power to the LNA is a small price to pay to prevent loss of data or dropping the link.

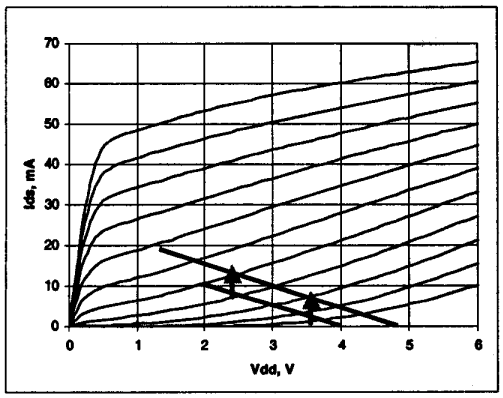

Figure 2. IV characteristics and loadline of the first FET

At first glance, a Class AB amplifier has the ideal prerequisites; the current drawn by the amplifier grows as increasing input power raises the dc bias of the active device [2]. However, in the Class AB region, the device inherently clips once every period, creating undesired non-linearity. In addition, to achieve very low noise figure and high gain, FETs are preferred. Due to variations in saturation drain-source currents (I_{DSS}) and pinch-off voltages (V_P) intrinsic to the devices, the FETs can have vastly different drain-source currents (I_{DS}) for given bias voltages. Active biasing and bootstraping are commonly used to mitigate these and variations over temperature, but both methods prevent the FETs from entering the Class AB region. Without any bias control, the power consumed by the FET becomes unpredictable. This design avoids these undesired properties of FETs and the "Catch 22" situation by actively moving the loadline, as shown in Figure 2, to a higher dc bias point instead of relying on the passive response of Class AB amplifiers.

The basic topology of the design is shown in Figure 3. It comprises three sections – the active devices, the power detector and the bias control. The design employs a two-stage cascaded configuration with a low-noise PHEMT at the input and a hetero-junction FET at the output. Two Schottky diodes in a dual package form the power detector. Diode D_1 performs the detection, while diode D_2 provides temperature compensation [3]. The bias control is composed of two operational amplifier that essentially act as comparators of the drain-source voltages (V_{DS}) and the power detector output voltage (V_{PD}).

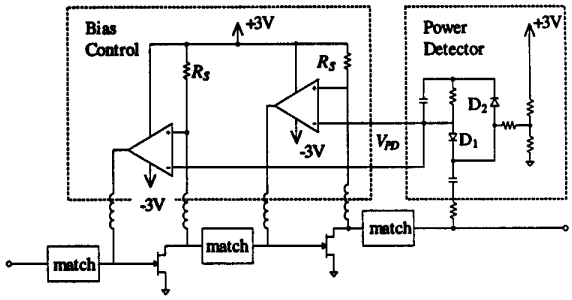

Figure 3. Simplified LNA schematic

Upon power-up, the gate-source voltages (V_{GS}) are initially zero with drain-source currents in saturation. At this moment, the negative inputs of the op-amps are equal to V_{PD} while the positive inputs are equal to

$$V_{DS} = V_{DD} - R_S I_{DS} \qquad (1)$$

$V_{DS} < V_{PD}$ when $I_{DS} = I_{DSS}$, the op-amps therefore provide negative voltages to the gates of the FETs,

$$V_{GS} = A(V_{DS} - V_{PD}) \qquad (2)$$

where A is the gain of the op-amp. Using the large-signal square-law approximation for junction FETs [4],

$$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \qquad (3)$$

the relationship between I_{DS} and V_{PD} is then

$$I_{DS} = I_{DSS}\left[1 - \frac{A(V_{DD} - R_S I_{DS} - V_{PD})}{V_P}\right]^2 \qquad (4)$$

or

$$I_{DS} = \frac{V_P^2 - 2AR_S I_{DSS} V_P + 2A^2 R_S I_{DSS}(V_{DD} - V_{PD})}{2A^2 R_S^2 I_{DSS}} \qquad (5)$$

A square-root term is omitted from Equation 5 as it is four orders of magnitude less than the other terms. I_{DS} is linearly proportional to V_{PD}.

The behavior of the power detector is described by the zero-order Bessel function of the first kind [5]. However, since the diode load resistance is approximately one-half of the input resistance of the op-amp and that the incident RF power into the diode is relatively weak, the simplified square-law relationship between V_{PD} and the LNA output power is sufficiently accurate. The drain-source currents of the FETs therefore response to the input power according to a square law. Steady-state is reached in 0.7 millisecond. This feedback scheme also allows the bias control circuit to automatically compensate for device and temperature variations.

The LNA requires supply voltages of ± 3V. The FETs are designed with a nominal I_{DS} of 5mA each, with an additional 0.8mA required by the op-amps and the diodes. Less than 1mA of total current variation is observed from –30°C to +80°C for a given input RF power. The LNA is also insensitive to device variations in the op-amps and diodes. Components from several manufacturers are used interchangeably with identical results.

In high power conditions, such as in the presence of a strong jammer, Diode D_1 conducts more current, lowering the negative inputs of the op-amps, and thus increasing V_{GS} and I_{DS} of the FETs. The LNA reaches a new steady state with higher dc power and improved linearity.

The power detector bias voltage can be adjusted to alter the steady-state I_{DS} of the FETs. This adjustability offers the versatility of variable I_{DS} under small and large-signal conditions. For example, when the system is near the edge of receiver sensitivity, the symbol error rate may be excessively high. The system can decrease the power detector bias voltage, lowering the output of the power detector and forcing the FET currents to increase. The mechanism is the same as the transition to high input power operation. As the FETs draw more current, noise figure decreases while gain increases, improving the receiver sensitivity. Adjusting the power detector bias can be performed independently or in conjuncture with LNA's automatic response to high power signals.

III. MEASUREMENT DATA

Figure 4 shows the small-signal performance of the LNA at 25°C. At 2.5GHz, the gain is 25.9dB, with greater than 45dB of reverse isolation. The input and output return losses are 16.0dB and 19.9dB respectively. The LNA is unconditionally stable as measured by the Rollett stability factor K and Δ [6] from 50kHz to 20GHz with input powers up to 0dBm.

Figure 5 demonstrates the improvement in IP3 as the input power increases. The third-order intermodulation products (IM3) are measured with two equally powered fundamental continuous-wave signals at 2499 and 2500 MHz. Under small-signal conditions, the single-tone input IP3 is measured to be –9dBm with 11mA of total current. At –13dBm total input power, the LNA reaches the maximum input IP3 of 6.8dBm with 23.9dB of gain and 22mA of total current.

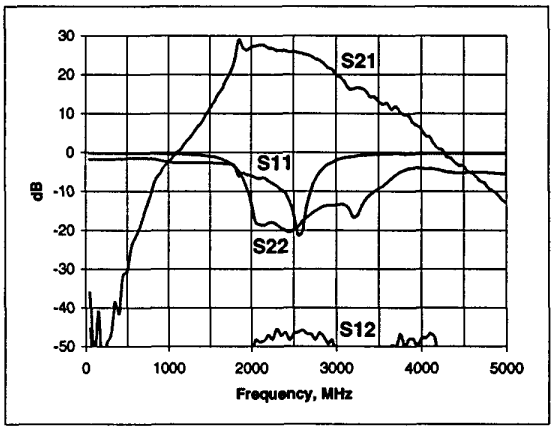

Figure 4. Measured small signal s-parameters

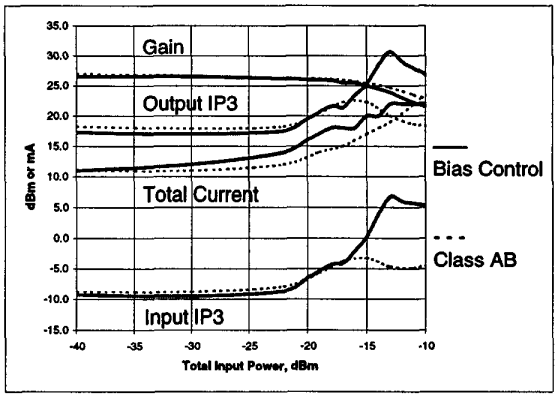

Figure 5. IP3 and total current consumption

The Class AB performance of the LNA without the power detector and the op-amp circuitry is included for comparison. The gate voltages are adjusted manually so that 5.5mA is supplied to each FET. The V_{DS} of each FET

is set to 3.0V. As the figure shows, the bias control significantly improves IP3 without requiring significantly more dc power than Class AB.

Figure 6 shows the NF of the LNA at 2.5GHz at input power levels from –50dBm to –10dBm. The nominal NF at 25°C is 0.87dB. A 2.4GHz jammer is input into the LNA along with the thermal noise from the diode head. The jammer forces the LNA into large-signal operation. The NF decreases to 0.68dB at –20dBm input power. As the input power continues to rise, however, the LNA enters compression. The NF increases dramatically as the inband diode noise is severely desensed by the jammer. The NF of the same LNA operating in Class AB, without the bias control, is included for comparison.

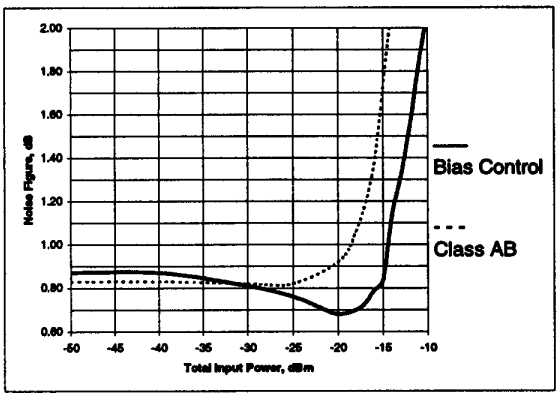

Figure 6. Noise Figure

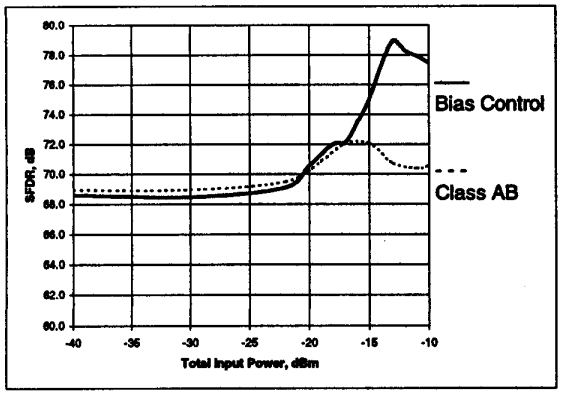

Figure 7. Spurious-free dynamic range

With higher IP3 and lower NF in large-signal operation, the LNA achieves a 10.5dB improvement in spurious-free dynamic range (SFDR) [7] compared to nominal conditions, as shown in Figure 7. The bandwidth used for calculating SDFR is 1.25MHz. The same LNA in Class AB could only obtain a 3.1dB improvement in SFDR. A typical LNA with fixed current consumption exhibits little, if any, increase in SFDR as the input power is increased.

IV. CONCLUSION

The low-noise amplifier with self-adjusting bias control demonstrated low power consumption in nominal small-signal conditions. The LNA showed significant improvement in dynamic range by automatically increasing the power consumption in the presence of a strong jammer to prevent receiver link degradation. The design concept can be readily adapted to suit a variety of applications of differing frequencies and requirements.

References

[1] S. Chen, "Linearity Requirements for Digital Wireless Communication," *IEEE GaAs IC Symp. Dig.*, Anaheim, CA, pp. 29-32, October 1997.

[2] K. L. Fong, C. D. Hull, and R. G. Meyers, "A Class AB Monolithic Mixer for 900-MHz Applications," *IEEE Journal of Solid State Circuits*, vol. 32, pp. 1166-1171, August 1997.

[3] T. Lee et al., "Temperature Dependence of the Ideality Factor of GaAs and Si Schottky Diodes," *Physica Status Solidi*, vol. 152, pp. 563-571, December 1995.

[4] P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*. New York: Wiley, 1993.

[5] R. G. Harrison and X. L. Le Polozec, "Nonsquarelaw Behavior of Diode Detectors Analyzed by the Ritz-Galerkin Method," *IEEE Trans. Microwave Theory Tech.*, vol. 42, pp. 840-845, May 1994.

[6] G. Gonzalez, *Microwave Transistor Amplifiers, Analysis and Design*. Eaglewood Cliffs, NJ: Prentice Hall, 1984.

[7] B. Razavi, *RF Microelectronics*. Upper Saddle River, NJ: Prentice Hall, 1998.