Applications of Si/SiGe Technology for High-Speed Communications Systems – Invited Paper

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Abstract This paper will summarize recent developments in the field of Si/SiGe HBT technology for high-speed communications applications. This technology promises to provide "III-V-like" performance in a silicon VLSI environment, and recent developments demonstrate that highly integrated mixed-signal devices can be implemented with outstanding performance and yield.

I. INTRODUCTION

The explosion of interest in integrated circuit technology for communications applications in the last decade has been driven by the expansion of the market for untethered communications in a variety of forms - from pagers and cordless telephones to analog and digital cellular telephones, DBS, and PCS. In addition, the widespread adoption of fiber-optic communications has created a need for high-frequency electronic repeater and switching circuits, whose bandwidth increases on an almost yearly basis. The high-frequency nature of these products typically requires that they contain a mixture of digital, rf and analog functions, operating at the highest possible performance levels.

CMOS, Si/SiGe, GaAs, InP, SiC and GaN are all vying for differing pieces of this evolving marketplace. Si/SiGe technology promises to satisfy the simultaneous requirements of outstanding high-frequency performance and low-cost silicon manufacturing for high-performance and high-levels of integration applications. These advantages can manifest themselves in several different ways.

II. HIGH-FREQUENCY PERFORMANCE OF Si/SiGe HBT TECHNOLOGY

The outstanding high-frequency performance of Si/SiGe HBT technology has been well established by a variety of groups [1, 2]. In many applications, this speed performance advantage can be "traded-off" in a very satisfactory way for dramatically reduced power dissipation. It is at low power levels where Si/SiGe HBT technology has a distinct advantage compared to most technologies. The germanium content within the base of the SiGe HBT leads to a device of superior performance compared with a similarly structured silicon-only epitaxial-base transistor.

A good example of this improvement can be seen from the transistor data presented in Fig.1 comparing transistor f_T and f_{max} as a function of collector current for 0.5μm X 2.5μm epi-base SiGe HBTs and Si BJTs of *comparable base resistance* (approximately 12KΩ/□) [3]. In this case, the peak f_T for the Si BJT and SiGe HBT are 38 and 50 GHz respectively, the peak f_{max} values of the Si BJT and SiGe HBT are 54 and 66 GHz respectively. The epi-base SiGe HBT achieves higher f_T and f_{max} values than the epi-base Si BJT over its entire range of operation. In addition, for a given required f_T or f_{max} , the SiGe HBT requires roughly one-third the collector current of an "equivalent" Si BJT for equivalently sized devices, dramatically lowering the power requirements in those circuits that are required to operate at very high frequencies.

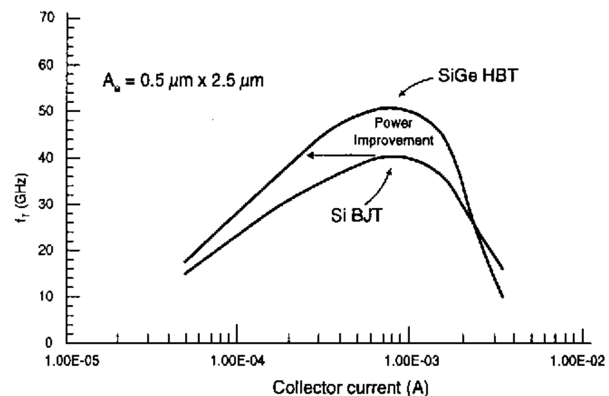

Fig.1. Comparison of epi-base Si/SiGe HBT and Si BJT f_T with comparable base resistivity [3].

The high-frequency systems applications of a technology capable of achieving f_T 's in excess of 100 GHz are numerous, and extend well into the millimeterwave frequency region. They include automobile collision warning radar, wireless distribution of cable television, and millimeterwave point-to-point radios. Recent research results have demonstrated outstanding performance for Si/SiGe HBT circuits operating at frequencies above 10 GHz. They include

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frequency dividers operating to 28 GHz [4], Gilbert mixers operating to 12 GHz [5], power amplifiers with over 25 dBM of output power at 1.9 GHz [6], VCOs with, -103 dBc/Hz of phase noise at 7.5 GHz. [7].

There is no question that III-V–based devices in GaAs or InP technology will exhibit superior f_T and f_{max} compared to a Si/SiGe device for a specified geometry. An excellent comparison of the technologies was presented in [8], and a plot from that paper of relative speed as a function of base width is shown in Fig. 2. Clearly, if maximum performance or speed is the *only* criteria, then III-V technology is the superior option.

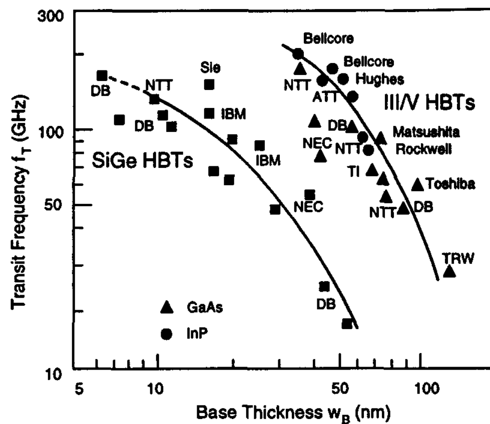

Figure 2. Comparison of HBT f_T as a function of base width for Si/SiGe and III-V technologies [8].

III-V-based devices will also exhibit superior *breakdown voltage* properties at a given speed due to the well-known higher bandgap energies and mobilities, The well-known Johnson limit [9] for speed vs. breakdown voltage in semiconductor devices results in higher gain for the GaAs power devices, even at the lower operating voltage, due to the higher electron mobility. The higher gain translates into improved power-added efficiency, and potentially improved linearity, at higher-frequencies of operation.

III. MICROWAVE PERFORMANCE of Si/SiGe HBTs.

Low-noise amplifiers are one of the key performance bottlenecks in an RF system. They are required to contend with a variety of signals coming from the antenna – often of larger amplitude than the desired signal – and so both low-noise and high linearity are simultaneously required. These requirements are often at odds with an additional requirement for low power dissipation.

Fig. 3 plots amplifier Gain/DC Power Dissipation (in dB/mW) as a function of Noise-Figure (in dB) for a variety of reported low-noise amplifiers in silicon and GaAs technology at 2 GHz. Most of the recently reported LNA results, fabricated in Si CMOS [10], or bipolar technologies [11, 12] fall along a Gain/(Pdc*NF) line of approximately 0.4 (1/mW). By comparison, a SiGe HBT result [13] demonstrated a fully integrated LNA with 0.95 dB Noise-Figure, 2 mW of power dissipation and 10.5 dB of gain at 2.4 GHz, for a figure of merit of approximately 5.5 (1/mW). The best reported GaAs LNA's have figures of merit of approximately 3.0 (1/mW) [14, 15, 16].

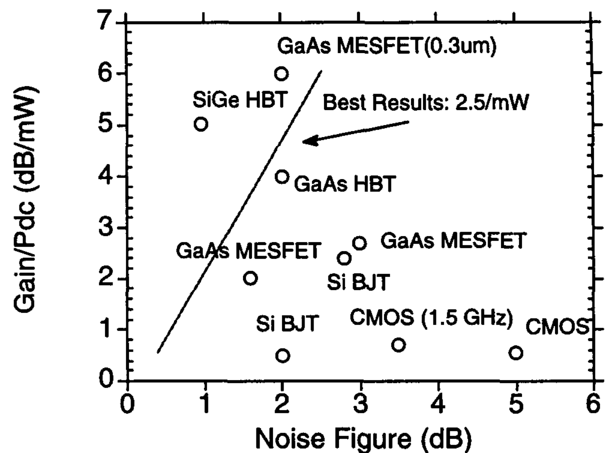

Figure 3. Gain to dc power ratio plotted versus Noise-Figure for state-of-the-art 2 GHz LNA's. The best results have a figure-of-merit of approximately 2.5/mW.

Linearity is an equally important figure of merit for front-end transistor amplifiers. In this case, an often-used linearity figure-of-merit is the ratio of the Input Third Order Intercept Point (IIP3) to the DC power dissipation, with values of 0.2 being typical. Field effect transistors (MOSFETs as well as GaAs MESFETs and PHEMTs) generally exhibit improved third order intermodulation distortion compared with bipolar devices, due to their near square-law current vs. voltage behavior.

On the other hand, GaAs HBT amplifiers have recently demonstrated outstanding linearity performance as well, apparently due to the cancellation of the resistive and capacitive non-linearities in the base-emitter junction at certain frequencies [17]. Si/SiGe HBTs appear to exhibit the same beneficial effects, as demonstrated by the recently announced IBM SGRF0100 high-dynamic range discrete HBT, which has a typical input intercept point of +13 dBm and a 1.2 dB NF at 1900 MHz, and a dc power dissipation of only 15 mW [18] with a 3V supply. This

leads to a linearity figure of merit of 1.3, and a NF figure of merit of approximately unity.

Si/SiGe device technology has also moved into the low-voltage power amplifier arena recently, with a number of promising results. Greater than 70% power-added efficiency was obtained at 1.8 GHz with a 33 mW output power, and greater than 60% PAE was observed with over 100 mW output power at 0.9 GHz using a modified "high-breakdown" profile [19]. Although not intrinsically well suited to power applications due to its low breakdown voltage, the high f_T and f_{MAX} of these devices will result in outstanding performance at low voltages and low output powers.

Advanced packaging techniques will also be required in order to fully utilize the technology in systems applications above 10 GHz. Typical bond-wire and lead-frame inductances limit the high-frequency performance of packaged devices to less than 5 GHz [20]. Flip-chip bonding of X-band and Ku-band Si/SiGe MMICs was recently demonstrated [21], with outstanding results, in a quasi-hybrid packaging environment.

One major potential limitation of silicon technology for very high-frequency applications is the availability of low-loss transmission line structures for impedance matching applications. Historically, transmission lines in silicon technology have suffered from extremely high losses resulting from the relatively high conductivity of typical silicon substrates. In addition, the ohmic losses of transmission lines implemented in silicon have tended to be high, because of the relatively thin Al-based metallization employed in most VLSI processes.

Despite these drawbacks, a number of approaches have been attempted to realize these structures in a monolithic silicon environment, including coplanar transmission lines on lightly-doped substrates [22,23], thick deposited SiO_2 for realization of microstrip structures [24], and thick polyimide layers to separate the transmission lines from the silicon substrate [25].

IV. Si/SiGe TECHNOLOGY FOR HIGHER LEVELS OF INTEGRATION

With the advent of 10 Gbps (OC-192) telecommunications systems and related high data rate signal processing, complex high speed digital circuits are required for a host of applications including optical transmitter and receiver modules, multiplexing and demultiplexing, and digital signal processing. The silicon pedigree of Si/SiGe technology will provide for a straightforward path for "up-integration" of standard radio-frequency functions along with analog-to-digital conversion and digital signal processing onto a single high-performance integrated circuit. This migration of multiple functions onto a single die will have some profound implications for wireless transceiver architectures and the telecommunications industry.

Hughes Space and Communications has explored the utility of SiGe technology for complex, high speed digital applications in ground and satellite communication systems. A total of forty-six 4 Gbps cells and sixty eight 16 Gbps cells have been developed. High-speed test circuits were characterized, including a 20 GHz regenerative divide-by-2, static divide-by-4, and 4 GHz XOR. The gate delay of a SiGe current mode logic (CML) circuit was found to be 19 ps (using a 15-stage ring oscillator. The gate delay chains through CML and emitter coupled logic (ECL) standard cell gates for SiGe HBTs were also measured, resulting in gate delays for all standard cells of 17 to 55 ps.

Hughes demonstrated the viability of SiGe for high speed, high yield, complex ASICs when it designed a timing circuit as part of a high speed digital signal processing (DSP) development program. The custom timing circuit was designed to operate with a 2.4 GHz input clock and provide system clock and synchronization signals to DSP ASICs. The circuit was slightly larger than 5000 transistors, dissipated 3.3 W, and was 124 mil x 151 mil. It was fabricated at IBM and 85% on-wafer chip yield was obtained using a 50 MHz input clock. The timing circuit, packaged in a kovar quad flatpack, demonstrated greater than 3.0 GHz operation.

To evaluate the limits of the complexity of the IBM SiGe BiCMOS process, as well as advanced ASIC packaging techniques, a complex Mux/Demux ASIC was designed. The design incorporated both Mux and Demux functions in a single chip with the functionality defined at "power on". The design utilized 39,000 transistors, which is believed to be the largest bipolar-only circuit yielded in the IBM SiGe technology. The circuit operated at the designed 3.5 Gbps clock speed when tested on-wafer with a membrane probe card. A unique feature of the design was the use of the IBM C4 solder bump technology designed for flip-chip packaging. In this demonstration the surface of the Demux/Mux chip was covered with an array of 480 (32 x 15) C4 solder bumps that provided high speed, low speed, bias, and ground connections. When flip-chip attached to a multilayer substrate the 3.5 Gbps performance was validated

As part of a continuing internal high-speed digital circuit development, a 14 Gbps multiplexer (Mux), demultiplexer (Demux) chip set was designed. The 1:4 Demux and 4:1 Mux chips utilized the 16 Gbps standard cell library described above and contained 958 and 1400

transistors, respectively. Both the Demux and Mux designs had greater than 85% on-wafer yield when tested at 50 MHz. When assembled on kovar carriers with alumina slave substrates, operation of 14 Gbps and 16 Gbps was obtained for the Demux and Mux, respectively. To test the high-speed performance of the ASICs, as well as the interconnects and packaging, a back-to-back test of the 1:4 Demux – 4:1 Mux was performed using an Anritsu test generator. A well defined eye pattern was observed using a 13.8 Gbps test pattern as seen in Fig. 5.

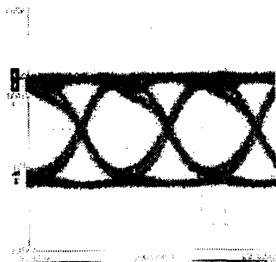

Fig. 5. Eye pattern measured in 13.8 Gbps back-to-back Demux/Mux test.

V. CONCLUSIONS.

The use of compound semiconductor technology promises dramatic improvements in existing applications in the coming years. Si/SiGe technology will allow high-performance *and* high levels of integration to be achieved, providing for the next performance "jump" in silicon technology.

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