A 16GHz Ultra High-Speed Si/SiGe HBT Comparator

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Abstract—**This paper presents an improved master-slave bipolar Si/SiGe HBT comparator design for ultra high-speed data converter applications. Implemented in a 0.5μm, 55GHz BiCMOS Si/SiGe process, this comparator consumes approximately 80mW with sampling speeds up to 16GHz.**

I. Introduction

Next-generation digital communications systems operating in the 10-60GHz range will rely on low-cost, high-bandwidth receivers operating in multi-gigahertz range. Analog-to-digital converters will be employed at higher and higher sampling rates in multi-gigahertz IF bandpass sampled and direct-to-digital systems. The comparator in these A/D converters plays a crucial role in the overall sample rate and resolution of the converter, and must be able to amplify and compare at rates greater than 10GHz. Increasing the sampling speed and bandwidth while minimizing offsets presents many challenges to the designer. This paper presents an improved design approach to the traditional bipolar master-slave comparator [1–6] to reduce the latch time and thus increase the overall clock speed of the comparator. The result is a design with a maximum clock rate that is much higher than traditional approaches.

II. Comparator Architecture

A. Review of Existing Comparator Approaches

A traditional latched comparator is shown in Fig. 1 [7]. When *clock* is high, (track phase), the input is amplified. When $\overline{clock}$ is high, (latch phase), the voltage difference at the output will cause the positive feedback pair to latch, resulting in a digital output signal. One well-known limitation in this design comes at high speeds where significant "kick-back" can be detected at the input due to Q3-Q4 being completely shut-off.

An improvement to this design can be seen in Fig. 2, [6]. Here a current-steering comparator is employed with the input devices (Q1-Q2) "always-on". The bias current, I_{bias}, is steered by the clock inputs either directly to the output in the track phase, or to a cross-coupled pair (Q7-Q8) in the latch phase. A key speed limitation of this improved design is that, when the latch phase is initiated, the base-emitter junctions of Q7-Q8 will need to "turn-on" and recharge, with the recharge current being provided by the bias current I_{bias}. At the absolute maximum clock rates, this junction charging time limits the maximum speed of the comparator, this problem is addressed later this paper.

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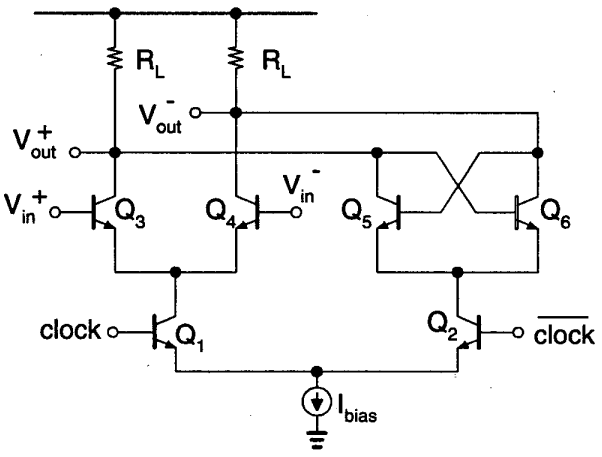

Fig. 1. Traditional track-latch comparator design.

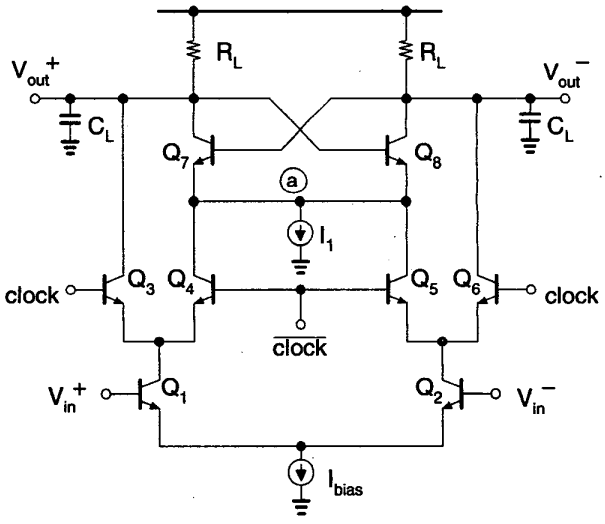

Fig. 2. Improved comparator design with additional current source.

During the track phase, with $I_1 = 0$, node @would rise to approximately $(V_{cc} - (I_{bias}/2 \cdot R_L))$. Once the latch activates, this node must drop by $V_{be}|_{on}$. This $V_{be}|_{on}$ is added across to the base-emitter capacitance at the start of the latch phase and extends the aperture of the comparator. The relative change in voltage at node @with respect to current is

$$\Delta V_{be} \approx V_T \cdot ln\left(\frac{I_{bias} + I_1}{I_1}\right) \quad (1)$$

where I_{bias} is the bias current for the entire comparator and I_1 is the keep-alive current in the latch. More time is required for the base-emitter junctions of the latch transistor to charge; and can be approximated by

$$t_{charge} \approx \frac{C_{be}(V_{be})\Delta V_{be}}{I_{bias}/2} \quad (2)$$

where $C_{be}(V_{be})$ is the base-emitter capacitance and ΔV_{be} is base-emitter voltage as described by (1). t_{charge} is approximately 43 picoseconds for our latch transistor with $I_{bias} = 1.0mA$ and $I_1 = 0$.

The total time required for a decision during the latch phase is equal to t_{charge}, plus the time required for the latch to achieve a full digital output signal, t_{latch} [5]. This latch-mode time constant can be written as

$$t_{latch} = \frac{\tau}{(A_{latch} - 1)} \cdot ln\left(\frac{\Delta V_{final}}{\Delta V_0}\right) \quad (3)$$

$$\approx \frac{C_L V_T}{I_{bias}/2} \cdot ln\left(\frac{2I_{bias}R_L}{\Delta V_0}\right) \quad (4)$$

$$(5)$$

and the minimum is achieved when

$$t_{latch}|_{min} = \frac{C_L V_T}{I_{bias}/2} \cdot ln\left(\frac{4V_T}{A_{pre}LSB}\right) \quad (6)$$

where ΔV_{final} is the desired final voltage difference of the latch, τ is $R_L C_L$, ΔV_0 is the voltage difference presented to the latch at time $t = 0$. The quantity $t_{latch}|_{min}$ is computed for ΔV_0 equal to $A_c A_{pre} \cdot LSB/2$, which is the worst case minimum input, where A_c is the gain of the comparator $(R_L g_m)$ and A_{pre} is the gain of any pre-amplification before the comparator. The result shows that gain before the comparator helps reduce the latch time by presenting a larger signal to the latch, at the expense of a reduction in bandwidth and increase in power consumption.

During the transition from the latch phase to the track phase, the time the differential output voltage takes to go from a full digital swing to zero when presented with an input voltage of $-LSB/2$, is the recovery time. Summing the currents at the output, the recovery time can be written as

$$t_{rec} = R_L C_L ln\left(1 + \frac{1}{tanh(q\Delta V0/2kT)}\right) \quad (7)$$

For our design t_{rec} is approximately 12 picoseconds for $I_{bias} = 1.0mA$. For low-power comparators this time can be much longer than the latch, or regeneration time, due to the larger output time constants [8]. Maintaining a large bandwidth is essential to reducing t_{rec}.

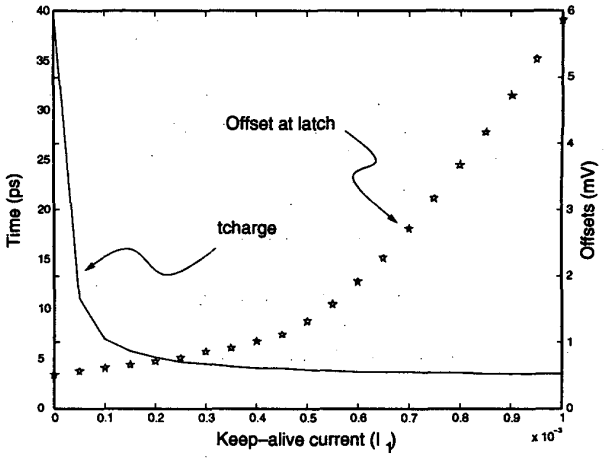

Fig. 3. a) Charge-time reduction with respect to keep-alive current. b) Offset at comparison point with respect to keep-alive current.

B. Improved Comparator Design

Current source, I_1 is added to keep the latch transistors from completely turning "off". If Q7-Q8 remains partially "on" during the "track" phase of operation, less time is required to fully charge the base-emitter junctions, and the overall speed is improved. This small change to the master-slave latch has a profound effect on the overall speed of the comparator.

The time to charge the base-emitter junction, from (2), now becomes

$$t_{charge} \approx \frac{C_{be}(V_{be})\,(V_{be,final} - V_{be,initial})}{I_{bias}/2} \quad (8)$$

With I_1 present, the base-emitter junction is pre-charged, significantly reducing t_{charge} to approximately 7 picoseconds.

Unfortunately, maintaining a small current through the latch devices during the track phase can add a small offset to the input *before* the decision is made. It is important to keep this offset small and provide adequate gain before the comparison occurs to limit its effects. So there is a fundamental tradeoff between hysteresis and switching speed with this approach that must be carefully assessed by the designer.

As long as I_1 is small during the track phase, the gain of the latch $(g_{m7} \cdot R_L)$ will be less than one and the latch will increase the overall small-signal gain of the comparator. The small-signal gain peaks when $g_{m7} = 1/R_L$. However, once I_1 exceeds $2V_T/R_L$ during the track phase, the negative conductance of the latch will be greater than $1/R_L$, and all of I_1 will switch to one side of the amplifier output.

This increases the hysteresis considerably. In this case $I_1 \cdot R_L$ will be added to, or subtracted from, the output during the track phase, depending on the previous decision of the latch. If it is desired to operate the comparator in this region, the values of

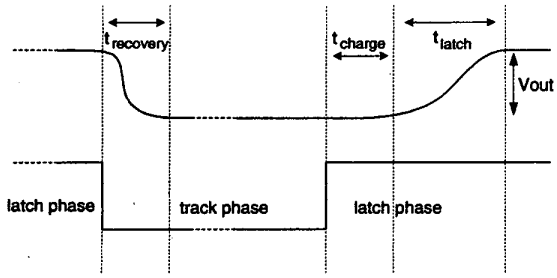

Fig. 4. Delay times during track and latch transitions

R_L and I_1 should be adjusted such that the hysteresis is kept below $A_{pre}A_0 \cdot LSB/2$. The improved sampling speed may prove to be more important than the hysteresis created by the latch. The offsets will increase with I_1 and eventually may grow larger than the input to the comparator. At this point the comparator will cease to function correctly and the output of the latch will remain in one logic state. Figure (3b) shows the simulated induced offset increases faster than I_1.

III. Analysis of Performance of the Improved Design

A. Comparator Meta-stability

Signals can exist that are so small that, when presented to the input, no decision is made over the clock period. These signals are called "meta-stable"; they are not truly stable, since provided enough time, the latch will eventually "trip". Previous work [6] has shown the probability of an occurrence of a meta-stable point after decision time t_d has elapsed, is

$$P(t > t_d) = exp\left(-\frac{A_{latch} - 1}{\tau} t_d\right) \quad (9)$$

where A_{latch} is the open-loop latch-gain. Normally for symmetric clocking t_d will equal $t_s/2$ where $t_s = 1/f_s$, where f_s is the sampling speed of the comparator. But as we can see in Figure 4, part of each clock period is occupied by the charging time. If we include the effects of t_{charge}, t_d is reduced to $t_s/2 - t_{charge}$. Now we have more time for the latch to reach the final differential voltage and a lower probability of a meta-stable point. For f_s samples, then the number of meta-stable states per second is

$$M_n = f_s exp\left(-\frac{A_{latch} - 1}{\tau} (t_s/2 - t_{charge})\right) \quad (10)$$

where τ is the RC constant of the latch. M_n is plotted against keep-alive current in Fig. 5. As I_1 increases, the charge time reduces quickly; and thus the number of meta-stable points per second dramatically reduces.

The technique that we have proposed here reduces the occurrence of meta-stable points, since the decision making time can be substantially decreased if the base-emitter junction of the latch is pre-charged. From the input buffer to the output of the master comparator there should be enough gain to minimize instability and overcome the hysteresis produced by the keep-alive

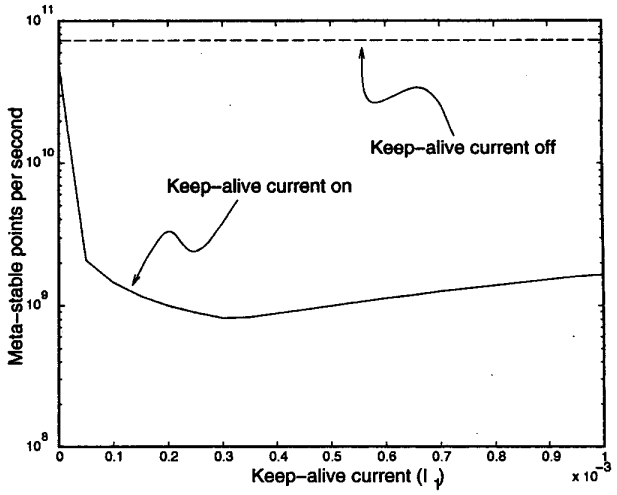

Fig. 5. Simulated number of meta-stable points per second with a sample rate of 16GHz.

current without drastic reduction in bandwidth. There is a gain of approximately 12dB in the input buffer (see Figure 6) and another 5dB in the comparator during the track phase. For I_1 equal to $100\mu Amps$, the input offset would be approximately 1mV, or about equal to that of the transistor mismatches of the comparator.

A wide signal bandwidth will help reduce the tendency for meta-stability by maintaining signal amplitude at high frequencies. Equation (10) shows that the number of meta-stable states is directly related to the unity-gain-bandwidth of the comparator [6]. To extend the unity-gain-bandwidth to its maximum, we used an extra pair of emitter-followers (Q5-Q6) within the loop (see Figure 6).

IV. Experimental Results

The design was fabricated in IBM's $0.5\mu m$ Si/SiGe BiCMOS process [9, 10]. The active area was $480\mu m$ x $200\mu m$ and the comparator consumes approximately 80mW with an additional 141mW consumed in the clock and output buffers used in the test chip. See Figure 8 for a die photo.

Input and clock signals were both differentially matched to 50ohms. Ultra-broadband off-chip baluns were used to bring the signals on and off chip. The input signal was sub-sampled with the clock frequency kept 40MHz lower than the input frequency. The digital output signal was processed with a logic analyzer state machine clocked at 80MHz. Without errors, the resultant output signal will be a stream of alternating ones and zeros.

At 16GHz with an input signal of 20mV and the I_1 turned off, the comparator is unable to function (see Figure 7b). By increasing the keep-alive current to about $100\mu Amps$, the emitter-base junction of the latch is pre-charged and the comparator functions properly (see Figure 7a).

V. Conclusions

A high speed comparator has been designed and fabricated with a clock speed in excess of 16GHz. A keep-alive device

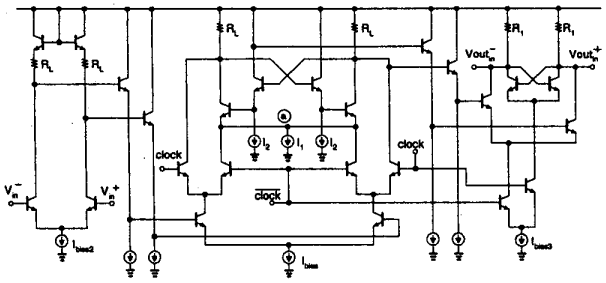

Fig. 6. Input buffer, master and slave comparators

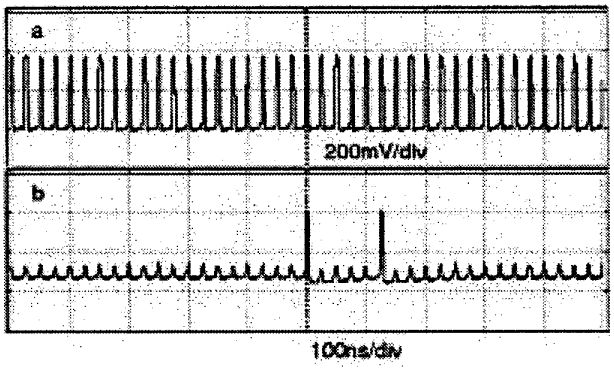

Fig. 7. 16.04GHz under-sampled digital signal. a)The keep-alive current is $100\mu A$, base-emitter diode pre-charged, and latch functions properly. b)The keep-alive current is turned off and the comparator is unable to operate.

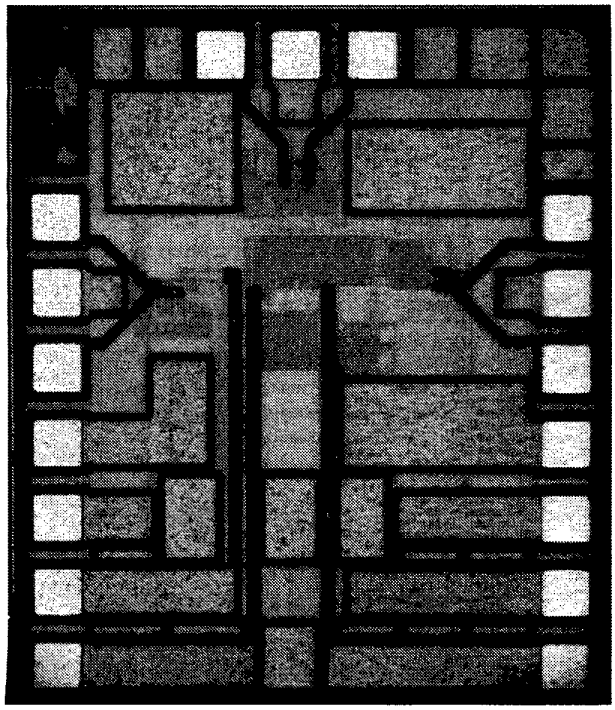

Fig. 8. Die Photo

is used to shorten the latch regeneration time and extend the frequency of operation.

VI. Acknowledgments

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