Bipolar Transistor Epilayer Design Using the MAIDS Mixed-Level Simulator

Leo C. N. de Vreede, Henk C. de Graaff, Joost A. Willemen, Wibo van Noort, Rik Jos, Lawrence E. Larson, Jan W. Slotboom, *Member, IEEE*, and Joseph L. Tauritz, *Senior Member, IEEE*

***Abstract*—In this paper, we address the epilayer design of the bipolar transistor using the one-dimensional (1-D) mixed-level simulator MAIDS (microwave active integral device simulator). MAIDS facilitates simulation of the electrical behavior of bipolar (hetero) junction transistors with various doping profiles and under different signal conditions in a realistic circuit environment. MAIDS as implemented within Hewlett Packard's microwave design system is a useful and promising tool in the development of bipolar transistors for large-signal conditions. Using MAIDS, we have identified the dominant bipolar transistor distortion sources with respect to the biasing conditions. Simulation results are compared with small- and large-signal measurements for the BFQ135 transistor, which has been developed for cable television (CATV) applications. By analyzing the measured and simulated data, we have developed an optimum epilayer design map for third-order intermodulation distortion that has proven to be particularly useful in the epilayer dimensioning of transistors for CATV applications.**

***Index Terms*—Bipolar transistor, cable television (CATV), epilayer, intermodulation, mixed-level simulator, nonlinear distortion.**

I. Introduction

RADIO-frequency (RF) amplifiers designed for multichannel communication systems are often hampered by nonlinear distortion. Recent improvements in compact modeling [1], [2] have led to more accurate design but are less fit in providing a direct link between process technology and circuit performance [3], [4]. A way to circumvent this limitation is to replace compact models by device simulator-based elements since they provide a direct and accurate link and are not limited by any assumption as to the shape of the doping profile. Device simulator-based elements are, therefore, most suitable for process technology optimization [5]–[7].

This paper describes the implementation and use of the mixed-level simulator MAIDS (microwave active integral device simulator) within Hewlett Packard's microwave design system (MDS). This combination facilitates accurate device simulation in an advanced circuit design environment. Following an introduction, MAIDS is used to identify three dominant sources of intermodulation distortion in bipolar transistors operated under class A bias conditions. Each of these distortion sources is shown to dominate in a specific region of the $I_c(V_{ce})$ characteristic. Based on this information, the optimum bias conditions for a given arbitrary epilayer structure can be identified. With this knowledge, an epilayer design chart yielding optimum epilayer dope and width for minimum third-order intermodulation distortion (maximum third-order interception point IP3) at a given collector-emitter voltage has been developed.

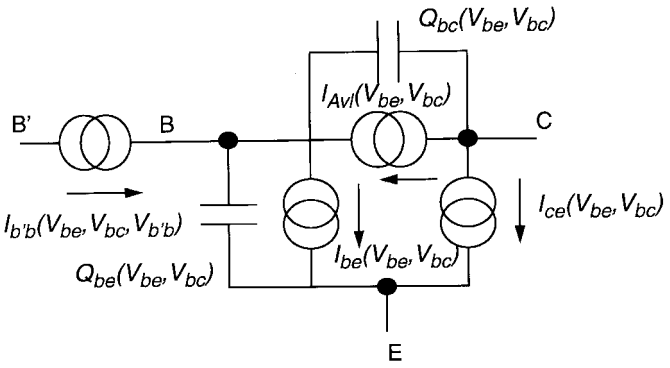


Fig. 1. Equivalent large-signal circuit for an intrinsic bipolar device within the MDS system. All functions are calculated based on the doping profile and applied voltages.

II. The MDS Implementation of MAIDS

We have chosen the one-dimensional (1-D) Si–SiGe bipolar device simulator HETRAP (developed at Philips Research) as a starting point for an implementation in MDS; at a later stage the core of the simulator was replaced by an extended version of the amorphous semiconductor analysis (ASA) program code [8], which has a more general structure and offers improved convergence at very high drive levels. The device simulator is used for calculating current and charge functions for the circuit elements of Fig. 1. All current and charge functions are calculated using the actual port voltages. The time dependence of the nonlinear devices is taken into account by the MDS simulator. The electrical implementation used for the intrinsic device is given in Fig. 1. External elements including series resistors, inductors, shunt capacitors, and other circuit elements can be easily added (Fig. 2). MAIDS has been successfully

Manuscript received January 7, 1999; revised April 2, 1999. This work was supported by Philips Semiconductors, Philips Research, and Hewlett Packard EEsof.

L. C. N. de Vreede, H. C. de Graaff, W. van Noort, J. W. Slotboom, and J. L. Tauritz are with the Department of Information Technology and Systems, Delft University of Technology, Delft 2600 GB The Netherlands (e-mail: l.c.n.devreede@its.tudelft.nl).

J. A. Willemen was with the Department of Information Technology and Systems, Delft University of Technology, Delft 2600 GB The Netherlands. He is now with Robert Bosch GmbH, Reutlingen, Germany.

R. Jos is with the Philips Semiconductors, Nijmegen 6534 AE The Netherlands.

L. E. Larson is with the Department of Electrical and Computer Engineering, University of California San Diego, La Jolla, CA 92093-0407 USA.

Publisher Item Identifier S 0018-9200(99)06495-1.

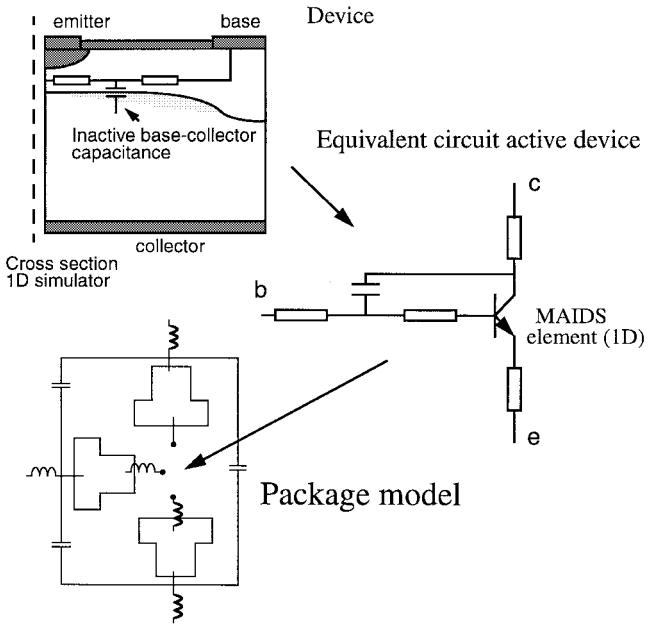


Fig. 2. Setup of the equivalent circuit for a packaged BFQ 135 transistor.

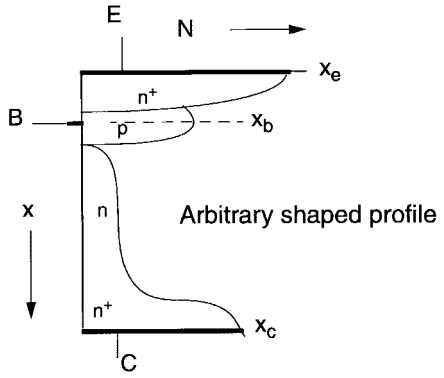


Fig. 3. Doping profile used for the computation of the current and charge functions of Fig. 1.

applied in the large-signal design of complete RF amplifier modules (with eight transistors).

III. Calculation of the Currents and Charges

The procedure employed to find the currents solves the Poisson and continuity equations using the user-specified doping profile (Fig. 3) and the applied voltages as input. Based on the specified doping profile, the variable stepsize generator automatically chooses a smoothly varying stepsize distribution. Various quantities like the electric field, mobility, current densities, recombination, and generation are calculated and can be accessed within the MDS program. The currents $I_{\rm be}$ and $I_{\rm ce}$ are found by multiplying the calculated current densities by the transistor area.

The charge functions $Q_{\rm be}$ and $Q_{\rm bc}$ are based on the electron distribution. Base charge partitioning is used to split the base emitter and base collector charges over the junctions at high frequencies in conformance with the base doping profile and the current drive level [9]. The method proposed in [9] introduces weighting functions (FE and FC). The charge functions are then given by

$$Q_{\rm be} = \int_E^C qnA \cdot FE(\eta)\, d\eta, \quad Q_{\rm bc} = \int_E^C qnA \cdot FC(\eta)\, d\eta \tag{1}$$

with

$$FE(x) = \frac{\displaystyle\int_x^C p(\eta)\, d\eta \Big/ \left(D_n n_{\rm ie}^2 \exp\left(\frac{\phi_p - V_{\rm be}}{v_T}\right)\right)}{\displaystyle\int_E^C p(\eta)\, d\eta \Big/ \left(D_n n_{\rm ie}^2 \exp\left(\frac{\phi_p - V_{\rm be}}{v_T}\right)\right)} \tag{2}$$

and

$$FC(x) = \frac{\displaystyle\int_E^x p(\eta)\, d\eta \Big/ \left(D_n n_{\rm ie}^2 \exp\left(\frac{\phi_p - V_{\rm be}}{v_T}\right)\right)}{\displaystyle\int_E^C p(\eta)\, d\eta \Big/ \left(D_n n_{\rm ie}^2 \exp\left(\frac{\phi_p - V_{\rm be}}{v_T}\right)\right)}. \tag{3}$$

Note that the sum of the weighting functions $FE(x) + FC(x) = 1$. The capacitance functions are calculated by taking the numeric derivative of the charges with respect to the nodal voltages.

IV. Implementation of the Avalanche Effect

The avalanche current is calculated as $I_{\rm avl} = I_c M_{\rm avl}$, in which $M_{\rm avl}$ is the avalanche multiplication factor, calculated including the effect of the electron energy relaxation length λ_e. This phenomenon is important for devices with a narrow peak in the electric field distribution. Reference [10] gives a suitable formulation of the effective electrical field with the energy relaxation length taken into account. This effective field can be calculated by performing postprocessing on the numerical solution found for the Poisson and continuity equations, Therefore, once the electric field $E(x)$ is known, we can calculate

$$E_{\rm eff} = \frac{1}{\lambda_e} \int_{x_b}^{x_c} E(u) e^{(u-x)/\lambda_e}\, du \tag{4}$$

$$M_{\rm avl} - 1 = \int_{x_b}^{x_c} a_n e^{-(b_n/E_{\rm ff}(u))}\, du. \tag{5}$$

In these

- λ_e energy relaxation length (0.065 μm is suggested in [10]);
- a_n constant (7.05×10^5 cm^{-1} for Si);
- b_n constant (1.23×10^6 V cm^{-1} for Si);
- x_b position of the base contact;
- x_c position of the collector contact.

V. Base Resistance

The nonlinear base resistance is modeled by a voltage-controlled nonlinear current source whose formulation is equivalent to that of the Mextram model [11], with the resistivity $\rho_{\rm base}(V_{\rm be}, V_{\rm bc})$ directly calculated from the internal device simulator data including conductivity modulation. The

formulation of $I_{b'b}$ also includes current crowding and is given by

$$I_{b'b} = \frac{2V_t(e^{V_{b'b}/V_t} - 1)}{r_b} + \frac{V_{b'b}}{r_b} \tag{6}$$

with

$$r_b = \rho_{\text{base}}(V_{\text{be}}, V_{\text{bc}}) \frac{H_e}{L_e} \tag{7}$$

and

$$\rho_{\text{base}}(V_{\text{be}}, V_{\text{bc}}) = \int_{x_e}^{x_c} q\mu_p p \, d\eta. \tag{8}$$

VI. Implementation Aspects

The program structure has been optimized for speed during transient and harmonic balance simulations by using the previous solution as a starting guess. This approach is very robust for small voltage steps; when the voltage steps become too large, intermediate voltage steps are used. The circuit simulator will on occasion supply the device simulator-based element excessive voltage values during the Kirchoff current law iteration. These voltages (e.g., $V_{\text{be}} > 5$ V) lead to numerical problems and consequently to floating-point errors. To overcome these difficulties, the current and charge functions are linearly continued beyond a user-specified junction voltage. The principle of this linear continuation is as follows. When one or both junction voltages exceed a given minimum or maximum, the voltages will be truncated to their maximum or minimum value before parsing them to the device simulator. Based on these voltages, the device simulator will calculate the main functions and their derivatives, which will be used for extrapolation of the main functions. The derivatives will be passed unchanged to the circuit simulator. As an example, the base current may be expressed as

$$I_{\text{be}} = I_{\text{be Max}} + \frac{\partial I_{\text{be}}}{\partial V_{\text{be}}}(V_{\text{be Overshoot}}) + \frac{\partial I_{\text{be}}}{\partial V_{\text{bc}}}(V_{\text{bc Overshoot}}). \tag{9}$$

This approach leads to a robust solution for dealing with high voltages during the iterations while avoiding convergence problems.

VII. The Electrical Representation

MAIDS is implemented in MDS in a manner analogous to the Gummel–Poon or Mextram model implementations. This implies the use of a model block to define the doping profile and all the material parameters for a given transistor type. Instances (symbols) are used to specify the location of the device in a circuit. Using this method, several MAIDS transistors can be combined in the same circuit.

To model lateral variation in current densities and potential over the transistor, quasi-two-dimensional (2-D) approximations have to be used to include these effects. By combining two 1-D elements with the appropriate area ratio, the influence of the extrinsic region (the nonlinear external base-collector capacitance) can be easily included. By coupling several 1-D device models via their internal base node, distributed 2-D and three-dimensional (3-D) effects like emitter current crowding can be approximated [12], [13]. This strategy yields robust convergence and results in an enormous saving in computational effort with respect to the time-consuming transient solution characteristics of full 2-D device simulators. Current spreading in the epilayer cannot, however, be modeled using this approach. The accuracy of simulation results is therefore limited for situations where current spreading in the epilayer is dominant. Nevertheless, MAIDS clearly identifies trends in transistor doping profile engineering for low distortion. For bipolar transistor amplifiers operating in class A, it turns out that the highest linearity is achieved for biasing where current spreading in the epilayer is basically absent. Optimum IP3 performance can then be accurately predicted.

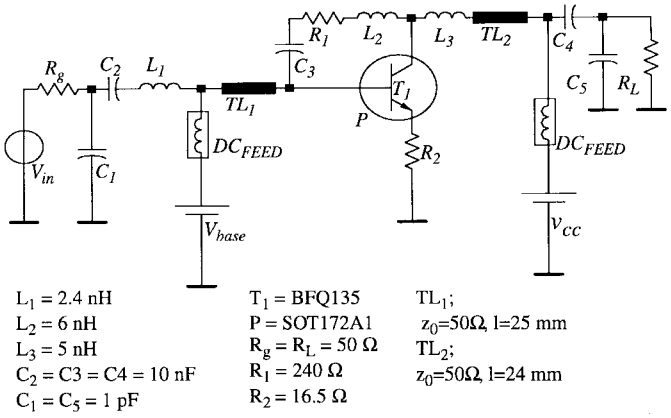


Fig. 4. Schematic of the modified 50-Ω BFQ135 intermodulation reference circuit.

In the rest of this paper, we will use, for reasons of simplicity, a single 1-D element with additional external circuit elements for the modeling of the parasitics (Fig. 2).

VIII. Using MAIDS for Large-Signal Transistor Design

The use of MAIDS to improve intermodulation distortion in bipolar transistors is now considered. We focus on Philips' BFQ135 transistor, which has been developed for cable television (CATV) applications. Realistic drive and circuit conditions are assured by using the datasheet intermodulation reference circuit given in Fig. 4. Initially, we carry out verification of our tool. We then identify the dominant bipolar transistor distortion sources with respect to the biasing conditions. By analyzing the measured and simulated data, we are able to reach some conclusions with respect to third-order intermodulation distortion in bipolar transistors under class-A bias conditions at high current levels.

IX. Verification of MAIDS using Small- and Large-Signal Measurements

For a 1-D intrinsic device, we have compared the computed MAIDS currents and capacitances with data using the 1-D option in the 2-D device simulator Medici [14] and found an agreement within a few percent. We have also measured and computed the small- and large-signal properties of the Philips BFQ135 intermodulation reference circuit (Fig. 4).

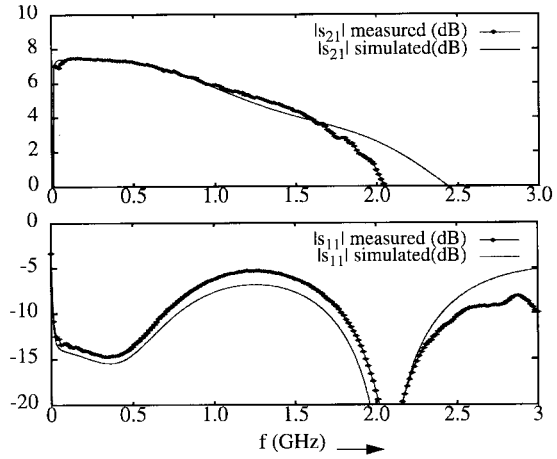


Fig. 5. Measured and simulated $|s_{21}|$ and $|s_{11}|$ between 300 kHz and 3 GHz.

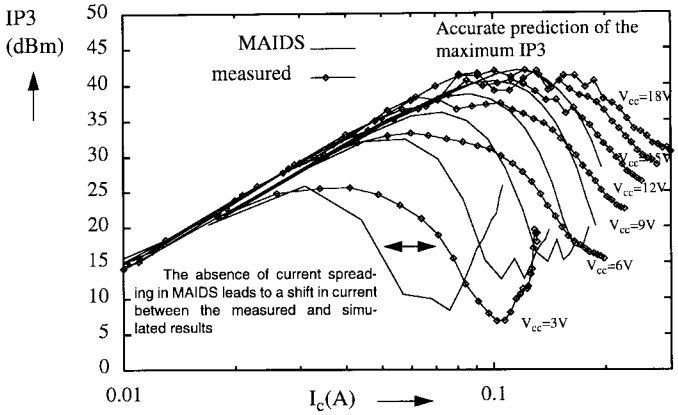


Fig. 6. Measured and simulated IP3 of the intermodulation BFQ135 reference circuit for a center frequency of 305 MHz as a function of I_c for the external voltage V_{cc} (3, 6, 9, 12, 15, and 18 V).

A. Small Signal

The measured and simulated S-parameters of the BFQ135 transistor are plotted in Fig. 5. The reference circuit is intended for use up to 500 MHz. However, measurements to 3 GHz have been taken in order to provide verification data required for the modeling of the distortion behavior, including the influence of higher harmonics. The measured and simulated S-parameters are in good agreement up to 1.8 GHz. Above 1.8 GHz, results begin to diverge.

B. Large Signal

Two-tone distortion measurements have been performed using a spectrum analyzer: by measuring the spectral components, the output third-order intercept point can be constructed. IP3 is also simulated as a function of the bias current for several external collector voltages (Fig. 6). MAIDS, although strictly 1-D in this case, proved able to predict accurately the level of distortion as a function of I_c and V_{cc} but failed (due to its 1-D nature) to predict the influence of current spreading in the epilayer, which results in a steeper decline of IP3 versus I_c (Fig. 6). This phenomenon can be explained by considering the current distribution in the epilayer for an increasing current level, using the 2-D device simulator Medici. A study of internal device conditions has shown that for a depleted epilayer, significant current spreading only starts when the base widens in quasi-saturation. Note, however, that from a design point of view, we are mostly interested in achieving the highest possible IP3, and this point is accurately predicted by the 1-D device simulator MAIDS.

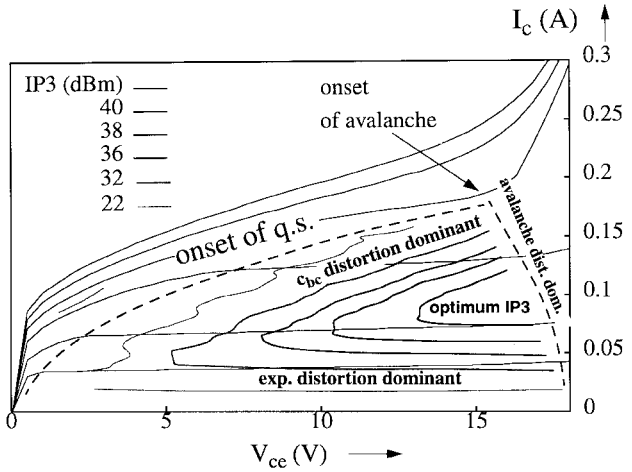


Fig. 7. Corresponding $I_c(V_{ce})$ characteristics of the intrinsic BFQ135 with lines of constant IP3.

X. Intermodulation Distortion and Optimum Bias Conditions

To gain more insight into the biasing conditions with respect to IP3 for class A, we have mapped the results of Fig. 6 on the $I_c(V_{ce})$ characteristics in Fig. 7 as lines of constant IP3. The onset of quasi-saturation (q.s.) and avalanche are indicated by dashed lines. Clearly, both the quasi-saturation region and the avalanche region are nonlinear regions, of little use for normal device operation. A study of the internal electric field has shown that optimum IP3 performance is found when the epilayer is fully depleted, the device is still far from the onset of q.s., and avalanche current generation is still very weak. These conclusions are in agreement with and extend the results found in [3], [4], and [15].

Mathematically, one can show that in a device, represented in MAIDS by the equivalent circuit of Fig. 1, nonlinear distortion is related to the variation of the partial derivatives of the current and charge functions along the load line. By concentrating on these partial derivatives, we have identified three major sources of distortion:

1) *exponential distortion* ($I_c \approx I_s e^{qV_{bc}/kT}$)*:* dominant at lower current levels (see Fig. 7) and the rising part of the curves in Fig. 6;
2) *nonlinear behavior of the base-collector capacitance* ($c_{bc} = \delta Q_{bc}/\delta V_{bc}$)*:* dominant at lower base-collector voltages and/or at higher current levels; its importance increases with frequency;
3) *nonlinear behavior of the avalanche effect, represented by the transconductance* ($g_{bc} = \delta I_{avl}/\delta V_{bc}$)*:* dominant at higher base-collector voltages.

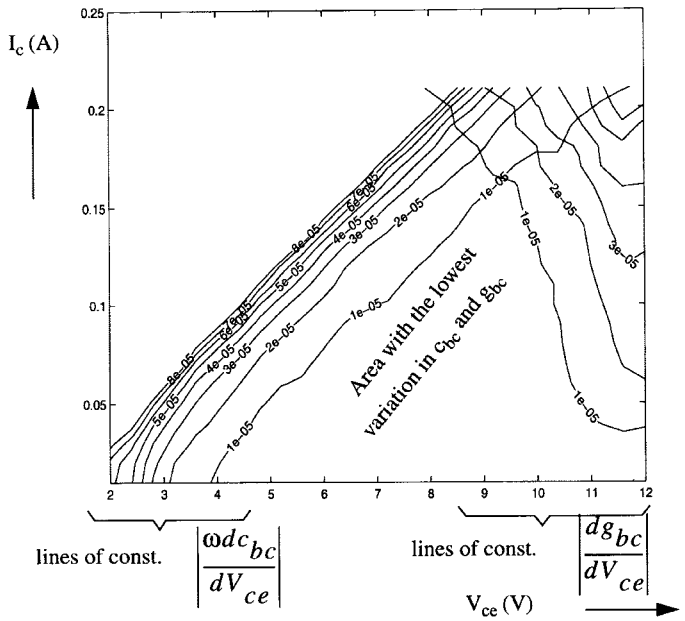


Fig. 8. Lines of constant $|\omega dc_{\rm bc}/dV_{\rm ce}|$ and $|dg_{\rm bc}/dV_{\rm ce}|$ for a device with $N_{\rm epi} = 3 \times 10^{15}$ cm^{-3} and $W_{\rm epi} = 1\,\mu$m ($f = 305$ MHz).

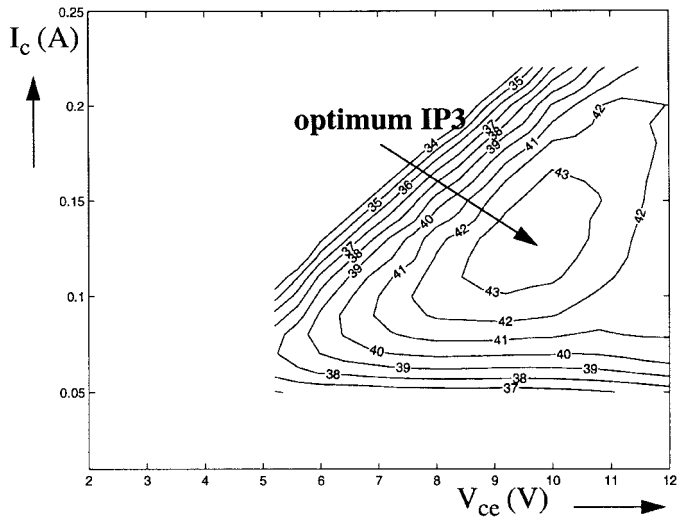


Fig. 9. Lines of constant IP3 for a device with $N_{\rm epi} = 3 \times 10^{15}$ cm^{-3} and $W_{\rm epi} = 1\,\mu$m, using MAIDS within the harmonic balance simulator MDS ($f_c = 305$ MHz and $\Delta f = 10$ MHz).

The influence of the nonlinear base resistance is of minor importance.

From the above, we conclude that $V_{\rm ce}$ should be as high as possible for a more constant behavior of $c_{\rm bc}$ (fully depleted epilayer). This is opposite to the avalanche effect, which requires a low $V_{\rm ce}$. Consequently, the optimum IP3 bias condition for $V_{\rm ce}$ requires a compromise between distortion sources (2) and (3). In practice, this is close to the point where the voltage and current swing along the load line yields a minimum variation in base-collector susceptance and conductance. Due to the opposite $V_{\rm ce}$ dependency and the compromise between these distortion sources, the optimum bias point for IP3 is found close to the point where ($\omega\Delta c_{\rm bc} \approx \Delta g_{\rm bc}$), provided that the collector current is sufficiently high that distortion source (1) no longer dominates (see Fig. 7).

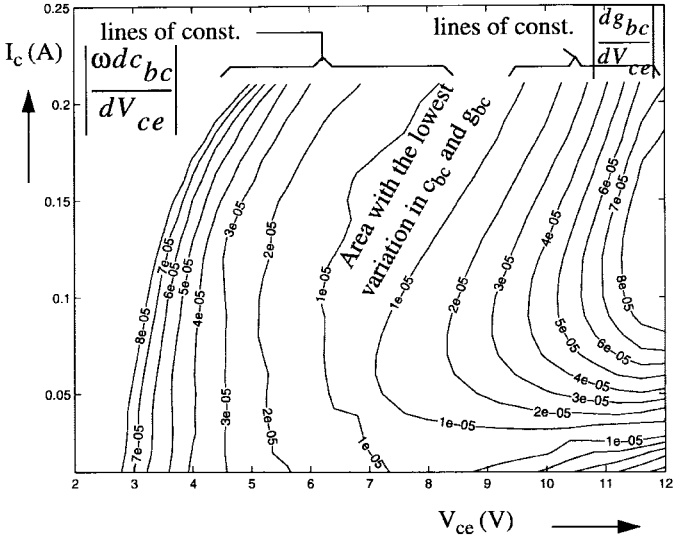


Fig. 10. Lines of constant $|\omega dc_{\rm bc}/dV_{\rm ce}|$ and $|dg_{\rm bc}/dV_{\rm ce}|$ for a device with $N_{\rm epi} = 9 \times 10^{15}$ cm^{-3} and $W_{\rm epi} = 1\,\mu$m ($f = 305$ MHz).

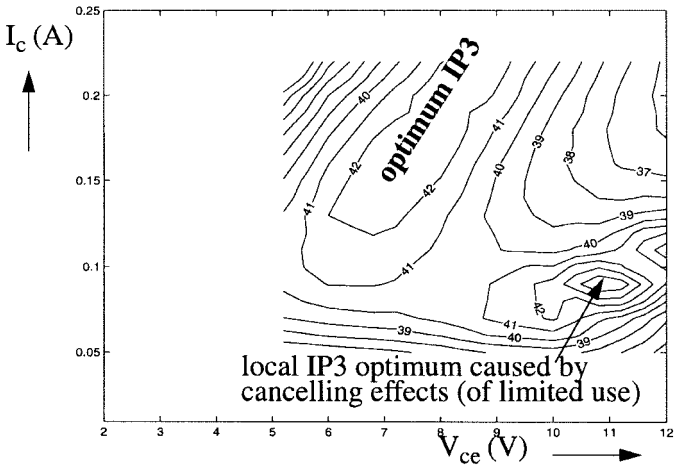


Fig. 11. Lines of constant IP3 for a device with $N_{\rm epi} = 9 \times 10^{15}$ cm^{-3} and $W_{\rm epi} = 1\,\mu$m, using MAIDS within the harmonic balance simulator MDS ($f_c = 305$ MHz and $\Delta f = 10$ MHz).

To verify the above, we have chosen a fictitious device structure with the epilayer parameters $N_{\rm epi} = 3 \times 10^{15}$ cm^{-3} and $W_{\rm epi} = 1\,\mu$m. For this device, we have calculated $c_{\rm bc}(V_{\rm ce}, I_c)$ and $g_{\rm bc}(V_{\rm ce}, I_c)$ over the entire $I_c(V_{\rm ce})$ plane, using MAIDS. Since we are only interested in the variation of $c_{\rm bc}(V_{\rm ce}, I_c)$ and $g_{\rm bc}(V_{\rm ce}, I_c)$, we calculate the total differential and eliminate $dI_c \approx -dV_{\rm ce}/R_{LT}$). Doing so, we obtain

$$dc_{\rm bc} = dV_{\rm ce}\left(\frac{\partial}{\partial V_{\rm ce}}\,c_{\rm bc}(V_{\rm ce}, I_c) - \left(\frac{1}{R_{LT}}\right)\frac{\partial}{\partial I_c}\,c_{\rm bc}(V_{\rm ce}, I_c)\right)$$

$$dg_{\rm bc} = dV_{\rm ce}\left(\frac{\partial}{\partial V_{\rm ce}}\,g_{\rm bc}(V_{\rm ce}, I_c) - \left(\frac{1}{R_{LT}}\right)\frac{\partial}{\partial I_c}\,g_{\rm bc}(V_{\rm ce}, I_c)\right). \tag{10}$$

Plotting lines of constant $|\omega dc_{\rm bc}/dV_{\rm ce}|$ and $|dg_{\rm bc}/dV_{\rm ce}|$ using (10) (Fig. 8) and comparing results with lines of constant

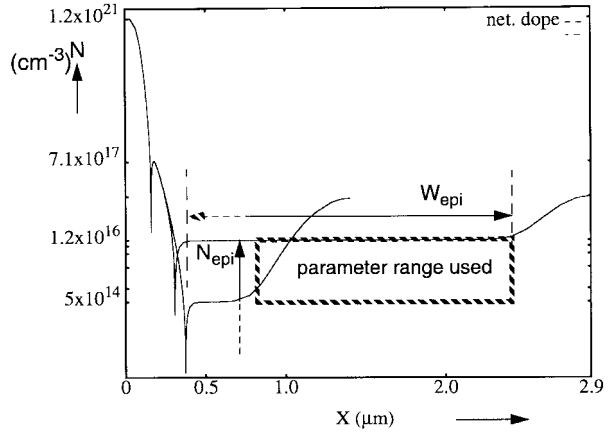


Fig. 12. Parameterized doping profile of the BFQ135 transistor.

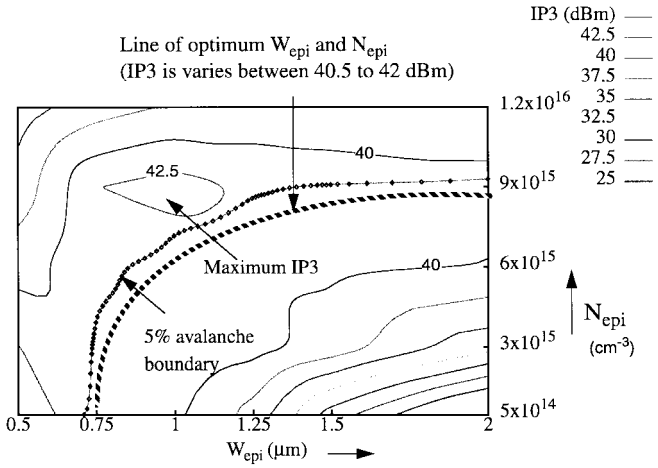


Fig. 13. The resulting lines of constant IP3 for the intermodulation reference circuit as a function of $W_{\rm epi}$ and $N_{\rm epi}$. $V_{\rm ce} = 12$ V, $V_{\rm be} = 0.950$ V, and I_c is 87 mA.

IP3 calculated using MAIDS with harmonic balance (Fig. 9), the highest IP3 is found for the bias region yielding the lowest variation in $c_{\rm bc}$ and $g_{\rm bc}$. To support this result even further, we have repeated the experiment for the same structure but now with the epilayer dope set to $N_{\rm epi} = 9 \times 10^{15}$. Comparing Figs. 10 and 11, the correlation becomes even more evident. Note that the effect of the exponential behavior is not taken into account in Figs. 8 and 10.

It is clear that the exponential distortion (1) is almost completely determined by the level of the collector bias current, while the distortion sources (2) and (3) are strongly influenced by the epilayer design. Furthermore, the nonlinear behavior of the base-collector capacitance can be reduced by highly doping the base and buried layer using steep edges.

With increasing frequency, the limitation on maximum IP3 is determined by the variation in the base-collector capacitance $\omega\Delta c_{\rm bc}$. Assuming a constant doping profile, the optimum bias condition will shift to higher base-collector voltages, up to the point where a new balance is found for the distortion caused by avalanche and the distortion caused by the nonlinear behavior of $c_{\rm bc}$. At lower frequencies $\omega\Delta c_{\rm bc}$ is less constrained, so that a higher IP3 can be achieved.

XI. Optimization of the BFQ135 Profile

Based on the above, we conclude that, in general, optimum bias conditions are found at higher current levels in combination with a fully depleted epilayer. Consequently, each specific collector-emitter voltage bias is associated with a unique optimum dimension of the epilayer. To investigate this, we have parameterized the collector doping profile of the Philips-developed BFQ135 transistor. The BFP135 has been experimentally optimized over a period of years for use in CATV applications. In our parameter sweep, we will change the effective epilayer width ($W_{\rm epi}$) and doping ($N_{\rm epi}$) as indicated in Fig. 12.

Using MAIDS, we have swept the epilayer width ($W_{\rm epi} = 0.5, 0.75, 1.0, 1.25, 1.5, 2.0$, and $2.5\ \mu$m) and the epilayer dope ($N_{\rm epi} = 0.5 \times 10^{15}$, 1×10^{15}, 3×10^{15}, 6×10^{15}, 9×10^{15}, and 12×10^{15} cm^{-3}) for each bias condition. By plotting lines of constant IP3, the optimal epilayer dimensions can be found for a given bias condition. In Fig. 13, lines of constant IP3 are plotted as a function of $W_{\rm epi}$ and $N_{\rm epi}$ for the optimum bias conditions $V_{\rm ce} = 12$ V and $I_c \approx 87$ mA. In this particular example, the maximum IP3 is found for $W_{\rm epi} = 1\,\mu$m and $N_{\rm epi} = 9 \times 10^{15}$ cm^{-3}; however, this maximum for IP3 lies beyond the $I_{\rm av1}/I_b = 5\%$ avalanche current generation limit and is therefore (due to significant cancellation effects) of limited use. The optimum dimensioning of the epilayer in this case is in fact close to the avalanche boundary. Since the IP3 does not vary significantly along the avalanche boundary (less than 2 dBm), the optimum epilayer design is given by a line rather than by a point (Fig. 13). We can repeat this procedure for different bias conditions and find a global epilayer design optimum for each collector-emitter voltage. The corresponding simulation results are combined into a single epilayer design graph (Fig. 14). The highest IP3 values tend to be found in the central region. The optimum IP3 for the intermodulation reference circuit is in the range of 40–42 dBm for different collector voltage conditions and appears to be relatively independent of the collector voltage.

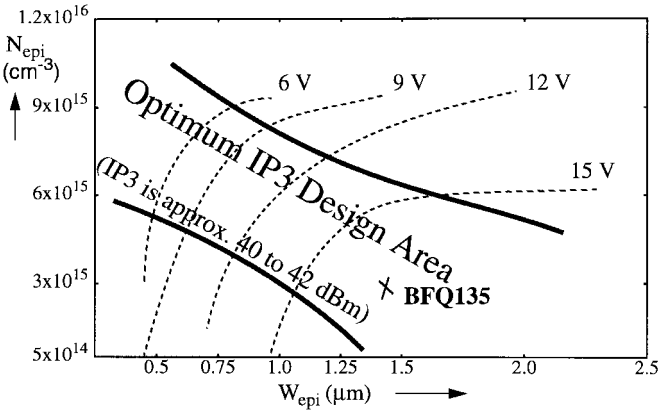


Fig. 14. IP3 transistor epilayer design map. The lines indicate the optimum dimensions of the epilayer quantities $W_{\rm epi}$ and $N_{\rm epi}$ for an optimal biased transistor placed in the intermodulation reference circuit for $V_c = 6$, 9, 12, and 15 V. The highest values for IP3 can be found between the solid lines. The center frequency is 305 MHz and Δf is 10 MHz.

As can be seen in Fig. 7, the optimum IP3 biasing for the BFQ135 is $V_{ce} \approx 17$ V and $I_c \approx 100$ mA, resulting in an IP3 of 42 dBm (Fig. 6). The epilayer parameters of the BFQ135, $W_{epi} = 1.5\,\mu$m and $N_{epi} = 3 \times 10^{15}$ cm^{-3}, are located in the optimum IP3 design area as indicated in Fig. 14, verifying that our numerical optimization matches with the experimental optimization of the BFQ135 doping profile. Additional transistor data can be found in [3] and [4].

XII. Discussion and Conclusions

With the implementation of MAIDS in MDS, the nonlinear circuit behavior of transistors, defined in terms of their doping profile, can be computed. By minimizing the calculation time, implementing automatic mesh generation and taking additional measures to ensure robust convergence, an easy to use, flexible modeling element has been created. This element not only facilitates increasing insight into the nonlinear behavior of a transistor but also opens a route to the automatic optimization of the doping profile with respect to various circuit specifications. Mixed-level simulator results have been compared with small- and large-signal measurements for the Philips BFQ135 intermodulation reference circuit and found to be in good agreement. The average calculation time for the third-order intercept point at each bias condition was five minutes on a HP9000/735/99 workstation. Optimum IP3 performance requires full depletion of the epilayer and device operation far from the onset of q.s., with very weak avalanche current generation and under relatively high collector current conditions. Complete depletion of the epilayer has as a consequence that each specific collector-emitter voltage requires a unique set of epilayer dimensions for optimum IP3. With the mixed-level simulator MAIDS, an epilayer design map has been developed that works out to be particularly useful in the epilayer dimensioning of transistors in ultra-high-frequency CATV applications.

References

[1] L. C. N. de Vreede, H. C. de Graaff, J. L. Tauritz, and R. G. F. Baets, "Advanced modeling of distortion effects in bipolar transistors using the Mextram model," *IEEE J. Solid-State Circuits*, vol. 31, pp. 114–121, Jan. 1996.

[2] L. C. N. de Vreede, H. C. de Graaff, J. L. Tauritz, and R. G. F. Baets, "Extension of the collector charge description for compact bipolar epilayer models," *IEEE Trans. Electron Devices*, vol. 45, pp. 277–285, Jan. 1998.

[3] H. F. F. Jos, "A model for the nonlinear base-collector depletion layer charge and its influence on intermodulation distortion in bipolar transistors," *Solid-State Electron.*, vol. 33, no. 7, pp. 907–915, 1990.

[4] ——, "Collector model describing bipolar transistor distortion at low voltages and high currents," *Solid-State Electron.*, vol. 37, no. 2, pp. 341–352, 1994.

[5] CIDER SPICE-based mixed level simulation program. [Online]. Available WWW: http://www-cad.eecs.berkeley.edu/Software/cider.html.

[6] J. Sato-Iwanaga *et al.*, "Distortion analysis of GaAs MESFET's based on physical model using PISCES-HB," in *Proc. IEDM'96*, Dec. 1996, pp. 6.7.1.–6.7.4.

[7] L. C. N. de Vreede, W. v. Noort, H. C. de Graaff, J. L. Tauritz, and J. W. Slotboom, "MAIDS; A microwave active integral device simulator," in *Proc. ESSDERC'97*, Stuttgart, Sept. 1997.

[8] J. A. Willemen, "Modeling of amorphous silicon single and multijunction solar cells," Ph.D. dissertation, Delft University of Technology, the Netherlands, Oct. 1998.

[9] H. Klose and A. W. Wieder, "The transient integral charge control relation—A novel formulation of the currents in a bipolar transistor," *IEEE Trans. Electron Devices*, vol. ED-32, pp. 1090–1099, May 1987.

[10] J. W. Slotboom, G. Streutker, M. J. v. Dort, P. H. Woerlee, A. Pruijmboom, and D. J. Gravestein, "Nonlocal impact ionization in silicon devices," in *Proc. IDEM'91* pp. 127–130.

[11] H. C. de Graaff and F. M. Klaasen, *Compact Transistor Modeling for Circuit Design.* New York: Springer-Verlag, 1990.

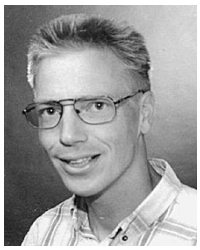
[12] H. N. Gosh, P. H. de la Moneda, and N. R. Dono, "Computer aided transistor design characterization and optimization," *Solid-State Electron.*, vol. 10, pp. 705– 726, 1967.

[13] D. J. Roulston, S. G. Chamberlain, and J. Seghal, "High level asymptotic variation of transistor base resistance and current gain," *Electronic Lett.*, vol. 7, pp. 438–440, July 1971.

[14] MEDICI two-dimensional device simulation program, ver. 2.1, Technology Modeling Associates Inc., Aug. 1995.

[15] K. W. Kobayashi, A. K. Oki, J. Cowles, L. T. Tran, P. C. Grossman, T. R. Block, and D. C. Streit, "The voltage-dependent IP3 Performance of a 35-GHz InAlAs/InGaAs-InP HBT amplifier," *IEEE Microwave Guided Wave Lett.*, vol. 7, pp. 66–68, Mar. 1997.

[16] H. C. de Graaff and W. J. Kloosterman. .Mextram documentation. [Online]. Available WWW: http://www-us.semiconductors.com/Philips_Models.



Leo C. N. de Vreede was born in Delft, the Netherlands, in 1965. He received the B.S. degree in electrical engineering from The Hague Polytechnic, the Netherlands, in 1988 and the Ph.D. degree from Delft University of Technology in 1996.

In 1988, he joined the Microwave Component Group of the Laboratory of Telecommunication and Remote Sensing Technology, Department of Electrical Engineering, Delft University of Technology. From 1988 to 1990, he worked on the characterization and modeling of CMC capacitors. From 1990 to 1996, he worked on modeling and design aspects of HF silicon IC's for wide-band communication systems. Since 1996, he has been an Assistant Professor at the Delft University of Technology working on the nonlinear distortion behavior of bipolar transistors at Delft Institute of Microelectronics and Submicron Technology (DIMES).

Henk C. de Graaff was born in Rotterdam, the Netherlands, in 1933. He received the M.Sc. degree in electrical engineering from Delft University of Technology, the Netherlands, in 1956 and the Ph.D. degree from the Eindhoven University of Technology, the Netherlands, in 1975.

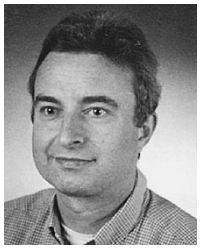
He joined Philips Research Laboratories, Eindhoven, in 1964 and worked on thin-film transistors, MOST, bipolar devices, and materials research on polycrystalline silicon. His present field of interest is device modeling for circuit simulation. Since his retirement from Philips Research (November 1991), he has been a Consultant to the University of Twente and the Delft University of Technology, both in the Netherlands.

Joost A. Willemen was born in Schijndel, the Netherlands, in 1967. He received the M.S. and Ph.D. degrees in electrical engineering from Delft University of Technology, Delft, the Netherlands, in 1993 and 1998, respectively.

From 1993 to 1998, he was with the thin-film solar-cell group at DIMES, Delft University of Technology. In this period, he worked on the device modeling of amorphous silicon single- and multijunction solar cells. In 1998, he joined the Semiconductors and Electronic Control Unit division of Robert Bosch GmbH, Reutlingen, Germany, where he is involved in the development of ASIC's and MEMS for automotive applications. His current research interests are modeling and characterization of electronic devices and MEMS, and coupled electrothermal circuit simulation.

Wibo van Noort was born in Amsterdam, the Netherlands, on September 20, 1972. He received the M.Sc. degree in electrical engineering from Delft University of Technology, Delft, the Netherlands, in 1996, where he currently is pursuing the Ph.D. degree.

The same year he joined the Laboratory of Electronic Components, Technology and Materials at Delft University of Technology. He is working on new technology for high-frequency bipolar transistors.



Rik Jos was born in Laren, the Netherlands, in 1954. He received the M.S. and Ph.D. degrees in physics from the University of Utrecht, the Netherlands, in 1982 and 1986, respectively.

In 1986, he joined Philips Discrete Semiconductors, Nijmegen, the Netherlands, where he developed silicon processes and devices for RF applications. He is particularly interested in semiconductor device physics and modeling with emphasis on nonlinear distortion. Since 1995, he has headed the process and device development group of Philips Discrete Semiconductors at Nijmegen.

Lawrence E. Larson received the B.S. degree in electrical engineering and the M.Eng. degree from Cornell University, Ithaca, NY, in 1979 and 1980, respectively. He received the Ph.D. degree in electrical engineering from the University of California, Los Angeles, in 1986.

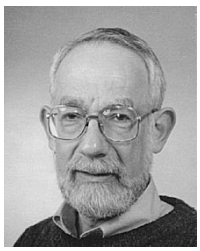
He joined Hughes Research Laboratories in Malibu, CA, in 1980, where he directed work on high-frequency InP, GaAs, and silicon integrated circuit development for a variety of radar and communications applications. While at Hughes, he led the team that developed the first MEMS-based circuits for RF and microwave applications. He was also Assistant Program Manager of the Hughes/DARPA MIMIC Program from 1992 to 1994. From 1994 to 1996, he was with Hughes Network Systems in Germantown, MD, where he directed the development of radio-frequency integrated circuits for wireless communications applications. He joined the Faculty at the University of California, San Diego, in 1996, where he is the inaugural holder of the Communications Industry Chair. He has published more than 100 papers and has received 21 U.S. patents.

Dr. Larson was a corecipient of the 1996 Lawrence A. Hyland Patent Award of Hughes Electronics for his work on low-noise millimeter-wave HEMT's.

Jan W. Slotboom (M'82) was born in Utrecht, the Netherlands, on December 26, 1942. He received the degree of electrical engineering from the Technical University of Delft, the Netherlands, in 1966 and the Ph.D. degree from the Technical University of Eindhoven, Eindhoven, the Netherlands, in 1977.

In 1967, he joined the Philips Research Laboratories, Eindhoven, the Netherlands, where he worked on bipolar device modeling, numerical simulation and experimental silicon device physics. His Ph.D. dissertation was about 2-D-numerical device simulation of bipolar transistors and pioneering experiments on bandgap narrowing in heavily doped silicon. He was involved in the development of CCD memories for video applications and exploratory research of high-density memories. He is currently studying novel silicon device technologies. He has authored or coauthored more than 70 papers and 17 U.S. patents. In 1994, he became a part-time Professor at the Delft Institute of Microelectronics and Submicron Technology (DIMES) of the Technical University of Delft. He was a member of the IEDM Solid-State Device Subcommittee in 1980, 1983, and 1984. He has been Vice Chairman and Chairman of International Arrangements of the IEDM. He was a Program Subcommittee member of the IEDM in 1991 and 1992 and has been a member of the Technical Program Committee of the ESSDERC since 1991. In 1995, he was a member of the Technical Program Committee of the BCTM Conference.

Dr. Slotboom has been a co-editor of ESSDERC issues of the IEEE TRANSACTIONS ON ELECTRON DEVICES (1997–1999).



Joseph L. Tauritz (S'60–M'63–SM'99) was born in Brooklyn, NY, in 1942. He received the B.E.E. degree from New York University, New York, in 1963 and the M.S.E. degree in electrical engineering from the University of Michigan, Ann Arbor, in 1968.

He was a Research Fellow at the Delft University of Technology, Delft, the Netherlands, from 1970 to 1971. He first became acquainted with microwaves while working as a Junior Engineer on circularly polarized antennas at Wheeler Labs in the summer of 1962. From 1963 to 1970, he was a Technical Specialist attached to the RF Department of Conductron Corp., where he designed innovative microwave, VHF, and video circuitry for use in high- resolution radar systems. In 1970, he joined the Scientific Staff of the Department of Electrical Engineering, Delft University of Technology, where he is presently an Associate Professor. Since 1976, he has headed the Microwave Component Group, where he is principally concerned with the systematic application of computer-aided design techniques in research and education. His interests include the modeling of high-frequency components for use in the design of MIC's and MMIC's, filter synthesis, and planar superconducting microwave components, as reflected in more than 70 publications and conference papers. He has served as a member of the Program Committee of the ESSDERC and of GAAS.

Mr. Tauritz is a member of Eta Kappa Nu. He was a cowinner of the 1997 European Microwave Prize.