A Wide-Bandwidth Si/SiGe HBT Direct Conversion Sub-Harmonic Mixer/Downconverter

Liwei Sheng, Jonathan C. Jensen, *Student Member, IEEE*, and Lawrence E. Larson, *Fellow, IEEE*

***Abstract*—A wideband sub-harmonic mixer/direct-conversion downconverter is implemented in a Si/SiGe HBT technology, with improved rejection of the local oscillator (LO), high input intercept point, and low current requirements. The circuit utilizes a combination of phase shifters operating at 45° and 90° to achieve better than 33-dB input-referred rejection of the LO. The measured third-order input intercept point (IIP3) was approximately −3 dBm and the second-order input intercept point (IIP2) was roughly 35 dBm, with a measured double sideband (DSB) noise figure of 7.8 dB. A comparison was made between devices of differing germanium concentration in the base, and the devices with higher Ge content exhibited improved noise figure and gain. Each mixer required approximately 2.8 mA from a 3.3-V supply.**

***Index Terms*—Direct conversion mixer, HBT, IIP2, IIP3, LO rejection, phase shifter, self-mixing, sub-harmonic mixer.**

I. Introduction

THE USE of direct-downconversion techniques is a promising approach for highly integrated wireless receivers due to their potential for low-power fully monolithic operation and extremely broad bandwidth [1]. Their potential for broadband operation is especially important for future wireless communication applications, where a combination of digital cellular, GPS, and WLAN applications are required in a single portable device. However, their application has been limited by the menagerie of dynamic range limitations associated with the conversion of an RF signal directly to baseband. In particular, *second-order distortion*, $1/f$ *noise*, and *local oscillator (LO) self-mixing* are some of the most important drawbacks [2]. LO self-mixing is a vexing problem with traditional homodyne approaches, because *any* signal at the LO frequency—including the LO!—appearing at the input terminals downconverts to dc. The magnitude of this signal can be measured and periodically subtracted from the mixer output [3], but its value varies with time in an unpredictable manner—limiting the effectiveness of the compensation—and it necessarily subtracts from the available dynamic range of the circuit.

Sub-harmonic mixers have historically been implemented in millimeter-wave technology as a means of performing downconversion of the received signal with an LO operating at a fraction of the frequency of the input signal [4]. Several early direct conversion receivers implemented diode-based sub-harmonic mixers as a means to minimize the conversion of the LO signal to dc [5]. Recently, they have been implemented in silicon bipolar technology for lower frequency applications using a "pulse-width modulation" technique [6].

In this paper, we present a Si/SiGe HBT direct-downconversion receiver using a "three-level multiplier" as a sub-harmonic mixer [7], multi-tanh input stage, [9] and improved 45° phase shifter. Its block diagram is shown in Fig. 1. Section II contains an analysis of the *multi-tanh* circuit and the effects of phase error on the LO rejection of the sub-harmonic mixer. An improved 45° phase shifter is discussed in Section III. Ideally, there is no second-order distortion for a fully balanced mixer. In practice, imperfections in the circuit symmetry and the duty-cycle of the LO signals result in a small second-order distortion. The second-order distortion will be addressed in Section IV. The fabricated circuit exhibits excellent dynamic range and reduced sensitivity to LO injection at the input port. Furthermore, we examine the effects of base germanium concentration on the performance of the circuit in Section V, and demonstrate that increasing germanium concentration in the base leads to improved noise figure and gain, without having a significant impact on intermodulation performance or power dissipation. The experimental results are also discussed in Section V.

II. Two-Level Sub-Harmonic Mixer Design

The two-level mixer is the key component of the direct conversion receiver. Fig. 2 shows the simplified schematic of the circuit. It is composed of two stages of a double-balanced switching cell ($T3$–$T10$) and a *multi-tanh* linearized input differential pair ($T1$–$T2$). The two stages of double-balanced switching provide for an effective doubling of the LO frequency if the switching phases are offset by 90°. The *multi-tanh* input cell improves the third-order input intercept point (IIP3) of the circuit [9], at the expense of a somewhat higher noise figure. The next two Sections will analyze the performance of the mixer.

A. Analysis of the Multi-Tanh Differential Input Cell

By using a *multi-tanh* differential pair, we can extend the voltage capacity of the mixer input at the expense of a small increase in noise and input capacitance, thereby increasing the dynamic range at the input [9]. The *multi-tanh* linearized differential pair is comprised of three differential pairs with their inputs and outputs in parallel, as shown in Fig. 2. The junction areas were optimized to obtain the best dynamic range. In this case, the emitter areas of $T1a$ and $T2a$ are set equal, and the emitter areas of $T1c$ and $T2b$ are set A times larger than the

Manuscript received November 8, 1999; revised January 12, 2000. This work was supported by the National Science Foundation sponsored ICAS Center and by a University of California Micro Program sponsored by AMCC.

The authors are with the Electrical and Computer Engineering Department, University of California at San Diego, La Jolla, CA 92093 USA.

Publisher Item Identifier S 0018-9200(00)05925-4.

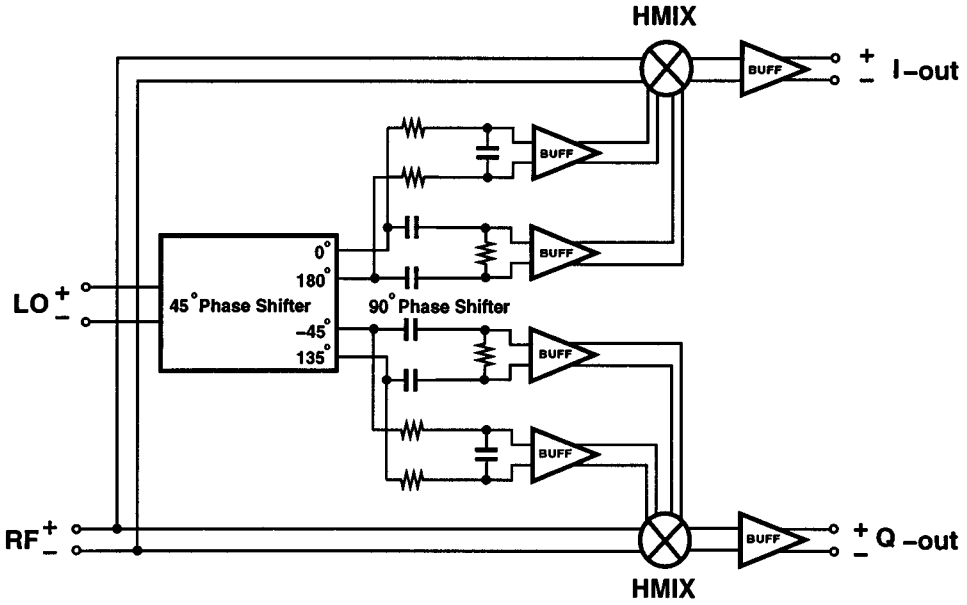


Fig. 1. Si/SiGe HBT direct-downconversion receiver implemented with a sub-harmonic mixer. The mixers are driven in *half-quadrature* with respect to each other.

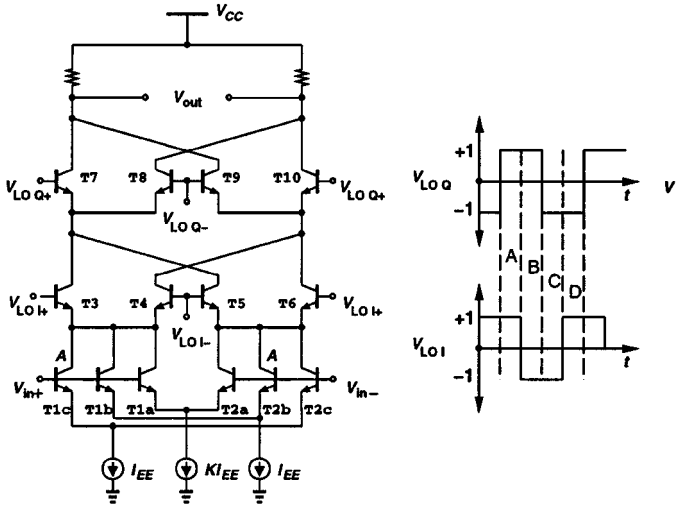


Fig. 2. Simplified schematic of the sub-harmonic mixer.

emitter areas of $T1b$ and $T2c$. The bias current of the center transistors $T1a$ and $T2a$ are optimized to be K times the outer bias current to obtain the best linearization. The overall emitter areas are then optimized to obtain the best noise performance.

The transconductance of a single bipolar differential pair biased at tail current I_{EE} is

$$G_m(V_{\rm in}) = \frac{dI_{\rm out}}{dV_{\rm in}} = \frac{I_{EE}}{2V_T}\,\mathrm{sech}^2\left(\frac{V_{\rm in}}{2V_T}\right) \tag{1}$$

and the composite G_m of the *multi-tanh* input circuit in Fig. 2 is

$$G_m(V_{\rm in}) = \frac{I_{EE}}{2V_T}\left(K\mathrm{sech}^2\,\frac{V_{\rm in}}{2V_T} + \mathrm{sech}^2\,\frac{V_{\rm in}+V_{os}}{2V_T} + \mathrm{sech}^2\,\frac{V_{\rm in}-V_{os}}{2V_T}\right) \tag{2}$$

where

$$V_{os} = V_T\,\ln(A). \tag{3}$$

For a small-signal input, the transconductance of the *multi-tanh* input is

$$G_{m0} = G_m(0) = \frac{I_{EE}}{2V_T}\cdot\frac{K(1+A)^2+8A}{(1+A)^2}. \tag{4}$$

To minimize distortion, we need to optimize the current ratio K and the transistor size ratio A. The composite G_m of the *muti-tanh* circuit with $A = 13$ and $K = 0.75$, along with the G_m of a simple differential pair, is shown in Fig. 3. The peak composite G_m is 2.19 times smaller than the G_m of a single pair with the same total current. The voltage capacity of the *multi-tanh* input is approximately l20 mV peak-to-peak, instead of approximately 8 mV if a single differential pair is used, where the voltage capacity is defined as the input voltage range in which the gain variation of a simple differential pair or *muti-tanh* circuit is less than 0.05 dB.

The use of the *multi-tanh* approach also has an impact on the noise performance of the mixer. For simplicity, we assume that the dominant noise is the shot noise current $\sqrt{2qI_C}$ at the collector operating on the incremental emitter resistance V_T/I_E. The total input-referred noise of the *multi-tanh* differential pair can then be shown to be

$$V_{\rm noise} = 2V_T\sqrt{\frac{2q}{I_{EE}}}\,\frac{1+A}{\sqrt{K(1+A)^2+8A}}. \tag{5}$$

The relative noise amplitude for varying area ratio A, with optimized K, is shown in Fig. 4. With the parameters $K = 0.75$ and $A = 13$, the noise amplitude is approximately 1.46 times larger than that of a single differential pair with the same total current, or the noise power of the *multi-tanh* input is 3.3 dB higher. With $A = 13$ and $K = 0.75$, $V_{1\,\rm dB}$ increases by approximately 10 dB [9]. As a result, the dynamic range of the

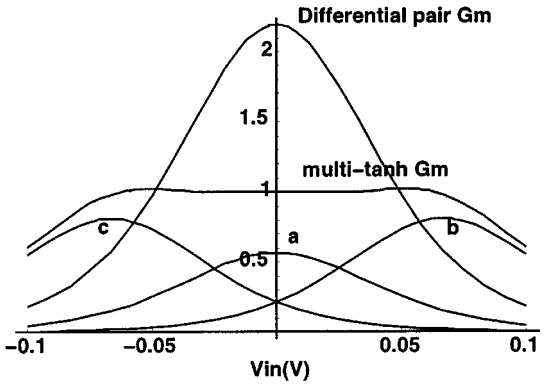


Fig. 3. Normalized G_m of *multi-tanh* differential pair of Fig. 2, compared to a traditional differential pair operated at the same total current.

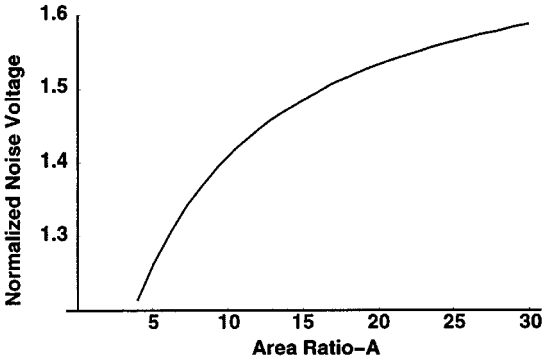


Fig. 4. Normalized noise voltage of *multi-tanh* differential pair of Fig. 2 with optimum K compared to a traditional differential pair operated at the same total current.

circuit is increased by roughly 7 dB. This noise versus linearity tradeoff is acceptable for a downconversion mixer application, where input linearity is especially important.

B. Analysis of Phase Error and Duty-Cycle Error of the Sub-Harmonic Mixer

The sub-harmonic mixing is realized with two stages of a Gilbert switching cell, as shown in Fig. 2. The upper stage is composed of $T7$–$T10$, the lower stage is composed of $T3$–$T6$. Both stages are driven by an LO signal whose frequency is half that of the frequency driving the conventional downconversion mixer. As a result, the output voltage can be expressed as

$$V_{\text{out}}(t) = V_{\text{in}}(t) \cdot V_{\text{LO}-Q}(t) \cdot V_{\text{LO}-I}(t) \tag{6}$$

where $V_{\text{LO}-Q}$ and $V_{\text{LO}-I}$ are the voltages driving the upper and lower switching cells respectively. $V_{\text{LO}-Q}$ and $V_{\text{LO}-I}$ are ideally 90° out of phase. V_{LO}—the product of $V_{\text{LO}-Q}$ and $V_{\text{LO}-I}$—is the same square wave used in a conventional mixer, with amplitude of unity and period of T as shown as a solid line in Fig. 5.

In a homodyne receiver, the RF signal is directly downconverted to baseband. Since the LO signal has the same frequency as the RF signal in a conventional homodyne mixer design, the LO signal is spectrally indistinguishable from the RF signal. The LO signal is also downconverted to dc, which causes a serious

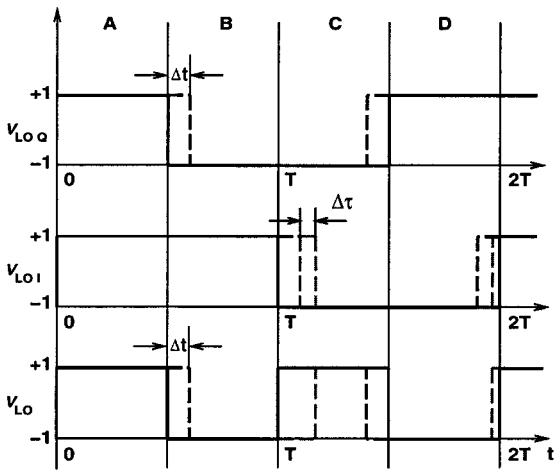


Fig. 5. Phase of LO signals, showing duty-cycle errors (Δt) and phase mismatch between I and Q phases of the mixer (Δr).

dc offset problem. In this harmonic downconverter, the LO frequency is one-half the desired RF frequency. If the phases of the two LO signals are matched ideally, the reception of the LO radiation will not cause a dc offset. However, imperfections in the circuit and signal matching can also cause the LO signal (at half of the RF frequency) to be downconverted to dc. The LO rejection reflects the immunity to this problem, and is defined by

$$LOR = \frac{\text{Conversion Gain at RF Frequency}}{\text{Conversion Gain at LO Frequency}}. \tag{7}$$

In a conventional homodyne mixer, self-mixing is unavoidable and the $LOR = 0$ dB. In this design, if the transistors and phases of $V_{\text{LO}-I}$ and $V_{\text{LO}-Q}$ are perfectly matched, the LO rejection will be infinity and no LO signal will be downconverted. However, the phase error of the LO signal causes an LO signal at the RF input port to be downconverted to dc.

The RF conversion gain is defined as

$$G_c = \frac{V_{\text{out}}(\omega_0)}{V_{\text{in}}(\omega_0)} \tag{8}$$

where $V_{\text{out}}(\omega_0)$ is the amplitude of the output signal at dc with an input frequency of ω_0, $V_{\text{in}}(\omega_0)$ the amplitude of the input signal at frequency ω_0. The quantity V_{out} is given by

$$V_{\text{out}}\left(\omega_{V_{\text{in}}}\right) = \frac{1}{2T}\int_0^{2T} V_{\text{in}} \sin\left(\omega_{V_{\text{in}}} t\right) \cdot g_m R \cdot V_{\text{LO}}\, dt \tag{9}$$

where $V_{\text{LO}} = V_{\text{LO}-I} \cdot V_{\text{LO}-Q}$. Substituting $\omega_{\text{RF}} = \omega_{\text{LO}}$ and $\omega_{\text{RF}} = 2\omega_{\text{LO}}$ into (9), the amplitudes of the output signal at dc due to the two signals (the desired and LO) are

$$V_{\text{out}}(\omega_{\text{LO}}) = \frac{2}{\pi}\sin\left(\frac{\Delta t}{T}\pi\right)\left(1+\sin\left(\frac{\Delta\tau}{T}\pi\right)\right) \cdot g_m R \cdot V_{\text{in}}(\omega_{\text{LO}}) \tag{10a}$$

$$V_{\text{out}}(2\omega_{\text{LO}}) = \frac{2}{\pi}\cos\left(\frac{\Delta t}{T}2\pi\right)\cos^2\left(\frac{\Delta\tau}{T}\pi\right) \cdot g_m R \cdot V_{\text{in}}(2\omega_{\text{LO}}) \tag{10b}$$

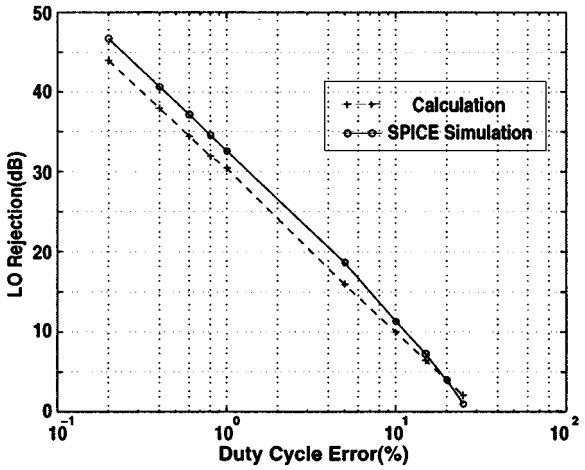


Fig. 6. Comparison of simulated and calculated LO rejection versus duty-cycle error.

where Δt is the time error due to the duty-cycle error of $V_{\mathrm{LO}-I}$ and $V_{\mathrm{LO}-Q}$, and $\Delta\tau$ is the time error caused by the phase difference between I and Q not being exactly equal to 90°, where

$$\Delta\tau = \frac{\Delta\theta}{\pi} T \tag{11}$$

where $\Delta\theta$ is phase difference error between I and Q. Refer to Fig. 5 for an illustration of these timing errors.

Substituting (10) into (7), the LO rejection is

$$LOR = \frac{\cos\left(\frac{\Delta t}{T} 2\pi\right) \cos^2\left(\frac{\Delta\tau}{T}\pi\right)}{\sin\left(\frac{\Delta t}{T}\pi\right)\left(1+\sin\left(\frac{\Delta\tau}{T}\pi\right)\right)} \cong \frac{T}{\Delta t \pi}. \tag{12}$$

Therefore, the LO rejection is relatively insensitive to the phase difference error between $V_{\mathrm{LO}-I}$ and $V_{\mathrm{LO}-Q}$; it is primarily a function of the duty-cycle error of $V_{\mathrm{LO}-I}$ and $V_{\mathrm{LO}-Q}$. Fig. 6 is a plot of the SPICE simulated and calculated LO rejection versus duty-cycle error, where

$$\text{Duty Cycle Error} = \frac{\Delta t}{T}. \tag{13}$$

The agreement between the two is excellent, demonstrating the accuracy of (12).

There are some potential drawbacks to this sub-harmonic mixer approach compared to a standard mixer. In particular, the power required for the LO is roughly double what is required for a standard double-balanced mixer. In addition, the noise distortion contribution of the upper switching pair is also increased, although the effect is usually small [11]. The two-level mixer design is also limited to approximately 2.5-V power supply voltage or greater, due to the extra devices in series compared to a standard double-balanced mixer configuration.

III. Broadband Phase Shifter Design

The realization of a broadband 45° phase shift circuit represents similar challenges to that encountered with the realization of a broadband 90° phase shift in traditional quadrature downconversion circuits. Fig. 7 shows a simplified schematic of the broadband 45° phase shifter [8]. If the parameters of the 45° phase shifter are chosen as

$$R_1 = 8R_2, \quad R_4 = 8R_3 \tag{14a}$$

$$R_1 C_1 = R_2 C_2 = 1/(2\pi f_1) \tag{14b}$$

$$R_3 C_3 = R_4 C_4 = 1/(2\pi f_2) \tag{14c}$$

where f_1 and f_2 are approximately the lower and higher frequency limits of operation, respectively.

Then

$$|V_I| = |V_Q| = \tfrac{1}{2}|V_{\mathrm{in}}| \tag{15}$$

where

$$V_I = V_{\mathrm{out}<0} - V_{\mathrm{out}<180}$$
$$V_Q = V_{\mathrm{out}<-45} - V_{\mathrm{out}<135}.$$

The phases of the output voltages are

$$\Phi_Q = \tan^{-1}\frac{12F_1(1-F_1^2)}{F_1^4 - 38F_1^2 + 1} \tag{16a}$$

$$\Phi_I = \tan^{-1}\frac{12F_2(1-F_2^2)}{F_2^4 - 38F_2^2 + 1} \tag{16b}$$

where $F_1 = f/f_1$ and $F_2 = f/f_2$ are normalized frequencies. In this case, we chose $f_1 = 400$ MHz and $f_2 = 1230$ MHz to achieve operation in the 1–2-GHz frequency range, and the calculated phase difference between the I and Q channels is shown in Fig. 8. Further optimization to decrease the phase error is possible at the expense of greater LO power loss. The curve of the phase difference between I and Q output has a relatively flat bottom at 700 MHz. This implies the element sensitivity is very low around the minimum point. If we assume that all resistors or capacitors in the phase shifter change by the same ratio, then the phase difference change at frequency f is

$$\Delta\Phi(f) = \left[\frac{12f_1(f^2+f_1^2)}{f^4+34f^2f_1^2+f_1^4} - \frac{12f_2(f^2+f_2^2)}{f^4+34f^2f_2^2+f_2^4}\right] \cdot \left(\frac{|\Delta R|}{R} + \frac{|\Delta C|}{C}\right) \tag{17}$$

where $\Phi = \Phi_I - \Phi_Q$ is the phase difference between I and Q signal. At $f = 700$ MHz and $f = 500$ MHz, a 10% change of resistors in the phase shifter network causes a phase error of 0.006° and 1°, respectively. The downconverter works in the RF frequency range from 1–2 GHz. So, the parameters were chosen such that the maximum phase difference error was less than 2° over the whole LO input frequency range. In this downconverter, 90° phase shifters were also used to generate the LO voltage, which is required in the process of sub-harmonic mixing. These 90° phase shifters add shunt impedance to the 45° phase shifters and cause the LO signal to be further attenuated and the phase deviated from the ideal. This effect was compensated by final parameter optimization through SPICE simulation. Although the conventional *RC* networks were used here to realize the 90° phase shift, by choosing proper f_1 and f_2 in (14), 90° and 135° can also be realized with a broadband phase shift network to alleviate LO attenuation and achieve near-zero amplitude distortion.

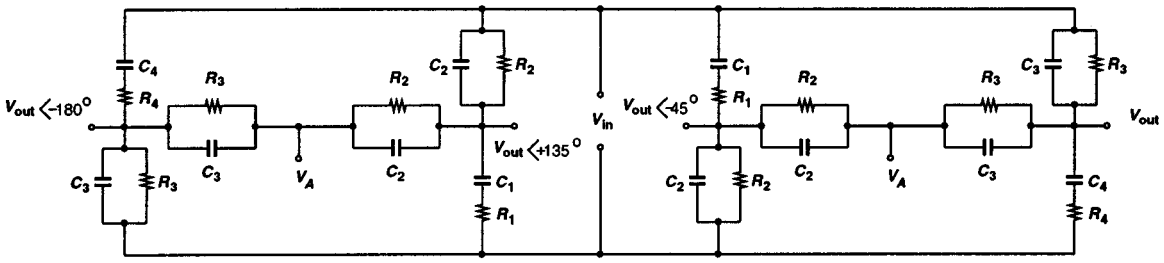


Fig. 7. Broadband 45° phase shifter.

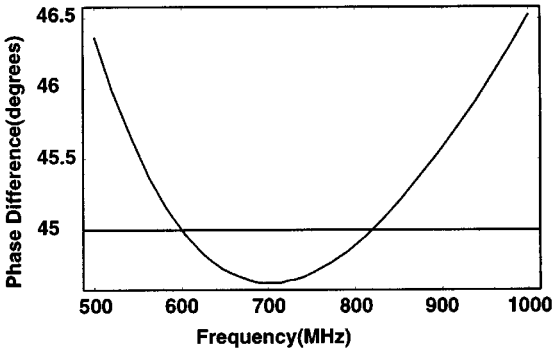


Fig. 8. Simulated phase difference of the LO signal applied to the phase-shift circuit of Fig. 7.

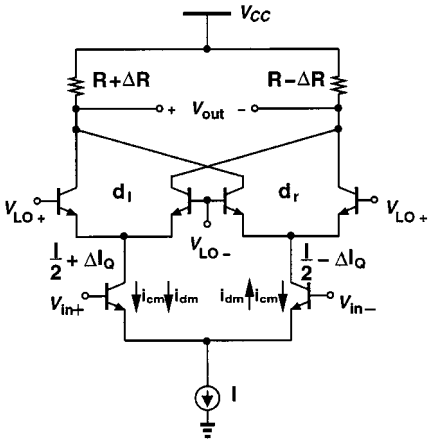


Fig. 9. Simplified schematic of bipolar double-balanced mixer, showing error sources for second-order intermodulation.

IV. Analysis of Mixer Second-Order Intercept Point Performance

One of the classic limitations on the use of direct conversion techniques for wireless communications is the necessity for an extremely high second-order input intercept point (IIP2). This requirement results from the observation that *all* interferers downconvert to dc—the IF—through a second-order distortion mechanism. As an example, the minimum sensitivity for the GSM system is −102 dBm, but the maximum *out-of-band* interferer can be as large as 0 dBm and the maximum *in-band* interferer can be as large as −20 dBm [12]. If limited by the in-band interferer, the resulting receiver IIP2 requirement exceeds +60 dBm; accounting for the gain of the preceding low-noise amplifier (LNA), the resulting IIP2 requirements on the mixer can exceed +70 dBm! Any ideal fully balanced structure generates no second-order distortion and has an infinite IIP2, but various mismatch effects throughout the circuit compromise the resulting performance. A simplified analysis of the effect of various mismatches on the IIP2 of a canonical doubly balanced mixer is a useful step to assess the effects of this issue.

In a bipolar circuit, the input differential pair can generate second-order distortion through the finite impedance of the current source and mismatch between the devices, as shown in Fig. 9. This second-order current consists of a common-mode portion—i_{cm}–and a differential portion—i_{dm}. Although the portion of i_{dm} due to finite current-source impedance is very small, the portion of i_{cm} due to finite current-source impedence is not negligible, and is given by

$$i_{cm} \cong \frac{\Delta v_{\text{in}}^2}{4V_T Z} + \frac{\Delta v_{\text{in}}^4}{16V_T^3 Z} \tag{18}$$

where Z is the shunt impedance to ground of the current source—ideally infinite and Δv_{in} is the differential input voltage.

Similarly, the effects of device mismatch—emitter area for example—generate a significant second-order i_{dm} component given by

$$i_{dm} \cong \frac{\Delta I_Q \Delta v_{\text{in}}^2}{2V_T^2} \tag{19}$$

where ΔI_Q is the difference in the dc bias of the emitter currents of the two input transistors.

Now, these two second-order distortion products are applied to the switching core, which can be viewed in the simplest case as two single-pole double-throw switches, operating with different duty cycles d_l and d_r. A harmonic mixer employs a second pair of these switches to double the effective LO frequency. The duty cycle of each pair differs from 0.5 due to duty-cycle errors in the LO generator, as well as device mismatch effects, and both effects can be described by d_l and d_r. The resulting *low-frequency* portion of the output current from the switching core applied to the load resistors can be approximated by

$$i_l \cong d_l(i_{cm} + i_{dm}) + (1 - d_r)(i_{cm} - i_{dm}) \tag{20a}$$

$$i_r \cong (1 - d_l)(i_{cm} + i_{dm}) + d_r(i_{cm} - i_{dm}) \tag{20b}$$

The error in the duty cycle can be expressed with respect to the mean duty cycle d and a duty cycle mismatch between the left and right branches (Δd), i.e., $d_l = d + \Delta d$ and $d_r = d - \Delta d$. The resulting output voltage results from the application of these

currents to load resistors, which themselves may be mismatched due to inevitable process variations, each being modeled as $R+\Delta R$ and $R-\Delta R$. The resulting output voltage is

$$v_{\rm out} \cong i_{cm}(2\Delta R + 4R\Delta d) + i_{dm}2R(1-2d). \tag{21}$$

This equation illustrates three of the most important sources of second-order distortion in the classic integrated circuit double-balanced mixer: resistor mismatch in the load and duty cycle mismatch in the switching core (both associated with i_{cm}), and overall duty-cycle errors (associated with i_{dm}). Inserting (18) and (19) into (21) yields

$$v_{\rm out_{2nd}} \cong \frac{\Delta v_{\rm in}^2 R}{V_T}\left[\frac{1}{2Z}\left(\left|\frac{\Delta R}{R}\right| + \left|\frac{\Delta d}{d}\right|\right) + \frac{I}{V_T}(1-2d)\left(\left|\frac{\Delta I_Q}{I}\right|\right)\right]. \tag{22}$$

This expression can be simplified further if the primary contributor to the nonzero output conductance of the current source is the Early voltage (i.e., $Z \approx V_A/I$). In this case

$$v_{\rm out_{2nd}} \cong \Delta v_{\rm in}^2 G_{ss}\left[\frac{1}{V_A}\left(\left|\frac{\Delta R}{R}\right| + \left|\frac{\Delta d}{d}\right|\right) + \frac{2(1-2d)}{V_T}\left(\left|\frac{\Delta I_Q}{I}\right|\right)\right] \tag{23}$$

where G_{ss} is the small-signal gain of the basic differential pair without the intervening switching core.

This last expression can be used to estimate the second-order input intercept point of the mixer as a result of all of the various sources of mismatch error. If the nonlinear transfer function of the mixer—defined as the IF output in response to an RF input—is given by

$$v_{\rm out} \cong (G_{ss}/2)\Delta v_{\rm in} + G_{ss} \cdot \left[\frac{1}{V_A}\left(\left|\frac{\Delta R}{R}\right| + \left|\frac{\Delta d}{d}\right|\right) + \frac{2(1-2d)}{V_T}\left(\left|\frac{\Delta I_Q}{I}\right|\right)\right]\Delta v_{\rm in}^2 \tag{24}$$

then the IIP2 (in volts) of the mixer is

$$\text{IIP2} \cong \left[2\left[\frac{1}{V_A}\left(\left|\frac{\Delta R}{R}\right| + \left|\frac{\Delta d}{d}\right|\right) + \frac{2(1-2d)}{V_T}\left(\left|\frac{\Delta I_Q}{I}\right|\right)\right]\right]^{-1}. \tag{25}$$

As a typical example, assuming fractional matching of all components of approximately 1%, an Early voltage of 100 V, and a duty cycle of 0.49, the resulting IIP2 amplitude is approximately 30 V—or 38 dBm in a 50-Ω system, well short of the most aggressive wireless system specifications. This result illustrates the great importance of nearly perfect device matching and a high current-source impedance to achieve the best possible IIP2 from a traditional double-balanced mixer design. These considerations also apply to the sub-harmonic mixer of Fig. 2.

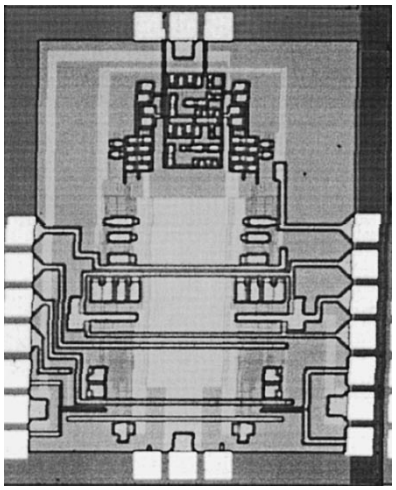


Fig. 10. Die photograph of the sub-harmonic direct conversion receiver.

TABLE I
SUMMARY OF DEVICE ELECTRICAL CHARACTERISTICS [13]

Performance	Si (BJT)	SiGe Control	14% Peak	18% Peak
β at V_{BE}=0.72V	67	114	350	261
$V_A(V)$	19	60	58	113
BV_{CEO}(V)	3.5	3.2	2.7	2.7
$R_{bi}(k\Omega/\square)$	12.8	9.8	10.3	10.7
Peak f_T (GHz)	38	52	52	57
Peak f_{MAX} (GHz)	57	64	63	67

V. EXPERIMENTAL RESULTS

The key performance issues for the direct conversion receiver are the gain, double-sideband (DSB) noise figure, intermodulation distortion, 2 × LO leakage to the input port, and rejection of the LO at the input port. Fig. 10 is a die photograph of the balanced sub-harmonic downconverter, and the measurement setup is shown in Fig. 11. Each downconverter was evaluated at a dc voltage of 3.3 and 2.5 V and an LO power of approximately 10 dBm, and was tuned to achieve optimum double-sideband noise figure and gain at a given bias point and input frequency. The IIP2 and IIP3 were measured with a two-tone test, where the two input tones were offset by 50 kHz and 59 kHz from $2f_{lo}$.

The performance of the downconverter was evaluated in a 0.5-μm Si/SiGe heterojunction bipolar transistor (HBT) process with differing peak alloy concentrations of germanium in the base, which varied from a peak of 18% to 0% in the homojunction case. This allowed us to examine the effects of optimization of the device technology on circuit performance for this small-signal RF application. A summary of the differing device characteristics is shown in Table I [13]. As described in [13], the effective strain in the three HBT cases was limited to 0.1%, while the peak germanium concentration was progressively moved away from the neutral collector region and toward the emitter–base junction. This is intended to improve the current gain at low collector current densities, which is desirable for small-signal RF as opposed to high-speed digital applications. This resulted in some improvement of single-device minimum noise figure in the 1–2-GHz frequency range.

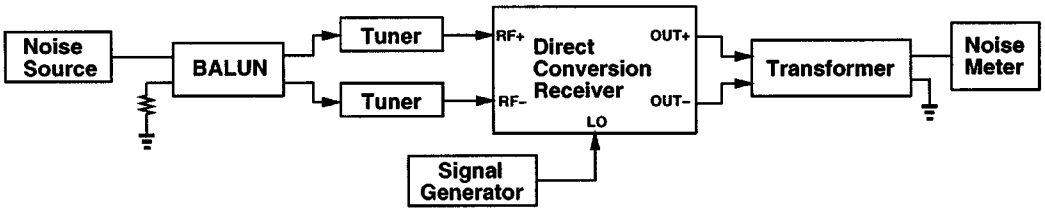


Fig. 11. Measurement setup.

TABLE II
MEASURED DOWNCONVERTER SUMMARY. $T_A = 25$ °C

Profile	Vcc(V)	I_{mix}(mA)	f_{RF}(GHz)	Gain(dB)	NF(dB)	IIP_2(dBm)	IIP_3(dBm)
Std.	3.3	2.77	1.0	19.2	7.3	35.0	-7.5
	2.5	1.76	1.0	14.8	9.0	35.7	-7.8
	3.3	2.77	2.0	17.2	9.8	31.7	-5.1
	2.5	1.76	2.0	13.5	10.4	29.7	-3.5
14%	3.3	2.95	1.0	20.6	7.2	34.7	-4.9
	2.5	1.89	1.0	15.8	9.8	37.2	-1.1
	3.3	2.95	2.0	18.9	9.0	31.0	-3.9
	2.5	1.89	2.0	14.2	10.6	29.7	-3.9
18%	3.3	2.83	1.0	19.5	7.0	33.6	-8.7
	2.5	1.80	1.0	15.1	8.4	34.0	-5.4
	3.3	2.83	2.0	17.0	9.7	29.9	-5.7
	2.5	1.80	2.0	13.0	10.5	27.0	-4.6
Si	3.3	2.55	1.0	17.4	8.3	31.0	-8.3
	2.5	1.64	1.0	13.5	9.6	34.3	-6.4
	3.3	2.55	2.0	13.6	11.9	44.7	-5.6
	2.5	1.64	2.0	10.9	12.6	36.6	-4.6

The general performance of the direct sub-harmonic mixers fabricated with different germanium concentration is listed in Table II. The best circuit performance was measured with the peak concentration of the germanium in the base of 14%—the gain at both 1 GHz and 2 GHz was slightly higher than that of the other profiles. This was consistent with the single-device performance comparison for these same devices reported in [13]. As expected, the Si homojunction profile exhibited the worst performance, with nearly 2 dB lower gain and approximately 1 dB higher noise figure. However, the homojunction devices exhibited intermodulation performance—both IIP2 and IIP3—comparable to the heterojunction devices, indicating that the presence of germanium in the base had little effect on distortion. Once again, this is consistent with the single-device results reported in [13].

The circuit requires a relatively high LO power of approximately 10 dBm due to the losses inherent in the phase shifting network. Fig. 12 plots the phase difference between the I and Q channels, which is double the phase difference of the 45° phase shift network, as a function of LO frequency. The measured worst-case phase error is approximately 3.5° over an entire octave frequency range as the LO frequency changes from 500 MHz to 1 GHz, corresponding to an RF frequency of 1–2 GHz. Although larger than desired, this error can be reduced through subsequent adaptive equalization—unlike quadrature errors in image-rejection mixers [14].

Table III summarizes the measured variation in the LO rejection (the IF output in response to an input at the LO frequency) of each of the different base profiles. As was demonstrated in (12), the LO rejection depends on the duty-cycle error of $V_{\mathrm{LO}I}$, and $V_{\mathrm{LO}Q}$, and it will also depend on the degree of balance within the circuit. Therefore, it is expected to degrade somewhat at higher frequencies. The LO rejection is measured with a 10-dBm input LO power at 500 MHZ and −30 dBm RF power (at the LO frequency). The maximum LO rejection was observed to be 39 dB at an LO frequency of 500 MHz, dropping to slightly better than 30 dB at 1 GHz. These results are a dramatic improvement over traditional homodyne architectures, which have an LO rejection of 0 dB by definition.

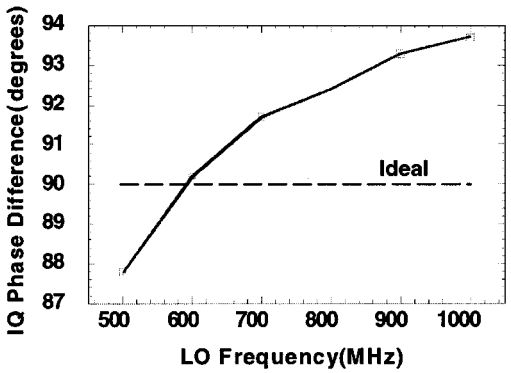


Fig. 12. Measured phase difference between I and Q channels on standard profile devices.

TABLE III
MEASURED LO REJECTION

Profile	$f_{LO} = 500MHz$	$f_{LO} = 1GHz$
Std.	36.8	35.0
14%	39.8	30.8
18%	37.8	35.6
Si	39.4	32.3

TABLE IV
2 × LO LEAKTHROUGH TO RF INPUT PORT

$P_{LO}(f_{LO})$	$11.7dBm(500MHz)$	$13.8dBm(1GHz)$
	Isolation at $1GHz$(dB)	Isolation at $2GHz$(dB)
Std.	71.4	75.6
14%	66.9	75.1
18%	71.0	74.1
Si	71.5	74.3

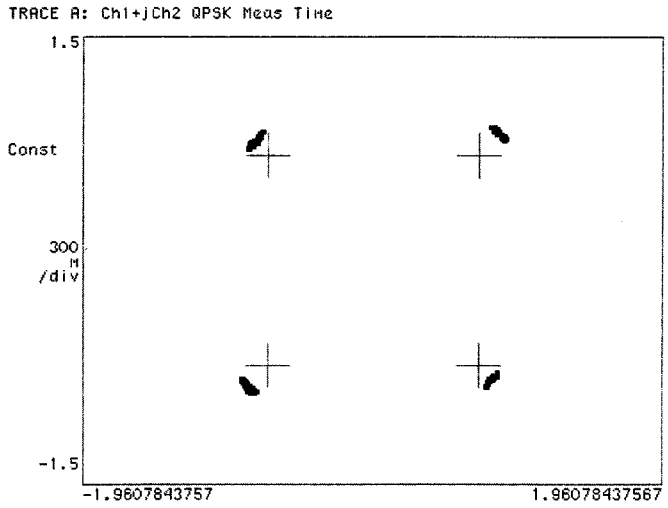


Fig. 13. Measured constellation of QPSK signal, $f_{\rm data} = 30$ kb/s.

Finally, the leakage at the output of the RF port at *twice* the LO frequency ($f_{\rm RF}$) was measured, in order to estimate the magnitude of the LO re-radiation problem. The result is listed in Table IV. This effect is a well-known and serious limitation to a direct conversion receiver. It is expected that this effect would be reduced compared to a standard homodyne architecture, but not as dramatically as with the LO rejection. This is due to the fact that there is a substantial second-order component of the local-oscillator oscillator, which appears at the collector of transistors $T1$–$T2$ in Fig. 2. The use of the *multi-tanh* approach raises the collector–base capacitance coupling to the RF input port, raising the coupling of the 2 × LO signal to the input. This effect could be reduced by the use of a cascode transistor pair between $T1$–$T2$ and $T3$–$T6$ in Fig. 2, albeit at the expense of extra power dissipation. The inherent balance in the circuit will reject a good portion of this signal, but any imbalance will raise the signal level dramatically. Typical measured LO–RF leakage was approximately −70 dB at an LO power of approximately 12 dBm, leading to a re-radiated 2 × LO power of approximately −60 dBm. The reverse isolation of the LNA driving this stage should reduce the level of this power delivered to the antenna to an insignificant level in most cases.

Fig. 13 demonstrates the measured constellation diagram of a 30 kb/s QPSK waveform downconverted by the circuit. The accuracy of the phase shifting circuit is clearly evident from the result.

VI. CONCLUSIONS

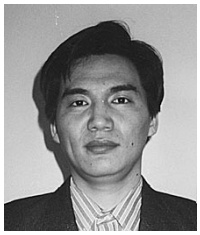
A direct conversion sub-harmonic mixer/downconverter has been presented in a Si/SiGe HBT technology, suitable for broadband downconversion of signals in the 1–2-GHz frequency range. An improved 45° phase shifting network was presented that produced a highly accurate phase shift over a broad range of frequencies. The effect of phase error and duty-cycle error on the performance and LO rejection of the downconverter were evaluated, and the effect of device mismatch on mixer second-order intermodulation was discussed. The effect of varying the Ge concentration in the base at a constant strain level was evaluated, and it was demonstrated that a modest improvement in performance could be achieved through increasing the concentration of germanium at the emitter–base junction. The circuit demonstrated outstanding performance at a relatively low dc power consumption of 5–9 mW per mixer. A DSB noise figure of approximately 7 dB, an IIP2 of +35 dBm, an IIP3 of −5 dBm, and a LO rejection of 35 dB were achieved.

ACKNOWLEDGMENT

The authors acknowledge support of Dr. D. Harame, Dr. J. Moniz, Dr. D. Nquyen-Noc, and Dr. R. Johnson at IBM for wafer fabrication, and Dr. G. Niu and Prof. J. Cressler of Auburn University for the device measurement data presented in Table I and valuable discussions. The authors also acknowledge valuable discussions with J. Groe of Nokia, S. Rosenbaum of Hughes Network Systems, D. Kelly of Peregrine Semiconductor, Prof. I. Galton of the University of California at San Diego (UCSD), and D. Rowe of Sierra Monolithics. The authors also acknowledge generous help from J. Fairbanks of UCSD on the circuit measurements.

REFERENCES

[1] B. Razavi, "Challenges and trends in RF design," in *9th Annu. IEEE Int. A SIC Conf. and Exhibit*, 1996, pp. 81–86.
[2] A. A. Abidi, "Direct-conversion radio transceivers for digital communications," *IEEE J. Solid-State Circuits*, vol. 30, pp. 1399–410, Dec. 1995.
[3] V. Comino, "A baseband integrated circuit for homodyne cordless phones," *IEEE 1998 Custom Integrated Circuits Conf.*, pp. 423–426, 1998.
[4] K. Itoh *et al.*, "A 40-GHz band monolithic even harmonic mixer with an antiparallel diode pair," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1991, pp. 879–882.
[5] ——, "Unbalance effects of an antiparallel diode pair on the virtual local leakage in an even harmonic mixer," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1998, pp. 857–60.
[6] T. Yamaji and H. Tanimoto *et al.*, "An I/Q active balanced harmonic mixer with IM2 cancelers and a 45 degrees phase shifter," *IEEE J. Solid-State Circuits*, vol. 33, pp. 2240–46, Dec. 1998.
[7] J. Choma, "A three-level broadbanded monolithic analog multiplier," *IEEE J. Solid-State Circuits*, vol. SC-16, no. 4, pp. 392–9, 1981.
[8] R. S. Carson, *Radio Communications Concepts: Analog*, 1989.
[9] B. Gilbert, "The multi-tanh principle: A tutorial overview," *IEEE J. Solid-State Circuits*, vol. 33, pp. 2–17, Jan. 1998.
[10] D. Harame, "Si/SiGe epitaxial-base transistors—Part 2: Proces integration and analog applications," *IEEE Trans. Electron Devices*, vol. 42, pp. 469–482, Mar. 1998.
[11] J. R. Long and M. A. Copeland, "A 1.9 GHz low-voltage silicon bipolar receiver front-end for wireless personal communications systems," *IEEE J. Solid-State Circuits*, vol. 30, pp. 1438–48, Dec. 1995.
[12] P. C. Davis, "Merits and requirements of a few RF architectures," in *1999 Bipolar/BiCMOS Circuits and Technology Meeting*, 1999, pp. 62–66.
[13] G. Niu and J. D. Cressler *et al.*, "SiGe profile design tradeoffs for RF circuit applications," in *IEDM99*, 1999.
[14] S. Lee and W. Song *et al.*, "A 1 GHz image-rejection down-converter in 0.8 μm CMOS technology," *IEEE Trans. Consumer Electron.*, vol. 44, no. 2, pp. 235–9, 1998.

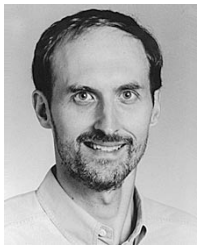


Liwei Sheng was born in Liaoning, China, in 1971. He received the B.S. and M.S. degree in electrical engineering from Beijing University, Beijing, China, in 1994 and 1997, respectively. He is currently working toward the Ph.D. degree at the University of California, San Diego.

His research concerns high-frequency integrated circuit for wireless communications.

Jonathan C. Jensen (S'00) received the B.S. degree in physics from the University of California, Santa Cruz, in 1992. He received the M.S. degree in electrical engineering from the University of California, San Diego, in 1999, where he is currently working toward the Ph.D. degree.

During the summer of 1997 he was with Sierra Monolithics, Redondo Beach, CA. In the summer of 1999 he was with Nokia Mobile Phones, San Diego, CA, where he worked with the RF/Analog IC Design group. His research interest is high-frequency integrated circuits for wireless communications.



Lawrence E. Larson (M'86–SM'90–F'00) received the B.S. degree in electrical engineering and the M.Eng. degree from Cornell University, Ithaca, NY, in 1979 and 1980, respectively. He received the Ph.D. degree in electrical engineering from the University of California, Los Angeles, in 1986.

He joined Hughes Research Laboratories, Malibu, CA, in 1980, where he directed work on high-frequency InP, GaAs, and silicon integrated circuit development for a variety of radar and communications applications. While at Hughes, he led the team that developed the first MEMS-based circuits for RF and microwave applications. He was also Assistant Program Manager of the Hughes/DARPA MIMIC Program from 1992 to 1994. From 1994 to 1996, he was with Hughes Network Systems, Germantown, MD, where he directed the development of radio-frequency integrated circuits for wireless communications applications. He joined the Faculty at the University of California at San Diego (UCSD) in 1996, where he is the inaugural holder of the Communications Industry Chair. He is currently Co-Director of the UCSD Center for Wireless Communications. He has published more than 100 papers and has received 21 U.S. patents.

Dr. Larson was a corecipient of the 1996 Lawrence A. Hyland Patent Award of Hughes Electronics for his work on low-noise millimeter-wave HEMTs.