$$IRR_{conventional} = 10\log\frac{(1+\cos\Delta\theta)}{(1-\cos\Delta\theta)} \quad [\text{dB}] \qquad (1)$$

where $\Delta\theta$ is the phase error of the local oscillator (LO).

$$IRR_{proposed} = 10\log\frac{(1+\cos\Delta\theta_1)(1+\cos\Delta\theta_2)}{(1-\cos\Delta\theta_1)(1-\cos\Delta\theta_2)} \quad [\text{dB}] \qquad (2)$$

where $\Delta\theta_1$ and $\Delta\theta_2$ are the phase errors of the RF signal and LO, respectively.

As a function of the path-gain mismatch, the IRRs given by

$$IRR_{conventional} = 20\log\left(\frac{2+\Delta A}{\Delta A}\right) \quad [\text{dB}] \qquad (3)$$

$$IRR_{proposed} = 20\log\left(\frac{4+\Delta A_1}{\Delta A_1}\right) \quad [\text{dB}] \qquad (4)$$

where ΔA and ΔA_1 are the gain mismatches of the conventional topology and proposed topology, respectively.

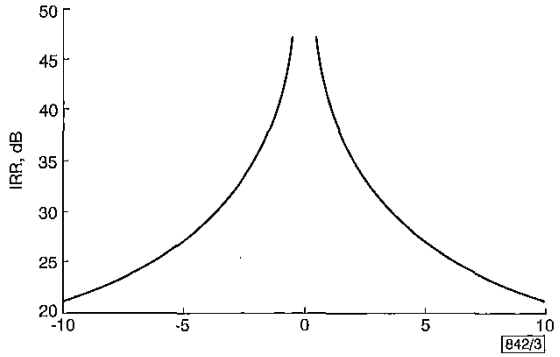

Fig. 3 *IRR against phase error of conventional topology*

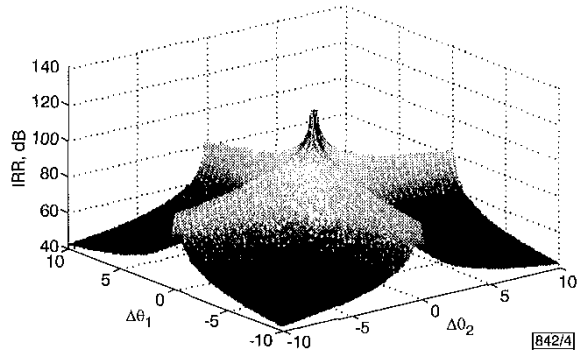

Fig. 4 *IRR against phase error of proposed topology*

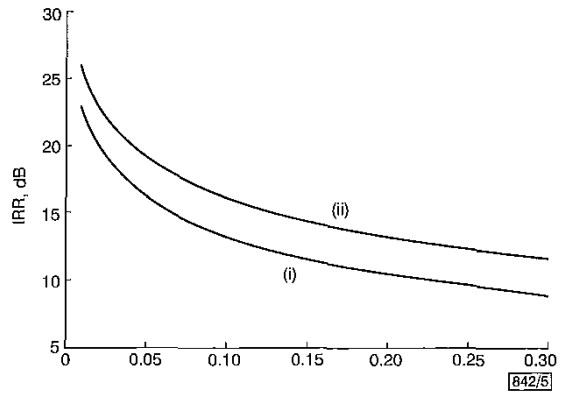

Fig. 5 *IRR against gain mismatch*

(i) conventional topology
(ii) proposed topology

Discussions on performance of image rejection: From eqns. 1 and 2, we obtained Figs. 3 and 4. From Figs. 3 and 4, we can conclude that the phase error requirements in the proposed topology are considerately reduced in contrast to that for a single-quadrature topology. For example, in the single-quadrature topology, the IRR is 41dB when $\Delta\theta$ is equal to 1°. In the double-quadrature topology, however, to obtain the same IRR, both $\Delta\theta_1$ and $\Delta\theta_2$ are increased to 10°. On the other hand, the IRR of the double-quadrature topology is doubled to 82dB when $\Delta\theta_1$ and $\Delta\theta_2$ are 1°. So, with the proposed topology the sensitivity of the IRR to phase errors in the quadrature channels can be greatly reduced.

In addition, we can obtain Fig. 5 from eqns. 3 and 4. From Fig. 5, we can see that the IRR against gain mismatch characteristics of the new topology are inherently superior to those of the conventional zero-IF topology by ~6dB.

Conclusions: A new zero-IF receiver has been presented. The proposed receiver is less sensitive to phase errors in the quadrature channels and its IRR against gain mismatch characteristics are inherently superior to those for the conventional zero-IF topology by ~6dB. So, compared with the conventional zero-IF topology, the image-rejection performance of the new receiver is significantly increased.

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Bandpass delta-sigma class-S amplifier

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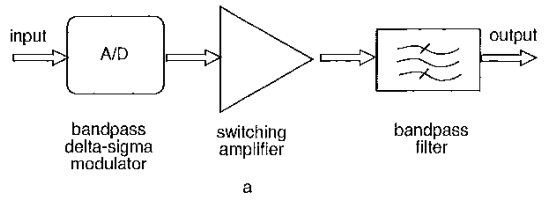
A class-S amplifier with a bandpass delta-sigma modulated input is demonstrated using CMOS devices at 10MHz. With a two-tone modulated input, third-order intermodulation products below –40dBc were measured, with an output power of 26dBm and a drain efficiency of 33%. This new amplifier topology demonstrates promising performance for simultaneously achieving high linearity and efficiency.

Introduction: Switching-mode power amplifiers have been of great interest due to their potential for high efficiency. However, a major drawback to these amplifiers is the inherent nonlinear nature of their outputs. In a class-S amplifier, this problem is resolved by driving the input with a pulsewidth-modulated (PWM) signal and filtering after the switching-mode amplifier [1]. Unfortunately, this technique becomes more complicated at higher frequencies due to the need for faster pulsewidth modulator switching speeds. In this Letter, we present a variation on the class-S amplifier in which the input is driven by a bandpass delta-sigma modulated signal. The concept of a bandpass delta-sigma

(BPDS) class-S amplifier has been previously proposed in [2]. A block diagram of the system is shown in Fig. 1*a*. An RF signal is converted to a digital signal by means of a BPDS modulator. The modulator is an A/D converter in which the quantisation noise is spectrally shaped to lie outside of the passband. This two-level (binary) signal is then fed into a switching amplifier and subsequently bandpass filtered. Since the BPDS signal is linear within a narrow bandwidth and the switching amplifier is a linear stage for digital signals, the filtered output should likewise be linear. With the combination of the modulator and switching amplifier, this simple amplifier topology has the potential to provide both high linearity and efficiency.



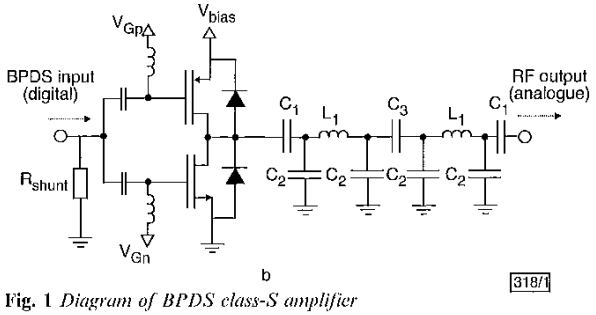


Fig. 1 *Diagram of BPDS class-S amplifier*

a Block diagram
b Schematic diagrams of switching amplifier and bandpass filter
Element values are L_1 = 2.5μH, C_1 = 84pF, C_2 = 163pF, and C_3 = 12pF

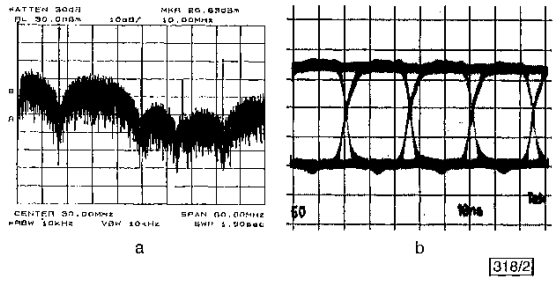


Fig. 2 *Output of switching amplifier*

a Spectrum (6MHz/div, centre = 30MHz and 10dB/div, reference level = 30dBm, attenuation = 30dB, span = 60.00MHz)
b Waveform (10ns/div and 5V/div

Design: A design frequency of 10MHz was selected for the demonstration circuit. At this frequency, a bandpass delta-sigma signal can be created from a preprogrammed pattern generator (HP 16522A) where the clock frequency is set at a rate four times the signal frequency (40MHz). Also, at this relatively low frequency, the switching amplifier can be realised with complementary FETs, avoiding the need for using baluns. Fig. 1*b* shows the circuit diagram of the switching amplifier and bandpass filter. The *n* and *p* channel FETs (ZETEX ZVN3306F and ZVP3306F) are in an inverter configuration, and the freewheeling diodes provide a current path when the corresponding transistors are off. The design of the filter is particularly important since insertion loss directly corresponds to reduction in efficiency and poor out-of-band rejection results in increased distortion from quantisation noise. Mica dielectric capacitors (Q > 300) and Micrometals toroid inductors (Q > 100) are used for their high Q values. The filter has an input impedance of 50Ω and was tuned to a centre frequency of 10MHz with an insertion loss of 0.8dB and 3dB bandwidth of 700kHz.

Owing to a small output power from the pattern generator, a preamplifier was necessary to supply the appropriate signal level to the input of the switching amplifier. A commercially available amplifier (Minicircuits ZHL-6A) with a bandwidth between 2.5kHz and 500MHz was used. A wide bandwidth preamplifier was necessary because the BPDS signal is broadband, and any significant lowpass or highpass filtering would corrupt the encoded signal. The resistor, R_{shunt} = 50Ω, was used to adjust the input drive of the switching amplifier.

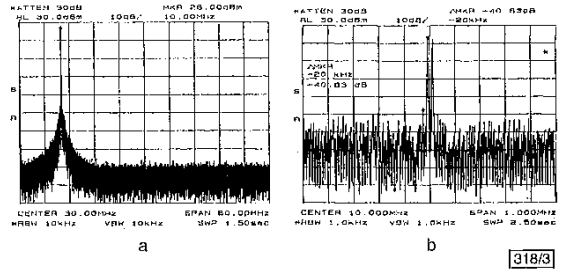


Fig. 3 *Spectral output of amplified signals*

a One-tone modulation (6MHz/div, centre = 30MHz and 10dB/div, reference level = 30dBm)
b Two-tone modulation separated by 20kHz (0.1MHz/div, centre = 10MHz and 10dB/div, reference level = 30dBm)

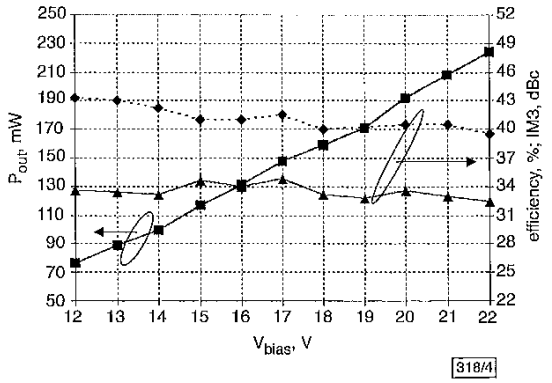


Fig. 4 *Output power per tone, IM3, and total drain efficiency against V_{BIAS}*

output power per tone
IM3
total drain efficiency

Measurements and discussion: The output (terminated with 50Ω) was measured using an HP8565E spectrum analyser. Fig. 2*a* shows the spectrum after the switching amplifier of a single-tone BPDS modulated signal at V_{BIAS} = 21V. Fig. 2*b* displays the time-domain waveform indicating that the amplified signal is digital. Fig. 3*a* shows the recovered signal after the bandpass filter. The measured power is 26.0dBm with a drain efficiency (η) of 30%, considering only the losses from the switching amplifier and filter. The gain of the switching amplifier and filter block is 10dB. Under the same bias conditions, two tones separated by 20kHz were encoded. The resultant output is shown in Fig. 3*b* where the third-order intermodulation product (IM3) is –40.8dBc at 23.0dBm per tone and η of 33%. To understand the effect of the output bias voltage, the output power, IM3, and η were measured as a function of V_{BIAS} (Fig. 4). The output power increases approximately in a quadratic manner as a function of V_{BIAS}, as expected. It is evident that the peak power level can be varied with V_{BIAS} without a significant change in linearity and efficiency.

The sources of the losses are due to several factors. These are (i) R_{DS} 'on' resistance of the FETs (p-FET = 10Ω); (ii) rise and fall times (~5ns); (iii) output capacitance; and (iv) filter insertion loss (0.8dB). If the entire system is accounted for, the power dissipated by the BPDS modulator and driver has to be considered. A high performance class-D amplifier with a sinusoidal input at 10MHz can perform with an efficiency of ~80% [3]. Significant improvements in efficiency are possible for the BPDS amplifier, including the use of devices with faster switching times and lower R_{DS}, a n-channel FET only design using baluns, and different filter topologies.

Conclusions: A bandpass delta-sigma class-S amplifier has been experimentally demonstrated at 10MHz. At a third-order intermodulation level of –40.8dBc, a drain efficiency of 33% and peak power of 23dBm per tone (26dBm total power) were measured. This combination of distortion and efficiency demonstrates the possibility of attaining both high linearity and efficiency in narrowband RF power amplifier applications.

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Differential CMOS edge-triggered flip-flop based on clock racing

Y. Moisiadis and I. Bouras

A differential CMOS edge-triggered flip-flop is proposed that employs a pair of cross-coupled inverters, providing fully static operation. The edge-triggering operation is achieved by a narrow pulse, produced by the clock signal and its inverted delayed version. The proposed flip-flop exhibits significant power savings of up to 25%, when compared with other static differential flip-flop circuits, maintaining its speed advantage for different power supply voltages and data activity rates. It also requires only 12 transistors resulting in a reduced transistor count. Moreover, unlike the existing differential circuits, it has the ability to operate under a reduced swing clock signal, without static power dissipation.

Introduction: The flip-flop is one of the most crucial elements in modern synchronous VLSI design, as it is the basic storage element in every pipeline stage, seriously affecting the overall system performance. Flip-flops can be categorised into two types: differential and non-differential. Although non-differential flip-flops exhibit low-power and high-speed characteristics, differential structures can play the role of amplifiers when the logic in the pipeline operates with reduced voltage swing signals. Therefore, even if differential flip-flops are not low power circuits, they may be used to reduce the overall power dissipation in pipeline structures.

Circuit description: operation: Fig. 1*a* illustrates the proposed edge-triggered flip-flop circuit. It consists of a pair of cross-coupled inverters (transistors M1-M4), providing fully static operation. The number of transistors can be further reduced by eliminating transistors M3 and M4, resulting in a semi-static design. The data signal and its complementary (D and Db) control transistors M5 and M6, respectively. To increase the driving capability of the flip-flop circuit, an inverting stage is inserted in each output of the cross-coupled pair. The cascaded transistors M7 and M8 enable the flip-flop to be active only during the rising edge of the clock (edge-triggered operation). Transistor M7 is driven by the clock signal (CLK), while transistor M8 is controlled by a delayed version of the inverted clock (CLK1). Consequently, there exists a conductive path to ground only during the time period where both signals CLK and CLK1 are high (from t_1 to t_2 as illustrated in Fig. 1*b*). During this short time period, immediately after the rising edge of the clock, the flip-flop can change its state according to the data signal. When either M7 or M8 is off, no conductive path to ground exists and the flip-flop is in its non-transparent state, keeping the last sampled data.

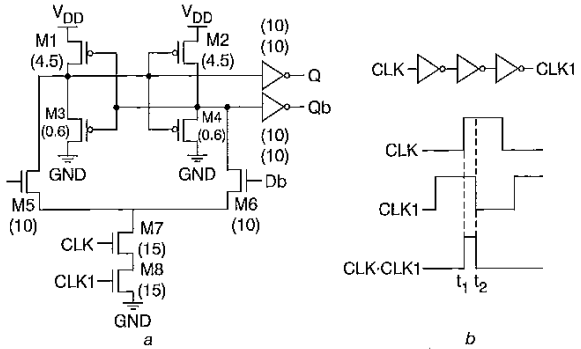

Fig. 1 *Proposed edge-triggered flip-flop and clocking scheme*

a Proposed flip-flop
b Clocking scheme

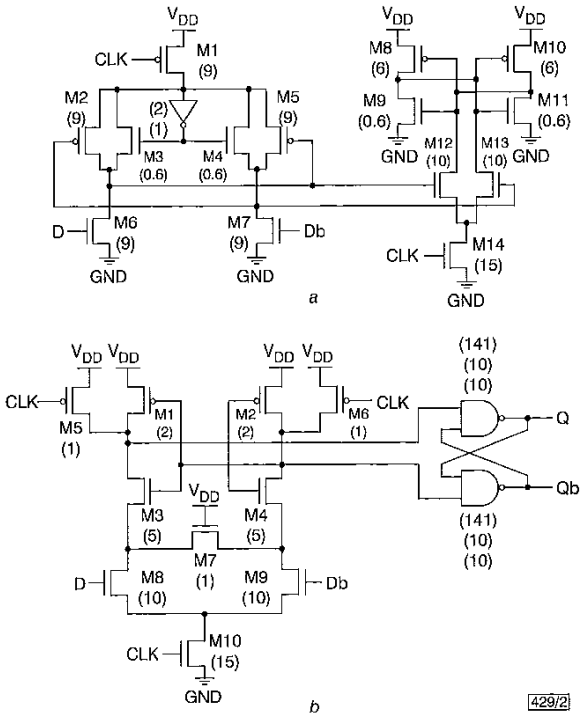

Fig. 2 *Static single-transistor-clocked (SSTC) flip-flop and flip-flop used in StrongArm110*

a SSTC flip-flop
b Flip-flop used in StrongArm110

The CLK1 signal can be generated locally by using a chain of inverters as shown in Fig. 1*b*. The extra area and power introduced by the inverting chain can be considered negligible if CLK1 is shared by other adjacent flip-flop cells. Clock signal racing has also been employed for the generation of a narrow pulse in the design of a CMOS edge-triggered flip-flop [1]. However in [1] three additional clock signals are needed apart from the main clock, while in the proposed flip-flop only one extra clock signal is necessary, reducing in this way the power dissipated by the clock.

A very attractive feature of the proposed flip-flop is that it employs only an NMOS transistor as the clock load. As a result,