Noise Parameter Modeling and SiGe Profile Design Tradeoffs for RF Applications

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(Invited)

Abstract— **This paper presents a unified approach to optimizing SiGe transistors for low noise. An intuitive model relating transistor structural parameters and biases to noise parameters is introduced, and used to identify the noise limiting factors in a given transistor technology. Issues related to the calibration of 2-D device simulation are discussed. SiGe profile design trade-offs for low noise performance are then presented with experimental results.**

I. Introduction

RF applications generally impose more serious device design constraints than digital applications. SiGe HBT technology, because it has higher intrinsic performance than Si BJT technology at similar process complexity, and delivers better cost-performance than GaAs technology, has recently emerged as a contender for the RF market. Existing SiGe profile design points are only optimized for high f_T and f_{max} at high current densities [1]. RF transceiver building blocks such as LNA's and mixers, however, often require very low broad band noise, high RF gain, and excellent RF linearity, thus complicating the device design. This work presents a simulation-noise model approach to optimizing SiGe profiles for low noise applications. An intuitive noise model is introduced and used to identify the dominant noise sources for a given transistor technology. The input of the noise model is the y-parameters, which can be either measured or simulated. We then examine the key issues related to calibrating a 2-D device simulator for accurate y-parameter simulation. SiGe profiles are designed using the ac simulation-noise model approach to explicitly improve noise performance without sacrificing film stability. The trade-offs between supressing high injection barrier effect and improving noise performance at low injection are discussed. Finally, experimental results are presented.

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II. Noise Modeling

Any linear noisy two-port can be represented by its noiseless counterpart, an input current noise source i_n, and an input voltage noise source v_n. The minimum noise figure NF_{min}, the optimum admittance, Y_{opt}, and the noise resistance R_n can all be expressed explicitly as a function of $< v_n^2 >$, $< i_n^2 >$, and $< v_n i_n^* >$. For a bipolar transistor, these quantities can be derived using the equivalent circuit in Fig. 1 as [4] [5]:

$$< i_n^2 >= 2qI_B + \frac{2qI_C}{|h_{21}|^2} \quad (1)$$

$$< v_n^2 >= 4kTr_B + \frac{2qI_C}{|y_{21}|^2} \quad (2)$$

$$< v_n i_n^* >= \frac{2qI_c y_{11}^*}{|y_{21}|^2} \quad (3)$$

where y_{11} is the input admittance, y_{21} is the transfer admittance, and $h_{21} = y_{21}/y_{11}$ is the ac current gain. Noise figure can be reduced by decreasing $< v_n^2 >$ and $< i_n^2 >$. Physically, $< i_n^2 >$ is contributed by $2qI_B$ and $2qI_C$, and v_n^2 is contributed by $4kTr_B$ and $2qI_C$. $2qI_C$ contributes to both v_n and i_n, and determines $< v_n i_n^* >$. The equations that link $< v_n^2 >$, $< i_n^2 >$, and $< v_n i_n^* >$ to NF_{min}, Y_{opt}, and R_n can be found in [3] and [4].

Fig. 2 shows $< i_n^2 >$ versus I_C at 2GHz for a $0.5 \times 20 \times 2\mu m^2$ SiGe HBT. Details of the fabrication process can be found in [1]. The data was calculated from measured y-parameters using (1). $|h_{21}|$ increases when I_C increases because of increasing f_T, therefore, the contribution of $2qI_C$ to $< i_n^2 >$ decreases rapidly with increasing I_C, and for most of the current range, $2qI_B$ dominates $< i_n^2 >$. For an ideal transistor with infinite current gain and infinite f_T (h_{21}), $< i_n^2 >$ would be zero.

Fig. 3 shows $< v_n^2 >$ versus I_C at 2GHz calculated from measured y-parameters using (2). Before the high injection f_T roll-off, $|y_{21}|$ is independent of frequency at frequencies

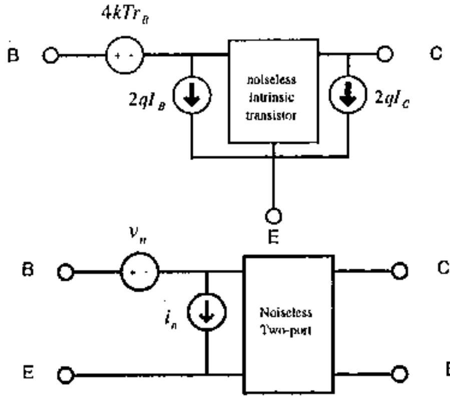


Fig. 1. Schematic of the noise sources in a transistor and its chain noisy two-port representation.

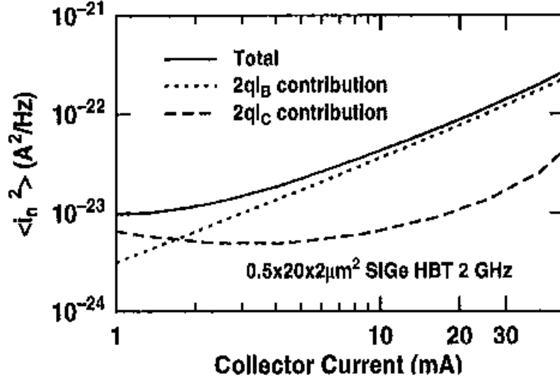


Fig. 2. Spectral density of the equivalent input current noise as a function of collector current at 2GHz.

of interest, and can be approximated by qI_C/kT. Therefore, the contribution of $2qI_C$ to $< v_n^2 >$ is solely determined by $1/I_C$ prior to the f_T roll-off I_C, and thus independent of any other transistor parameters, as can be seen from (2). This has significant implications because it sets the fundamental limit of the noise performance of a bipolar transistor at a given I_C for zero base resistance, infinite DC current gain, and infinite f_T (h_{21}). This fundamental limit only depends on the bias current and temperature, and independent of technology (III-V or SiGe). For the SiGe HBT results shown in Fig. 3, the contribution of r_B dominates over most of the bias current range, indicating that significant improvement of noise performance can be expected by increasing the base doping.

For a given technology generation (transistor geometries and constant doping), the base resistance R_B and y_{21} at a given I_C are fixed, thus fixing $< v_n^2 >$. $< i_n^2 >$, however, can be reduced by increasing β (to reduce I_B) and increasing f_T (to increase h_{21}). In particular, at relatively high current where gain is large, $2qI_B$ dominates $< i_n^2 >$, and noise improvement can only be achieved through the increase of β. Consequently NF_{min} can be reduced.

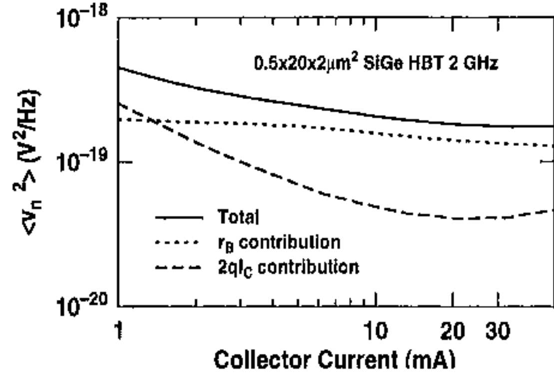


Fig. 3. Spectral density of the equivalent input voltage noise as a function of collector current at 2GHz.

Next, we use 2-D device simulation to calculate the y-parameters for various SiGe profiles at constant film stability (integrated Ge dose). The noise parameters were then calculated from the simulated y-parameters. To produce sensible results, the 2-D device structure for the standard control SiGe HBT was first calibrated to measured y-parameters. Issues related to the calibration are discussed in the following section.

III. Calibration of 2-D Device Simulation

MEDICI [2] was used to simulate DC and y-parameters from measured SIMS profiles. The first step is to determine the most plausible profiles based on SIMS data. The base pinch sheet resistance can be used to calibrate the base doping profile, and determine the EB and CB junction locations. The base doping and Ge profiles also set the $I_C - V_{BE}$ characteristics. The measurement should be made on very long emitter devices to avoid 3-D effects. The carrier lifetime in the emitter can be adjusted to reproduce the $I_B - V_{BE}$ characteristics. Bandgap narrowing (BGN) parameters can be adjusted to shift the simulated $I_C, I_B - V_{BE}$ curves towards measured curves. For accurate y-parameters simulation, particularly at the low currents of interest here, all of the lateral structure must be included in the simulation. For state-of-the-art bipolar transistors with very narrow emitters, the shallow-trench isolation and extrinsic CB capacitances can often be comparable to the intrinsic CB capacitance, and therfore non-negligible. The base resistance, EB and CB capacitance were extracted from measured and simulated y-parameters using a set of analytical equations, and then plotted as a function of $log(I_C)$. The extraction used the y-parameters at only the frequency of interest (e.g. 2GHz), thus speeding up the calibration. By comparing the simulated and measured r_B, C_{BE}, and C_{BC}, one can identify the dominant factors of simulation-measurement discrepancy, and adjust the lateral doping extension accordingly. The diffusion capacitance component of C_{BE} is proportional to I_C at relatively lower currents, and can be distinguished from the depletion capacitance component. By simulating and measuring devices with different emitter widths, the contribution of the extrinsic and intrinsic base resistances

can be distinguished. Another important aspect of calibration is to select a proper set of physical models and coefficients. For instance, incomplete ionization, though recommended explicitly by users' manuals, often leads to an overestimation of the base resistance. At concentrations higher than $10^{18}/cm^3$, the semiconductor-metal transition occurs, and the dopants are completely ionized. This, however, is not, to the authors' knowledge, modeled in today's commercial device simulators. Therefore, we intentionally used complete ionization in order to accurately simulate the base resistance since it is of great importance for noise modeling. The mobility model was critical in determing the f_T roll-off J_C, and in our experience the Philips unified mobility model (PHUMOB) was found to be the most accurate.

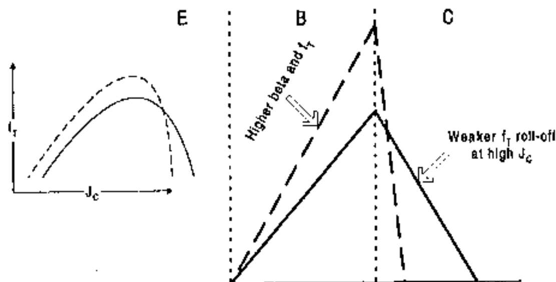


Fig. 4. Schematic of the SiGe profile design tradeoffs between improving f_T and β at low injection and supressing the f_T roll-off at high injection.

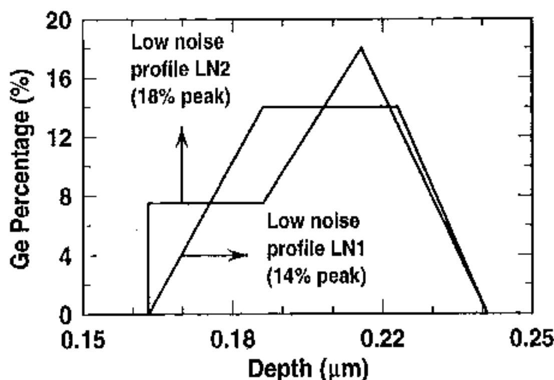


Fig. 5. Schematic of the two low noise profiles designed that are both unconditionally stable.

IV. SiGe Profile Design

For constant film stability, at a given geometry and doping, a higher f_T and higher β can only be realized in practice by pushing the edge of the Ge retrograde in the collector significantly closer to the EB junction (surface). The additional Ge can then be used to reduce the effective Gummel number in the neutral base (for higher β), and increase the Ge grading (for higher f_T) [7]. We are thus forced to trade high-J_C performance for improved NF_{min}. Fig. 4 illustrates the SiGe profile design tradeoffs. The dash profile has more Ge content and a larger Ge gradient in the base, and therefore higher β and f_T, and lower noise. The solid profile has deeper Ge retrograding into the collector, and therefore a better (weaker) f_T roll-off at high injection. Obviously there are numerous possiblities of SiGe profiles to choose from for a given Ge integral. Extensive numerical simulations were performed to determine the optimum profiles for lowest noise. Fig. 5 shows two such low-noise Ge profiles (LN1 and LN2) which maintain the stability of the SiGe control profile but have significantly lower NF_{min} in simulation (by 0.2dB). All of the SiGe profiles are unconditionally stable to defect generation, as shown in the stability plot in Fig. 6. Compared to the SiGe control profile, the two low noise profiles have a smaller effective thickness, and a higher strain, because more Ge were pushed into the base. The two low noise profiles have f_{max} values comparable to the SiGe control in simulation. The excellent linearity of the Si BJT and SiGe control devices are expected to be retained in the two low noise profiles, because the linearity is primarily determined by the EB and CB depletion capacitances, and insensitive to the diffusion capacitance (base transit time) in this technology [8].

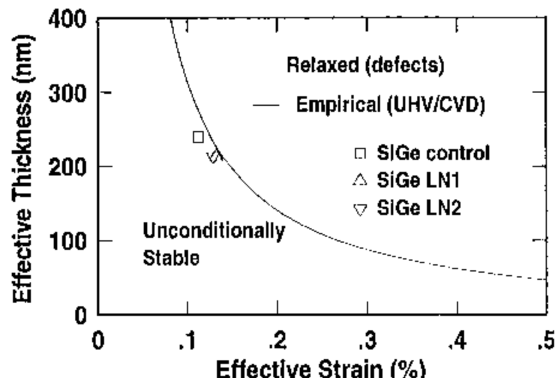


Fig. 6. Stability of the SiGe control design point and the two low noise profiles. All of these profiles are unconditionally stable.

V. Experimental Results

For unambiguous comparisons all four profiles were fabricated in the same wafer lot in a state-of-the-art $0.50\mu m$ SiGe HBT technology [1] using UHV/CVD growth and identical processing conditions. DC charactersitics were measured using an HP4155, and S-parameters were measured using a HP8510C network analyer from 2 - 40GHz, from which f_T and f_{max} were extracted. The noise parameters were measured from 2 - 18GHz using an NP-5 on-wafer measurement system from ATN Microwave Inc., and two-tone load-pull measurements were made at 1.9GHz with 1MHz tone spacing.

TABLE I
SUMMARY OF DEVICE ELECTRICAL CHARACTERISTICS

Performance	Si BJT	SiGe control	SiGe LN1	SiGe LN2
β at V_{BE}=0.7V	67	114	350	261
V_A(V)	19	60	58	113
$BV_{CEO}(V)$	3.5	3.2	2.7	2.7
R_{Bi} ($k\Omega/\Box$)	12.8	9.8	10.3	10.7
peak f_T (GHz)	38	52	52	57
peak f_{max} (GHz)	57	64	62	67

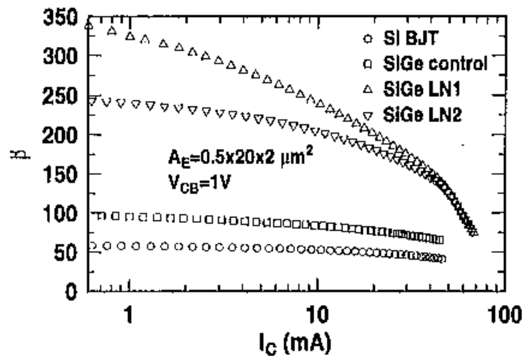


Fig. 7. Measured dc current gain versus collector current of the fabricated Si BJT, SiGe control, and the SiGe low noise profiles.

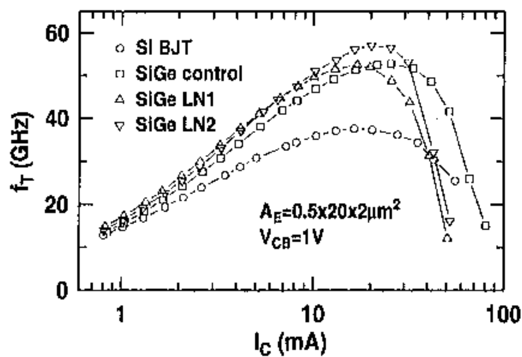


Fig. 8. Measured f_T versus collector current of the fabricated Si BJT, SiGe control, and the SiGe low noise profiles.

Table I summarizes the measured transistor parameters of the four fabricated profiles. The penalty in BV_{CEO} over the SiGe control for LN1 and LN2 is due to the higher β, and should not impact LNA designs, which see finite source impedance (i.e., not an 'open'). The measured $\beta_{DC} - I_C$ and $f_T - I_C$ curves of a $20\mu m^2$ ($0.5 \times 20 \times 2\mu m^2$ stripe) unit cell device are shown in Figs. 7 and 8 respectively, and bear-out exactly the expected high injection design trade-off. The two low noise profiles, LN1 and LN2, have a higher β and f_T at low J_C because of more total Ge content and higher Ge gradient in the neutral base. The SiGe control and Si BJT devices have a weaker (better) f_T roll-off at high J_C, because of the deeper Ge grading into the collector-base junction, as designed. This design tradeoff translates into a significant improvement of the NF_{min} across the range of J_C of interest to LNA and mixer circuits over the Si BJT and SiGe control profiles, as shown by the measured NF_{min} data in Fig. 9 . The LN1 profile achieves an impressive NF_{min} of 0.2dB at 2mA, 0.2dB lower than the SiGe control profile. The measured delta's between profiles are consistent with our simulations. The associated gain at noise matching is still above 13dB at NF_{min} for all of the profiles, as can be seen from Fig. 10. The two low noise profiles have f_{max} values comparable to the SiGe control (Fig. 11), indicating that the high power gain in the control design point is retained.

Two-tone load-pull measurements were performed at 1.9GHz with 1.0MHz tone spacing on the $20\mu m^2$ ($0.5 \times 20 \times 2$ stripe) unit cell device to determine the linearity. The input 3rd order intermodulation intercept point (IIP3) for a two-tone input is used as a figure-of-merit, and was extracted in the low input power region where the 3rd order intermodulation slope is 3:1. The measured IIP3 is affected by the source and load termination, and thus load-pull data sheds light on the variation of linearity with impedance for each profile. Figs. 12-13 and 14-15 show the measured IIP3 and power gain contours on the load impedance Smith chart for the SiGe control device, and the low noise profile LN1, respectively. The maximum IIP3 achieved is 3dBm (SiGe control) and 3dBm (LN1), with the maximum gain of 17dB (SiGe control) and 20dB (LN1), at 1.9GHz for I_C=3mA and V_{CB}=3V. An excellent linearity efficiency (defined as OIP3/P_{DC} to account for the differing load states at maximum gain and maximum IIP3) of 7 and 10 is achieved for the SiGe control and the low noise SiGe profile LN1, respectively, and is comparable to GaAs HEMT (10) and GaAs HBT technology (11) [9]. Preliminary measurements on RF sub-harmonic mixers fabricated with the identical low noise profiles (LN1 and LN2) also show improved noise and linearity over the SiGe control profile, indicating that these device improvements translate to the circuit level [10].

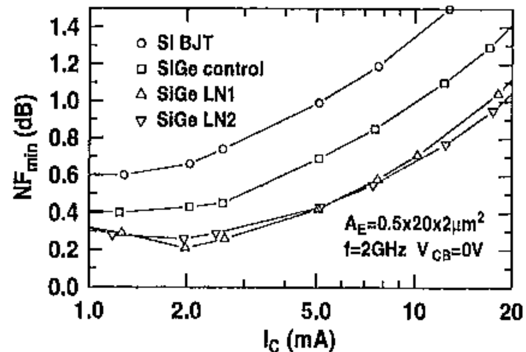


Fig. 9. Measured minimum noise figure (NF_{min}) versus collector current at 2GHz for the fabricated Si BJT, SiGe control, and the SiGe low noise profiles.

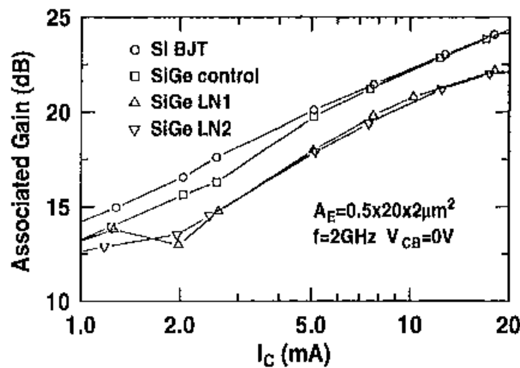


Fig. 10. Measured associated gain versus collector current at 2GHz for the fabricated Si BJT, SiGe control, and the SiGe low noise profiles.

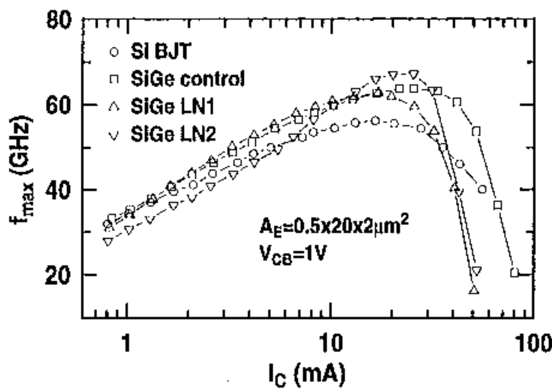
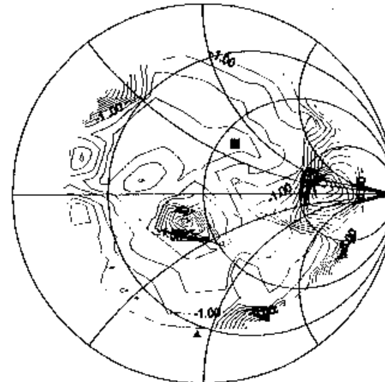


Fig. 11. Measured f_{max} versus collector current at 2GHz for the fabricated Si BJT, SiGe control, and the SiGe low noise profiles.

VI. Conclusions

A unified approach to the modeling of transistor noise was presented, and used to identify the limiting factors of noise performance for a given transistor technology. Key issues related to a successful calibration of 2-D device simulation to measured y-parameters were also discussed. A higher DC current gain and a higher f_T at relatively lower current are shown to be critically important for reducing NF_{min} for a given transistor geometry and doping. By applying careful SiGe profile optimization, significant improvement in RF performance can be achieved. Using the noise model-simulation approach, new SiGe profiles were designed explicitly for improving minimum noise figure (NF_{min}) without sacrificing gain, linearity, frequency response, or the stability of the SiGe strained layer. A measured NF_{min} of 0.2dB at 2.0GHz with an associated gain (G_{assoc}) of 13dB at noise matching, and a linearity efficiency ($OIP3/P_{DC}$) of 10 were obtained for the best low-noise profile, all of which represent substantial improvements in RF performance over the Si BJT and control SiGe HBT design point, and were accomplished without sacrificing SiGe film stability.

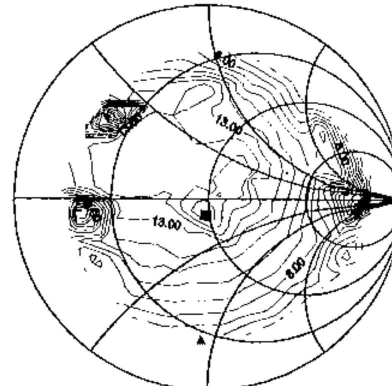
SiGe Control Third-Order Intermodulation Intercept Point
0.5x20x2, F=1.9 GHz, Ice=3.0mA, Vce=3.0V



IIP3 Max=2.81 dBm at 58.9+j34.9 load,
Source Impedance=13.9-45.8j Pin=-24.0dBm

Fig. 12. Measured IIP3 contour on the load impedance Smith chart for the SiGe control device.

SiGe Control Load-Pull GAIN on 0.5x20x2 NPN HBT
Ice=3.0mA, Vce=3.0V, F=1.9 GHz, Pin=-24.0dBm



GAIN Max=17.31 dB at 48.1-j8.0 load
Sourc Impedance=13.9-j45.8

Fig. 13. Measured power gain contour on the load impedance Smith chart for the SiGe control device.

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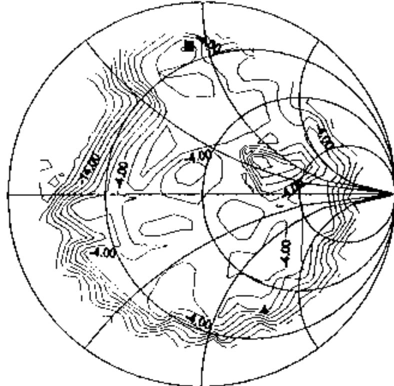
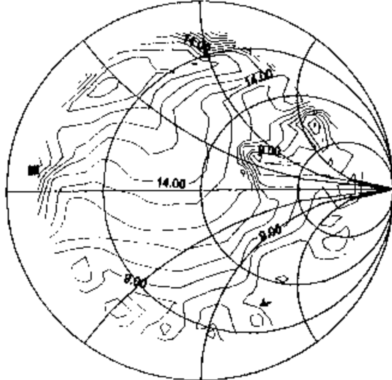
SiGe Low Noise Profile LN1 Third-Order Intermodulation
Intercept Point, Ice=3.0mA, Vce=3.0V, F=1.9 GHz



IIP3 Max=2.89 dBm at 11.6+j44.5 load,
Source Impedance=33.7-73.5j Pin=-23.5dBm

Fig. 14. Measured IIP3 contour on the load impedance Smith chart for the low noise profile device LN1.

SiGe Low Noise Profile LN1 Load-pull GAIN
Ice=3.0mA, Vce=3.0V, F=1.9 GHz, 0.5x20x2



GAIN Max=19.82 dB at 3.6+j3.3 load
Sourc Impedance=33.7-73.5j,Pin=-23.5dBm

Fig. 15. Measured power gain contour on the load impedance Smith chart for the low noise profile device LN1.

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