Silicon Bipolar Transistor Design and Modeling for Microwave Integrated Circuit Applications (Invited Paper)

Lawrence E. Larson
Head - Telecommunications Technology Department
Hughes Research Laboratories
3011 Malibu Cyn. Rd.
Malibu, CA 90265

ABSTRACT: This paper summarizes the recent progress in the fabrication, design, and modeling of silicon and Si/SiGe bipolar transistors for high-frequency microwave integrated circuit applications. These devices are now capable of performance levels that were only achievable with GaAs technology just a few years ago. The specific device requirements for low-noise, signal, and power amplifiers are discussed, as well as required improvements in device modeling for these applications.

INTRODUCTION: Thanks to improvements in processing and materials growth technology, silicon bipolar transistor integrated circuits are now capable of performance that would have recently been possible only with GaAs technology. An excellent example of this is the Ku-Band DBS downconverter IC, announced by Hewlett-Packard at the 1995 BCTM [1]. This bipolar silicon integrated circuit has an integrated mixer/oscillator operating at 12 GHz, followed by several stages of lower frequency microwave amplification and switching. Its performance is comparable in many ways to well-known GaAs designs operating in the same frequency band [2]. Other microwave integrated circuits, operating at even higher frequencies, have been demonstrated recently in silicon bipolar technology, including broadband gain stages [3], oscillators [4], and mixers [5].

This paper will summarize the device design and modeling considerations required to achieve the best microwave performance from monolithic silicon bipolar transistors in the areas of low-noise, high-linearity, and high-power amplification, as well as mixer and oscillator applications. These considerations are often different from those required to optimize the device for high-speed digital or precision analog applications - the traditional areas of application for silicon bipolar technology.

HIGH-FREQUENCY SCALING OF SILICON BIPOLAR TRANSISTORS: The improvement in speed of silicon bipolar transistors has been dramatic in recent years. Several technological innovations have accounted for the performance improvement: self-aligned polysilicon emitter structures, deep and shallow trench isolation, epitaxial base deposition, and SiGe alloys in the base [6]. Several groups have reported transistor $f_T's$ - the frequency of unity short-circuit current gain - in excess of 100 GHz [7]. Similarly, the f_{MAX} of the transistor - the frequency of maximum power gain - has also been demonstrated in excess of 100 GHz [8]. Although no device yet has demonstrated simultaneous f_T and f_{MAX} in excess of 100 GHz, it is anticipated that this will be achievable shortly. Until recently, these performance levels were only achievable with the most advanced GaAs technology.

From the perspective of microwave circuit design, both frequency figures of merit - f_T and f_{MAX} - are important for the optimization of circuit performance. The f_T of a bipolar device is related to its transit times by the simplified expression:

$$\frac{1}{2\pi f_T} = \tau_{ec} = \tau_E + \tau_B + \tau_{CSL} + \tau_C \qquad (1)$$

$$= \frac{C_{TE} + C_{TC}}{g_m} + \frac{w_B{}^2}{KD_B} + r_c(C_{TS} + C_{TC}) + \frac{x_C}{v_{\lim}}$$

where $\tau_E, \tau_B, \tau_{CSL}$, and τ_C are the emitter, base, collector space charge layer, and collector transit/charging times respectively, and where C_{TE} is the emitter-base junction capacitance, C_{TC} is the base-collector junction capacitance, g_m is the transconductance, w_B is the effective base-width, D_B diffusion constant in the base, K is a grading coefficient (typically between 1 and 5), r_c is the collector resistance, C_{TS} is the substrate capacitance, x_c is the collector depletion width, and $v_{\lim}$ is the saturated carrier velocity.

Figure 1 shows a simplified schematic cross-section of a bipolar transistor, highlighting the various components of its transit times, as well as the factors limiting their reduction.

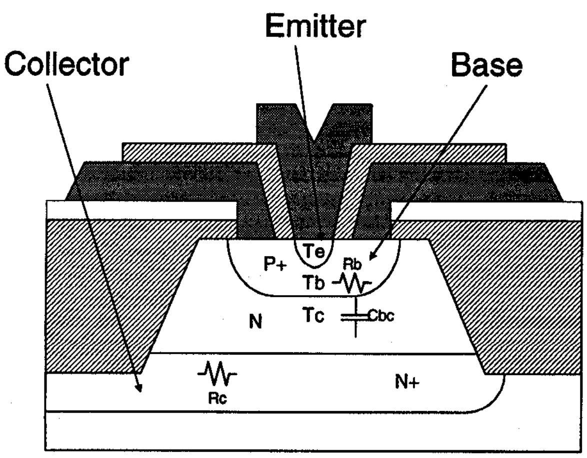

Figure 1: Simplified Cross Section of Bipolar Transistor.

The key issues for device scaling at these frequencies are minimization of base width without degrading base resistance, optimization of the collector and emitter doping profiles for minimum resistance and capacitance, and scaling emitter width for reduce power consumption and improved speed.

The unity power gain frequency f_{MAX} is related to f_T by the simplified expression:

$$f_{MAX} = \sqrt{\frac{f_T}{8\pi r_B c_{BC}}} \qquad (2)$$

where r_B is the base resistance and c_{BC} is the base-collector capacitance.

If the transistor f_T is raised substantially above f_{MAX}, then the performance of the device is limited by parasitic elements ($r_B\, c_{BC}$), and its resulting microwave gain is lowered. Conversely, if the f_{MAX} of the device is substantially higher than the f_T, then the impedance required to optimally match the device for power gain can become unrealistically high or low (very far from 50Ω), and the *achievable* gain of the circuit is reduced. The optimum design typically has f_T and f_{MAX} values within roughly a factor of two of each other over a broad range of collector-base bias conditions.

These two figures of merit - f_T and f_{MAX} - are useful for device comparisons under impedance matched or extreme impedance conditions. However, in many microwave integrated circuit applications, impedance matching results in excessive power dissipation. Other device parasitic elements become significant under these conditions. One of which is the collector-substrate capacitance (c_{CS}), which can limit power gain at high frequencies in non-impedance matched situations.

This capacitance has diminished considerably in recent years due to improvements in isolation techniques and the use of lightly-doped epi-layers. It can be as low as several fF in the most advanced trench isolated structures. In addition, the associated rise in the series substrate resistance has further diminished the relative importance of this capacitance. Early voltage considerations are typically not significant in these structures, especially in the case of Si/SiGe HBTs, where the base doping is extremely high.

The improvements in transistor f_T and f_{MAX} have not occurred without some significant compromises, primarily involving reductions in transistor BV_{CEO}. This reduction is related to the well-known Johnson limit on transistor performance, where the product of the breakdown voltage and f_T is roughly constant (approximately 300GHz•V in the case of silicon). This limit is *material* related, and consequently is not amenable to improvements in device design or process technology. Figure 2 plots the reported f_T and BV_{CEO} for a variety of modern bipolar transistors, all of which perform quite closely to the Johnson limit [9].

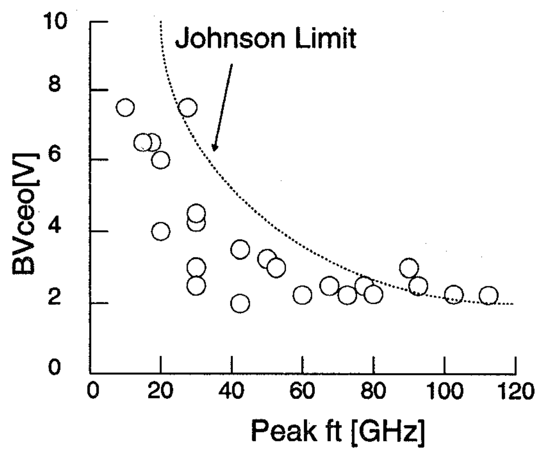

Figure 2: Measured f_T and BV_{CEO} for a variety of advanced silicon bipolar structures [9].

The BV_{CEO} of the device is determined in part by the collector-base breakdown voltage - BV_{CBO} and the low-frequency current gain (α_0) of the device through

$$BV_{CEO} = BV_{CBO}(1-\alpha_o)^{1/n} \tag{3}$$

where α_o is the common-base current gain and n is a fitting factor for the avalanche multiplication factor of the collector-base junction breakdown characteristics

$$M = \frac{1}{1-\left(V_{CB}/BV_{CBO}\right)^n} \tag{4}$$

This tradeoff between speed and breakdown voltage represents a fundamental limit on microwave circuit performance. Note that a high dc value of β is not crucial for high-performance microwave circuit applications, since the current gain is largely determined by f_T at high frequencies. As a result, the microwave performance can be somewhat improved by increasing the base doping, at the expense of f_T and β, with a resulting increase in BV_{CEO} and f_{MAX}.

LOW-NOISE DEVICE DESIGN: Microwave low-noise amplifiers are typically realized with GaAs MESFET or PHEMT structures, due to their superior electron transport properties and low gate resistance. However, Si/SiGe heterojunction bipolar transistors have recently demonstrated outstanding noise figure results, e.g. 0.9 dB at 10 GHz and 0.2 dB at 2 GHz [10]. The origins of this improvement can be seen from the simplified expression for the minimum noise figure of a bipolar transistor [11]

$$F_{\min} \approx 1+u+(2u+u^2)^{1/2} \tag{5}$$

where

$$u \equiv \left[1-\alpha_0+\left(f/f_T\right)^2\right]\frac{r_b I_e}{V_T}$$

where I_e is the dc emitter current and V_T is 25.8 mV at room temperature.

This expression demonstrates the importance of minimizing r_B and maximizing f_T at very low emitter currents in order to obtain the lowest possible noise figure. In this respect, the requirements for low-noise figure are similar to those for a high transistor f_{MAX}, with the exception that the device is required to operate at a low current - typically 0.5 to 3 mA - to obtain the best noise figure.

Modern silicon and Si/SiGe bipolar transistors are ideal for the realization of these low-noise devices, because of their high base doping and f_T. It is expected that they will be able to achieve performance close to that of commercially available GaAs MESFETs in the near future. Figure 3 plots a comparison of minimum noise figures for a variety of competing low-noise transistor technologies [12].

Another important source of noise in microwave transistors is 1/f noise, since this can have a significant effect on close in phase-noise of VCOs at microwave frequencies. Bipolar transistors have historically demonstrated excellent 1/f noise characteristics compared to FET-based technologies, and modern microwave bipolar transistors continue to demonstrate outstanding performance. 1/f noise corner frequencies of approximately 400 Hz were recently reported for both Si and Si/SiGe transistors [13]. The low-frequency input referred base noise current is shown to be inversely proportional to emitter area and quadratically dependent on dc base current. This implies that the noise sources are almost uniformly distributed throughout the base region.

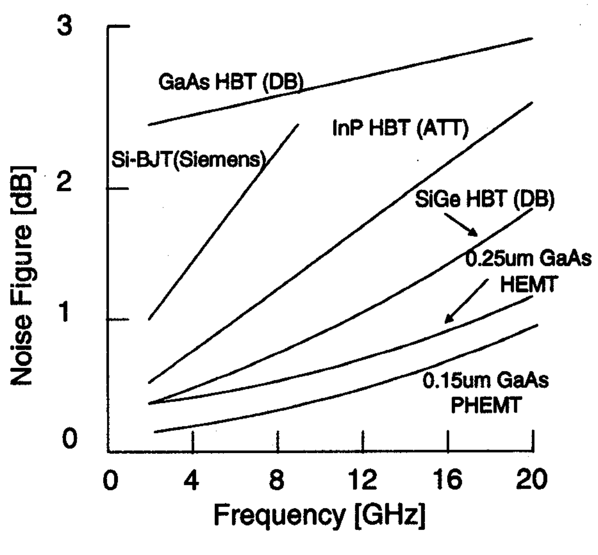

Figure 3: Comparison of minimum noise figures of low-noise microwave transistor technologies [12].

DEVICE DESIGN FOR SIGNAL APPLICATIONS: The low-frequency distortion characteristics of silicon bipolar transistors re well-known and have been thoroughly documented [14]. The highly non-linear relationship between the collector current and base-emitter voltage has historically resulted in relatively high levels of third-order intermodulation distortion, which is especially detrimental to the performance of high-frequency communications circuits. A transistor figure-of-merit for linearity is the ratio of dc power dissipation (Pdc) to input third order intercept point (IP3), although this ratio can be somewhat misleading because the measurement of IP3 is itself dependent on both input signal level and frequency.

Recently, it has been determined that the microwave linearity of GaAs HBT amplifiers is remarkably good, with linearity figures of merit (IP3/Pdc) in excess of 10, compared with three or less for the theoretical low-frequency limit determined by the classical I-V relationship of a BJT. The difference between the linearities of low-frequency Si BJTs and higher frequency GaAs HBTs has been attributed to several factors, including cancellation of the reactive and resistive portions of the non-linear base-emitter current at high frequencies [15], relatively constant base-collector capacitance, and negative feedback effects of Re and Rb [16]. In practical situations, all of these considerations aid device performance.

In practice, it is not clear whether or not these advantages will also accrue to high-speed *silicon* bipolar transistors operated at microwave frequencies. This is clearly a potential area for further study.

DEVICE DESIGN FOR POWER AMPLIFIER APPLICATIONS: Silicon bipolar transistors have historically dominated the high-power transistor market at the lower microwave frequencies (300-1000MHz). The devices typically operate under pulsed conditions to avoid heating effects, and they are capable of producing in excess of 100W of output power.

More recently, a variety of groups have begun to explore the use of advanced silicon or Si/SiGe bipolar transistors for higher frequency (1-10GHz) amplifier applications with more modest CW output power considerations (<1W). For example, these amplifiers can be employed as the output driver stages of a cellular or PACS telephone, or the transmitter for a wireless LAN. The key figure of merit for these amplifiers are output power, power-added efficiency (to maximize battery life), and low voltage (3.3V) operation.

The power-added efficiency of the transistor amplifier can be approximated by

$$PAE = \frac{P_{out}(rf) - P_{in}(rf)}{P_{in}(dc)} = \frac{\eta}{1 - 1/G} \qquad (6)$$

where η is the collector efficiency of the transistor, which varies with the class of operation, and G is the large-signal gain of the transistor.

In a practical situation, the maximum applied collector voltage should be kept to less than the maximum collector voltage (BV_{CBO} in common-base operation and BV_{CEO} in common-emitter operation). With a reactively tuned load, the collector can swing to almost twice the supply voltage, so the maximum output power is given by

$$P_{max} = \frac{V_{max}^{2}}{8R_L} \qquad (7)$$

where R_L is the load resistance presented to the device and V_{max} is the maximum voltage across the device.

Due to the tradeoff between device f_T and breakdown voltage (Johnson's limit), the maximum output power of high-performance silicon or Si/SiGe bipolar transistors is limited at frequencies above 10 GHz, although this limit can be partially circumvented by use of common-base operation. Recent results have demonstrated 100 mW at 12 GHz [4]. However, at lower frequencies, the power-added efficiency and gain of these devices is outstanding. They function especially well at the lower supply voltages favored by hand-held systems designers. A recent SiGe HBT amplifier demonstrated 22 dB gain and 70% power-added efficiency with 20 mW of output power at 900 MHz [17].

Bipolar transistors have an *intrinsic* advantage over field-effect transistors in collector(drain) efficiency (η) due to the exponential nature of the collector current vs. base-emitter voltage characteristic when operated in Class-B mode. The peak efficiency for an FET is 78.5% for a transistor with constant transconductance, rising to 85% for a linearly increasing transconductance, whereas the peak efficiency for an ideal bipolar transistor is 90.4% [18]. This advantage translates into significant potential advantage for the BJT circuit when operated in Class-B mode.

TRANSISTOR EQUIVALENT CIRCUIT MODELING FOR MICROWAVE APPLICATIONS: Although bipolar transistor technology has reached an unprecedented level of maturity and sophistication, many aspects of high-frequency circuit modeling of these devices continue to produce significant limitations, especially for devices operating at high frequencies. I will attempt here to highlight some of the limitations of commercially available circuit simulation models for bipolar transistors.

The measured f_T of silicon bipolar transistors tends to drop dramatically when emitter current densities exceed a certain critical value. This effect is modeled in most advanced silicon bipolar equivalent circuit models, but the measured effect is typically much larger than the models are able to predict. This is related to the dramatic increase in base transit time due to base "push-out" effects when the concentration of injected electrons exceeds the collector doping (Kirk effect).

In SiGe HBTs, the onset of the Kirk effect is altered by the collector-base heterojunction, which creates a barrier that opposes the flow of electrons into the collector. When the critical current density for the onset of the Kirk effect is exceeded, there is a very rapid drop-off in f_T, which is not modeled well in commercial circuit simulators. Circuits designs operating in this region will typically simulate very optimistic performance.

Another important area for improvements in modeling accuracy is the "quasi-saturation" region of device operation, which typically occurs at low collector voltages and high collector current densities, where the voltage drop across the lightly-doped epi-layer of the collector can lead to forward biasing of the collector-base junction. This effect can lead to a drop in f_T and β, as well as changes in the distortion characteristics of the device [19]. It is especially important to model correctly in mobile telecommunications circuits applications, where the devices typically operate at low voltages and high current densities. A recent paper demonstrated significant improvements in the modeling of transistor distortion using improved models for quasi-saturation behavior [20].

Finally, the accurate modeling of breakdown phenomena - collector-base as well as base-emitter- is still not handled well in most circuit simulators, due to the well-known problems it can cause with convergence (the multiplication factor M in Eq.(4) exhibits a singularity at $V_{CB} = BV_{CBO}$). Accurate modeling of breakdown is especially important for high-power amplifier applications, where maximum collector-voltage swing is desired in order to realize high power-added efficiency. Various attempts to model BV_{CEO} and BV_{CBO} have been made in the past, but they have not found their way into commercial circuit simulators [21]. Recently, a non-singular Newton backward difference expansion of Eq. (4) was suggested, as an alternative expression for carrier multiplication in the collector-base region, which should exhibit significantly improved convergence characteristics [22].

CONCLUSIONS : Silicon bipolar technology has demonstrated remarkable improvements in performance in the last several years, and is now able to address applications in the upper reaches of the microwave spectrum. This paper has summarized the key device design issues required to meet these challenges. However, considerable work remains to be done in the areas of transistor and passive device equivalent circuit modeling, circuit design and test.

Further improvements in device technology are expected to allow silicon BJT technology to address millimeterwave applications in the near future. This will require even more aggressive scaling of all aspects of device geometry and processing. However, the high losses of microwave and millimeterwave signals on the conducting silicon substrate need to be reduced in order for the circuit performance to reach its optimum level, and this remains an area for additional development.

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