

Noise Modeling and SiGe Profile Design Tradeoffs for RF Applications

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Abstract—This paper investigates SiGe profile design tradeoffs for low-noise RF applications at a given technology generation (i.e., fixed minimum feature size and thermal cycle). An intuitive model relating structural parameters and biases to noise parameters is used to identify the noise limiting factors in a given technology. The noise performance can be improved by pushing more Ge into the base and creating a larger Ge gradient in the base. To maintain the SiGe film stability, the retrograding of the Ge into the collector has to be reduced, leading to a stronger $f_T - I_C$ roll-off at high injection. Two low-noise profiles were designed and fabricated explicitly for improving minimum noise figure (NF_{min}) without sacrificing gain, linearity, frequency response, or the stability of the SiGe strained layer. A 0.2 dB NF_{min} was achieved at 2.0 GHz with an associated gain (G_{assoc}) of 13 dB.

Index Terms—Bipolar technology, device simulation, film stability, HBT, linearity, modeling, noise, RF circuits, SiGe.

I. INTRODUCTION

RF APPLICATIONS generally impose more serious device design constraints than digital applications. SiGe HBT technology, because it has higher intrinsic performance than Si BJT technology at similar process complexity and delivers better cost-performance than GaAs technology, has recently emerged as a contender for the RF market. Existing SiGe profile design points are typically optimized for high f_T and f_{max} at high current densities [1]. RF transceiver building blocks such as LNA's and mixers, however, often require very low broad-band noise, high RF gain, and excellent RF linearity, thus complicating the device design. The purpose of this work is to investigate the SiGe profile design tradeoffs associated with RF circuit applications. An intuitive noise model is introduced and used to identify the dominant noise sources for the control profile design point. The input of the noise model is the transistor

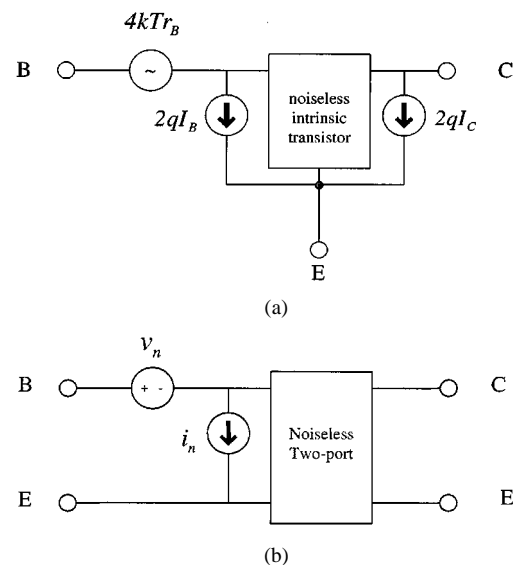


Fig. 1. (a) Schematic of the noise sources in a bipolar transistor and (b) its chain noisy two-port representation.

y -parameters, which can be either simulated or converted from measured s -parameters. We then examine the key issues related to the calibration of dc and ac two-dimensional (2-D) device simulation. SiGe profiles are designed to explicitly improve noise performance without sacrificing film stability and other key performance metrics. The tradeoffs between suppressing high injection barrier effect and improving noise performance are discussed. Finally, experimental results are presented.

II. NOISE MODELING

A. Y -Parameter Based Noise Model

At high frequencies, the major noise sources in a bipolar transistor include the base resistance-induced thermal noise, the base current shot noise, and the collector shot noise, as shown in Fig. 1(a). We have neglected the effects of space-charge generated currents [2] because the devices used in this work have nearly ideal current-voltage (I - V) characteristics. High injection effects [3] were also neglected because low-noise amplifiers typically operate at low current densities (as low as $10 \times$ below the current density where we reach peak f_T).

The traditional approach to noise modeling is to derive the noise figure equation using an equivalent circuit [4], [5]. The resulting equations depend on the specific equivalent circuit used. The equivalent circuit parameters need to be extracted

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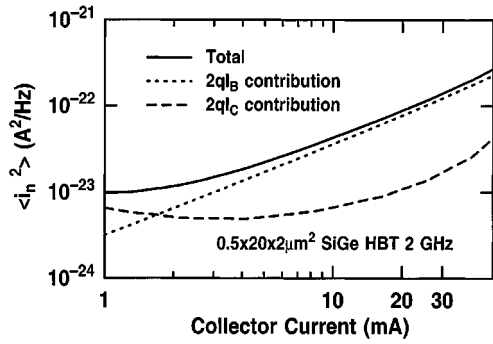


Fig. 2. Spectral density of the equivalent input current noise as a function of collector current at 2 GHz calculated from measured y -parameters using (1).

to obtain noise figure. To overcome these difficulties, we use here a different approach that is based on the circuit theory for linear noisy two-ports [6] and the y -parameters of the transistor [7]–[9]. In this way, the noise figure can be directly obtained from measured or simulated y -parameters.

According to circuit theory [6], any linear noisy two-port can be represented by its noiseless counterpart, an input current noise source i_n , and an input voltage noise source v_n , as shown in Fig. 1(b). The minimum noise figure NF_{min} , the optimum source admittance, Y_{opt} , and the noise resistance R_n can all be expressed explicitly as a function of $\langle v_n^2 \rangle$, $\langle i_n^2 \rangle$, and $\langle v_n i_n^* \rangle$. The general expressions can be found in [6].

For a bipolar transistor, $\langle v_n^2 \rangle$, $\langle i_n^2 \rangle$, and $\langle v_n i_n^* \rangle$ can be derived using the chain representation of the noisy two-port in Fig. 1(b) as [9], [10]

$$\frac{\langle i_n^2 \rangle}{B} = 2qI_B + \frac{2qI_C}{|h_{21}|^2} \quad (1)$$

$$\frac{\langle v_n^2 \rangle}{B} = 4kTr_B + \frac{2qI_C}{|y_{21}|^2} \quad (2)$$

$$\frac{\langle v_n i_n^* \rangle}{B} = \frac{2qI_C y_{11}^*}{|y_{21}|^2} \quad (3)$$

where

- y_{11} input admittance;
- B measurement bandwidth;
- y_{21} transfer admittance;
- h_{21} = ac current gain.
- y_{21}/y_{11}

Physically, $\langle i_n^2 \rangle$ is contributed by the base current shot noise ($2qI_B$) and the collector current shot noise ($2qI_C/|h_{21}|^2$). $\langle v_n^2 \rangle$ is contributed by the base resistance-induced thermal noise ($4kTr_B$) and the collector current shot noise ($2qI_C/|y_{21}|^2$). $2qI_C$ contributes to both v_n and i_n , and thus determines $\langle v_n i_n^* \rangle$. NF_{min} can be decreased by reducing either $\langle v_n^2 \rangle$ or $\langle i_n^2 \rangle$ [6]. For completeness, we have included the cross-correlation $\langle v_n i_n^* \rangle$ in all of the simulations.

B. Input Noise Current Limiting Factors

Fig. 2 shows $\langle i_n^2 \rangle$ versus I_C at 2 GHz for a 0.5 (emitter width) \times 20 (emitter length) \times 2 (stripe number) μm^2 SiGe HBT. Details of the fabrication process can be found in [1]. The data was calculated using (1) from y -parameters that were converted from measured s -parameters. The biasing current dependence

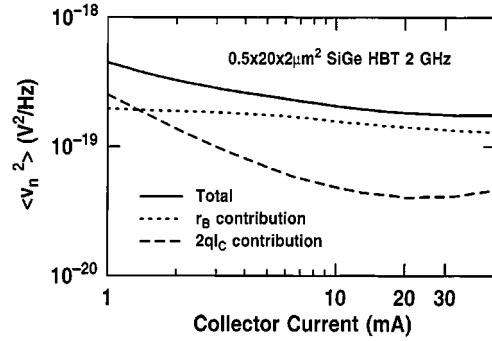


Fig. 3. Spectral density of the equivalent input voltage noise as a function of collector current at 2 GHz calculated from measured y -parameters using (2).

of the contribution of $2qI_C$ to $\langle i_n^2 \rangle$ (i.e., $2qI_C/|h_{21}|^2$) has two factors. First, $|h_{21}|$ at the frequency of interest, which appears in the denominator, increases with increasing I_C because of increasing f_T . Such an increase, however, saturates when f_T becomes much higher than the frequency under question (2 GHz in our case). The typical frequency dependence of $|h_{21}|$ is that $|h_{21}|$ is constant at low frequencies, and decreases at higher frequencies, at a slope of -20 dB/decade. Second, $2qI_C$, which appears in the numerator, increases monotonically with increasing I_C . As a result, the ratio $2qI_C/|h_{21}|^2$ decreases with increasing I_C first when the increase of $|h_{21}|^2$ dominates over the increase of I_C . At higher currents, when the increase of I_C dominates over the increase of $|h_{21}|^2$, the ratio $2qI_C/|h_{21}|^2$ starts to increase again. For most of the current range, $2qI_B$ dominates $\langle i_n^2 \rangle$, implying that a higher β is desired to reduce $\langle i_n^2 \rangle$. For an ideal transistor with infinite current gain and infinite f_T (h_{21}), $\langle i_n^2 \rangle$ would be zero.

C. Input Noise Voltage Limiting Factors

Fig. 3 shows $\langle v_n^2 \rangle$ versus I_C at 2 GHz calculated from y -parameters using (2). Before the high injection f_T roll-off, $|y_{21}|$ can be approximated by qI_C/kT . Therefore, the contribution of $2qI_C$ to $\langle v_n^2 \rangle$ is solely determined by $1/I_C$ prior to the f_T roll-off I_C , and is thus independent of any other transistor parameters, as follows:

$$\langle v_n^2 \rangle |_{\text{contributed by } 2qI_C} = \frac{2qI_C}{|y_{21}|^2} = \frac{2(kT)^2}{qI_C} \quad (4)$$

where $y_{21} = qI_C/kT$ was used. Equation (4) has significant design implications because it sets the fundamental limit of the noise performance of a bipolar transistor at a given I_C for zero base resistance, infinite β , and infinite f_T (h_{21}). This fundamental limit only depends on the bias current and temperature, and is independent of technology (III–V or Si or SiGe). The $1/I_C$ functional form results from the fundamental exponential I_C – V_{BE} characteristics that determines $y_{21} = qI_C/kT$, and is corroborated by the data prior to high injection in Fig. 3. For the devices under discussion [1], the contribution of r_B dominates over most of the bias current range, as shown in Fig. 3. Therefore, significant improvement of noise performance can be expected by increasing the base doping and decreasing the emitter width in future technology generations. Because $\langle v_n^2 \rangle$ is dominated by the thermal noise $4kTr_B$ and $\langle i_n^2 \rangle$ is dominated

by the base current shot noise $2qI_B$, the cross-correlation term $\langle v_n i_n^* \rangle$ can be neglected for these devices.

D. Approaches to Noise Improvement

To improve transistor noise performance, we need to reduce $\langle v_n^2 \rangle$ and $\langle i_n^2 \rangle$. According to the above analysis, r_B needs to be reduced to reduce $\langle v_n^2 \rangle$. It has to be remarked here that we need to normalize r_B with respect to the emitter length when comparing devices with different emitter lengths. For similar reasons, noise figure comparison should be made at the same current density. A simple increase of the emitter length reduces r_B , but does not improve the noise capability, because of the corresponding increase of capacitances by the same factor. However, the emitter length (or the number of unit cells) can be optimized to minimize the losses in the passive matching network by making the optimum source impedance close to the characteristic impedance (for instance, 50Ω) [8].

At a given technology generation, the minimum emitter width is determined by the minimum feature size, and the parasitic CB capacitances. The base sheet resistance is determined by the amount of boron dopants that can be kept in place, which is limited by the thermal cycle. Therefore, r_B and $\langle v_n^2 \rangle$ are fixed. In other words, the input noise voltage can only be reduced by lateral and vertical scaling, the reduction of thermal cycle, or the use of carbon doping [11] in a more advanced technology. There is no room for further reduction of $\langle v_n^2 \rangle$ at a given technology generation.

The input noise current $\langle i_n^2 \rangle$, however, can be reduced by increasing β (to reduce I_B) and increasing f_T (to increase h_{21}) according to (1). In particular, at relatively high current where the RF power gain is large, $2qI_B$ dominates $\langle i_n^2 \rangle$ in these devices. Therefore, significant noise improvement can only be achieved through an increase of β at relatively high biasing currents.

The approaches to improving noise performance at a given technology generation are now clear. The SiGe profiles need to be optimized for higher β and f_T under the fundamental constraint of SiGe film stability. Next, we simulated the noise parameters for various SiGe profiles at constant film stability (integrated Ge content) to determine the optimum profiles for low noise. To produce sensible results, the 2-D device structure for the standard control SiGe HBT was first calibrated to measured y -parameters. Issues related to the calibration are discussed in the following section.

III. CALIBRATION OF 2-D DEVICE SIMULATION

MEDICI [12] was used to simulate the dc and high frequency y -parameters using measured SIMS profiles. The first step is to determine the profiles based on the SIMS data. The base pinch sheet resistance can be used to calibrate the base doping profile, and determine the EB and CB junction locations. The base doping and Ge profiles also set the I_C - V_{BE} characteristics. The measurement should be made on very long emitter devices to avoid three-dimensional (3-D) effects. The carrier lifetime in the emitter can be adjusted to reproduce the I_B - V_{BE} characteristics. Bandgap narrowing (BGN) parameters can be adjusted to shift the simulated I_C , I_B - V_{BE} curves toward the measured

curves. For state-of-the-art bipolar transistors with narrow emitters, the shallow-trench isolation and extrinsic CB capacitances can often be comparable to the intrinsic CB capacitance, and are therefore nonnegligible. For accurate y -parameter simulation, all of the 2-D lateral structures must be included. The base resistance, EB and CB capacitances were extracted from measured and simulated y -parameters using a set of analytical equations [13], and then plotted as a function of $\log(I_C)$. By comparing the simulated and measured r_B , C_{BE} , and C_{BC} , one can identify the dominant factors of simulation-measurement discrepancy, and adjust the lateral doping extension accordingly. The diffusion capacitance component of C_{BE} is proportional to I_C at relatively lower currents, and can be distinguished from the depletion capacitance component. By simulating and measuring devices with different emitter widths, the contribution of the extrinsic and intrinsic elements can be distinguished.

Another important aspect is to select a proper set of physical models and coefficients. For instance, incomplete ionization, though recommended explicitly by users' manuals, often leads to an overestimation of the base resistance. At concentrations higher than $10^{18} / \text{cm}^3$, the semiconductor-metal (Mott) transition occurs, and the dopants are completely ionized. To the authors' knowledge, this, however, is not modeled correctly in today's commercial device simulators. Therefore, we intentionally used complete ionization in order to accurately simulate the base resistance, since it is of great importance for noise modeling. The mobility model was critical in determining the f_T roll-off I_C , and in our experience the Philips unified mobility model (PHUMOB) was found to be the most accurate.

IV. SiGe PROFILE DESIGN

For constant film stability, at a given geometry and doping, a higher f_T and higher β can only be realized in practice by pushing the edge of the Ge retrograde in the collector significantly closer to the EB junction (surface). The additional Ge can then be used to reduce the effective Gummel number in the neutral base for higher β , and increase the Ge grading for higher f_T [14], [15]. We are thus forced to trade high- J_C f_T roll-off performance for improved NF_{min} . Under high injection, the minority carrier charges are sufficient to compensate for the ionized depletion charges in the collector-base space charge region, thus exposing the hetero-interface between the collector and the base, which was originally masked by the band bending in the depletion region. In SiGe HBTs, since most of the bandgap offset occurs in the valence band, the collapse of the original collector-base electric field at the heterointerface reveals the valence band barrier, which opposes the hole injection into the collector under base push-out [16], [17]. The piling up of holes further induces a potential barrier in the conduction band profile, which retards the flow of electrons into the collector, and thus decreasing the cut-off frequency [17]. Fig. 4 illustrates the SiGe profile design tradeoffs. The solid profile and the dash profile have the same integrated Ge content, the upper limit of which is set by the SiGe film stability constraint [18]. The dashed profile has a larger Ge content and a higher Ge gradient in the base, and therefore higher β and f_T , and hence lower noise. The solid profile has deeper Ge retrograding into

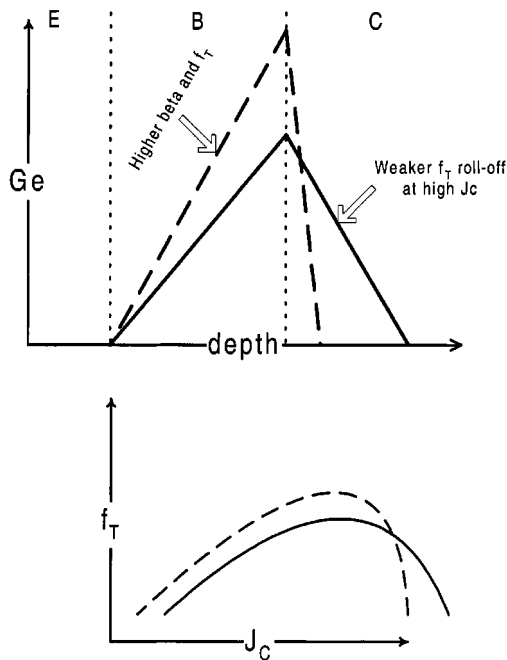


Fig. 4. Schematic of the SiGe profile design tradeoffs between improving f_T and β at low injection and suppressing the f_T roll-off at high injection.

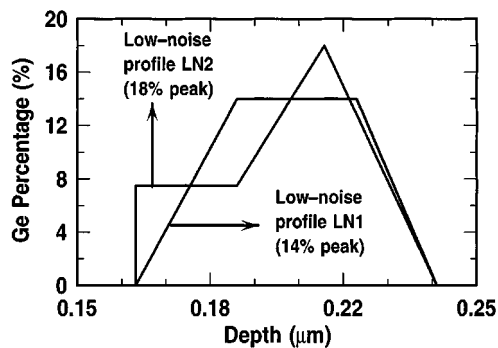


Fig. 5. Schematic of the two optimized low-noise profiles that are both unconditionally stable.

the collector, and therefore a better (weaker) f_T roll-off at high injection.

Obviously, there are numerous possibilities of SiGe profiles to choose from for a given integrated Ge content. Extensive numerical simulations were performed to determine the optimum profiles for lowest noise. The key here is to achieve noise performance improvements while minimizing the f_T degradation at high injection. Our goal is to maintain the peak f_T and f_{max} comparable to the control profile design point in the presence of a worsened high-injection barrier effect. Fig. 5 shows two such low-noise Ge profiles (LN1 and LN2) which maintain the stability, the peak f_T and peak f_{max} of the SiGe control profile, but have significantly lower NF_{min} in simulation (by 0.2 dB). All of the SiGe profiles are unconditionally stable to defect generation [18], [1] by design, as shown in Fig. 6. The linearity of the Si BJT and SiGe control devices are expected to be retained in the two low-noise profiles, because the linearity of bipolar transistors is relatively insensitive to the diffusion capacitance (base transit time) [19].

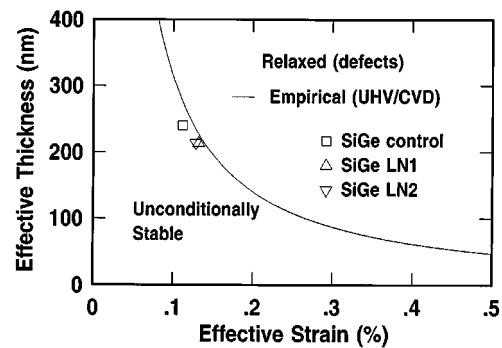


Fig. 6. Stability of the SiGe control design point and the two low noise profiles. All of these profiles are unconditionally stable [18].

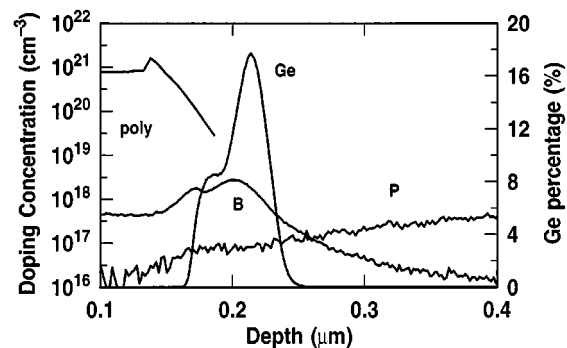


Fig. 7. Measured SIMS doping and Ge profiles for the fabricated SiGe low noise profile LN2.

V. EXPERIMENTAL RESULTS

A. Device Fabrication and Measurement

For unambiguous comparisons, the two low-noise profiles, the SiGe control profile, and a Si control profile were fabricated in the same wafer lot in a state-of-the-art $0.50 \mu\text{m}$ SiGe HBT technology [1] using UHV/CVD growth and identical processing conditions. Fig. 7 shows the doping and Ge profiles for the 18% peak Ge low-noise profile LN2 measured by SIMS. To within the SIMS resolution, the designed Ge shape is basically reproduced.

DC characteristics were measured using an HP4155. S -parameters were measured using a HP8510C vector network analyzer from 2 to 40 GHz, from which f_T and f_{max} were extracted. Noise parameters were measured from 2–18 GHz using an NP-5 on-wafer measurement system from ATN Microwave Inc. Two-tone load-pull measurements were made at 1.9 GHz with 1 MHz tone spacing.

B. Experimental Design Tradeoffs

Table I summarizes the measured transistor parameters of the four fabricated profiles. The penalty in BV_{CEO} over the SiGe control for LN1 and LN2 is due to the higher β , and should only have a small impact on LNA designs, which see a finite source impedance (i.e., not an “open”). The measured $\beta - I_C$ and curves of a $20 \mu\text{m}^2$ ($0.5 \times 20 \times 2 \mu\text{m}^2$ stripe) unit cell device are shown in Fig. 8. The corresponding $f_T - I_C$ and $f_{max} - I_C$ curves are shown in Fig. 9. The experimental results confirm the expected high injection design trade-off discussed above. The two low-noise profiles, LN1 and LN2, have a higher β and f_T

TABLE I
 SUMMARY OF DEVICE ELECTRICAL CHARACTERISTICS

| Performance | Si BJT | SiGe control | SiGe LN1 | SiGe LN2 |
|--------------------------------|-----------|-----------------|-------------|-------------|
| β at $V_{BE}=0.7V$ | 67 | 114 | 350 | 261 |
| $V_A(V)$ | 19 | 60 | 58 | 113 |
| $BV_{CEO}(V)$ | 3.5 | 3.2 | 2.7 | 2.7 |
| R_{Bi} ($k\Omega/\square$) | 12.8 | 9.8 | 10.3 | 10.7 |
| peak f_T (GHz) | 38 | 52 | 52 | 57 |
| peak f_{max} (GHz) | 57 | 64 | 62 | 67 |

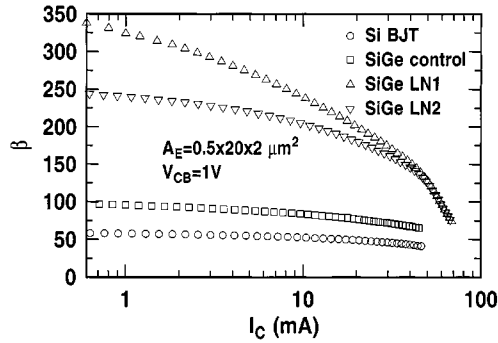
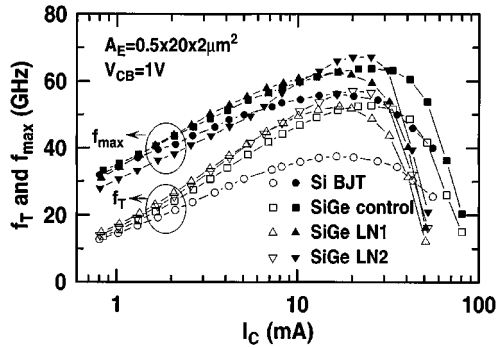


Fig. 8. Measured dc current gain versus collector current of the fabricated Si BJT, SiGe control, and the SiGe low noise profiles.


 Fig. 9. Measured f_T and f_{max} versus collector current of the fabricated Si BJT, SiGe control, and the SiGe low noise profiles.

at low J_C because of a higher total Ge content and higher Ge gradient in the neutral base. On the other hand, the SiGe control and Si BJT devices have a weaker (better) f_T roll-off at high J_C , because of the deeper Ge grading into the collector-base junction in SiGe profile design. In circuit applications, the upper biasing current limit of these devices is set by the minimum f_T and f_{max} requirements. For instance, the upper collector current limit for meeting a requirement of $f_{max} > 30$ GHz is 50 mA for the two low-noise profiles. We have also achieved the goal of maintaining the peak f_T and peak f_{max} of the SiGe control design point, despite the worsened high-injection barrier effects in the two low-noise profiles. In fact, the peak f_T and peak f_{max} values in LN2 are higher than in the SiGe control, as can be seen from Table I. The f_{max} of the two low-noise profiles are comparable to that of the SiGe control indicating that the high power gain in the control design point is retained.

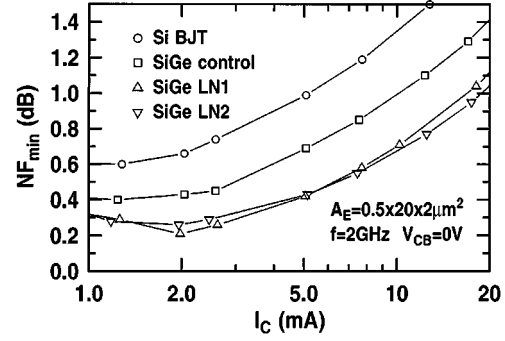
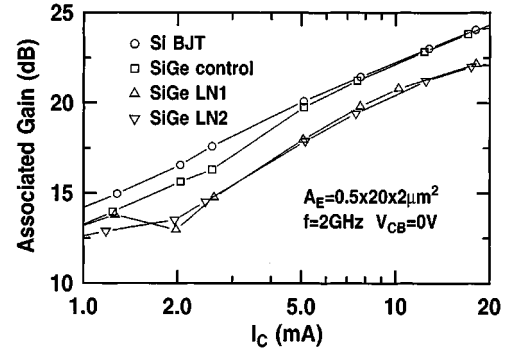

 Fig. 10. Measured minimum noise figure (NF_{min}) versus collector current at 2 GHz for the fabricated Si BJT, SiGe control, and the SiGe low noise profiles.


Fig. 11. Measured associated gain versus collector current at 2 GHz for the fabricated Si BJT, SiGe control, and the SiGe low noise profiles.

C. Noise Improvements

The above improvements of β and f_T translate into a significant improvement of the NF_{min} over the Si BJT and SiGe control profiles across the range of J_C that is of interest to LNA and mixer circuits, as shown by the measured 2 GHz NF_{min} data in Fig. 10. The LN1 profile achieves an impressive NF_{min} of 0.2 dB at 2 mA, 0.2 dB lower than the SiGe control profile. The measured noise figure improvements between profiles are consistent with our simulations. The associated gain at noise matching is still above 13 dB at NF_{min} for all of the profiles, as can be seen from Fig. 11. Similar improvement is achieved at higher frequencies for the same bias current. For instance, a 0.3 dB NF_{min} improvement is obtained at $f = 10$ GHz and $I_C = 5$ mA.

D. Linearity

To determine the device linearity, two-tone load-pull measurements were performed at 1.9 GHz with 1.0 MHz tone spacing on the $20 \mu m^2$ ($0.5 \times 20 \times 2$ stripe) unit cell device. The input third order intermodulation intercept point (IIP3) [20] for a two-tone input is used as a figure-of-merit. IIP3 was extracted in the low input power region where the third order intermodulation slope is 3:1. A larger number of IIP3 implies better linearity. IIP3 can be related to more robust distortion metrics such as adjacent-channel power ratio (ACPR) in modern digital mobile communications through compact formulas [21], [22].

Fig. 12 shows the measured output power versus input power characteristics for the four profiles at $I_C = 30$ mA and $V_{CE} =$

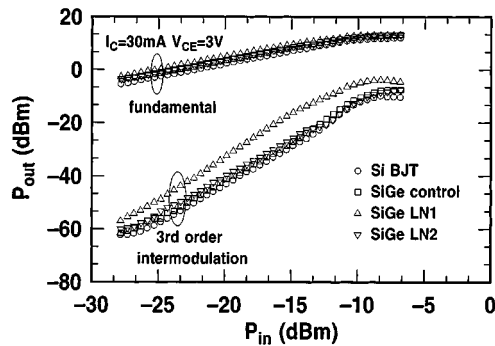


Fig. 12. Measured output power versus input power for all the profiles at $I_C = 30$ mA and $V_{CE} = 3$ V. The source and load terminations are 50Ω .

3 V. The source and load impedance used is 50Ω . The performance does not differ substantially between the various profiles. The IIP3 values are: 2.7 dBm for Si BJT, 3.0 dBm for SiGe control, -1.5 dBm for SiGe LN1, and 2.5 dBm for SiGe LN2. The power gain values are: 22.4 dB for Si BJT, 23.4 dB for SiGe control, 25.0 dB for SiGe LN1, and 24.0 dB for SiGe LN2. Small differences are attributed to the fact that IIP3 strongly depends on the load condition, and maximum IIP3 occurs at different load states for different profiles [23]. The maximum linearity efficiency ($OIP3/P_{DC}$) achieved is in the range of 7 to 10, and is comparable to GaAs HEMT (10) and GaAs HBT technology (11) [24]. Linearity efficiency is defined as $OIP3/P_{DC}$ to account for the differing load states at maximum gain and maximum IIP3 [24]. Preliminary measurements on RF subharmonic mixers fabricated with the identical low-noise profiles (LN1 and LN2) also show improved noise over the SiGe control profile, indicating that these device improvements translate to the circuit level [25].

VI. CONCLUSIONS

A unified approach to the modeling of transistor noise was presented, and used to identify the limiting factors of noise performance for a given SiGe HBT technology. Key issues related to a successful calibration of 2-D device simulation to measurement were also discussed. A higher dc current gain and a higher f_T at relatively lower current are shown to be critically important for reducing NF_{min} for a given transistor geometry and doping. By applying careful SiGe profile optimization, significant improvement in RF performance can be achieved. Using the noise model-simulation approach, new SiGe profiles were designed explicitly for improving minimum noise figure (NF_{min}) without sacrificing gain, linearity, frequency response, or the stability of the SiGe strained layer. A measured NF_{min} of 0.2 dB at 2.0 GHz with an associated gain (G_{assoc}) of 13 dB at noise matching, was obtained for the best low-noise profile, all of which represent substantial improvements in RF performance over the Si BJT and control SiGe HBT design point, and were accomplished without sacrificing SiGe film stability.

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