A Broadband 10-GHz Track-and-Hold in Si/SiGe HBT Technology

Jonathan C. Jensen, *Student Member, IEEE,* and Lawrence E. Larson, *Fellow, IEEE*

***Abstract*—High-performance multistage data converters and sub-sampling frequency downconverters typically require track and hold amplifiers (THAs) with high sampling rates and high linearity. This paper presents a THA for sub-sampling communications applications based on a diode bridge design with high-speed Schottky diodes and an improved current source approach for enhanced linearity. Implemented in a 45-GHz BiCMOS Si/SiGe process, this IC has an input bandwidth in excess of 10 GHz, consumes approximately 550 mW, and can accommodate input voltages up to 600 mV. With an input frequency of 8.05 GHz and a sampling frequency of 4 GHz, the THA has an IIP3 of 26 dBm and a spurious free dynamic range of 30 dB.**

***Index Terms*—Analog circuits, analog–digital conversion, BiCMOS analog integrated circuits, bipolar analog integrated circuits, broadband amplifiers, heterojunction bipolar transistors, high-speed integrated circuits, HF radio communication, sample and hold circuits, Schottky diode frequency converters, Schottky diodes.**

I. Introduction

NEXT-GENERATION Internet-oriented mobile satellite systems will require low-cost high-bandwidth receivers operating in the 20–40-GHz range [1]. Very often, the intermediate frequency (IF) of the receiver chain is in the neighborhood of 8 GHz, and so a second downconversion step is usually required. One possible approach for the implementation of these systems employs a sub-sampling architecture in the final stage of downconversion prior to the analog-to-digital conversion as shown in Fig. 1. The sub-sampling stage has the most exacting requirements on linearity and noise, in addition to the extremely wide bandwidth requirements.

At the same time, the increasing bandwidths of these systems put a greater demand on the digital conversion of the received signal; the analog-to-digital-converter (ADC) must operate at a higher sampling rate, while still maintaining a large signal-to-noise-and-distortion ratio. Single-stage multibit flash ADCs can be very difficult to implement at high speeds, making multistage designs more practical [2]. These multistage ADCs require a track-and-hold amplifier (THA) with linearity and bandwidth superior to that of the overall system. It is imperative that the track-and-hold be relatively free of distortion since distortion incurred in the analog portion of an ADC is difficult to remove by subsequent digital correction. Typical requirements for these systems are input bandwidths of 8 GHz and nearly 8 bits of resolution in a 1-GHz signal bandwidth.

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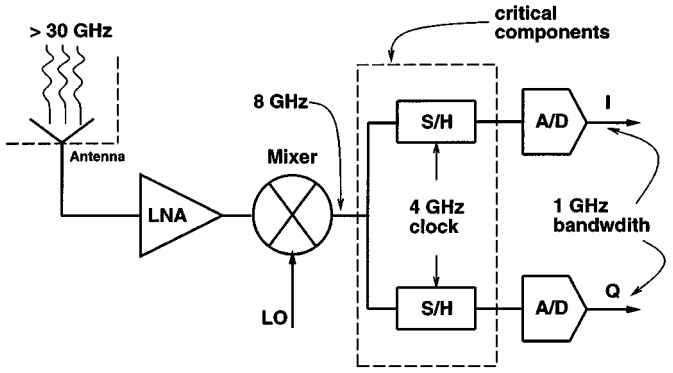

Fig. 1. Sub-sampling architecture.

Very high-speed track-and-hold amplifiers have been implemented in GaAs technology with results that approach these requirements [3]–[5]. Silicon bipolar implementations have also been demonstrated with satisfactory resolution, but with considerably lower bandwidths [6]–[9]. CMOS track-and-hold architectures have shown continued advances in high-resolution data conversion, but the typical frequency of operation is even lower [10], [11].

It is difficult to maintain low distortion in a sampling circuit operating at these bandwidths due to frequency-dependent sampling errors, which tend to grow at higher frequencies. This paper presents improved circuit design techniques to minimize these errors, and demonstrates the performance of a sub-sampling diode-bridge track-and-hold with an input bandwidth greater than 10 GHz and a IIP3 of 26 dBm at 8.05 GHz implemented in a production Si/SiGe BiCMOS technology. The sampling rate of this circuit at the required dynamic range is superior to other THAs in silicon technology, and is comparable to state-of-the-art GaAs-based circuits (see Fig. 2) [4], [12].

II. Track-and-Hold Architecture

A. Diode Bridge Design for Wide-Bandwidth Operation

In typical applications the track-and-hold amplifier samples the input voltage prior to quantization. This design uses a classic high-speed Schottky diode bridge to disconnect the output from the input and a hold capacitor to maintain that voltage (see Fig. 3) [3], [4], [12]–[14].

In the track phase, transistor Q_1 is on and current I_1 flows through the diode bridge, D_1, D_2, D_3, and D_4, resulting in $v_a = v_{\rm in}$, after a small delay. In the hold phase, Q_1 turns off, Q_2 turns on, and the currents from I_1 and I_2 are directed around the diode bridge, forward biasing the clamp diodes, D_5 and D_6, and

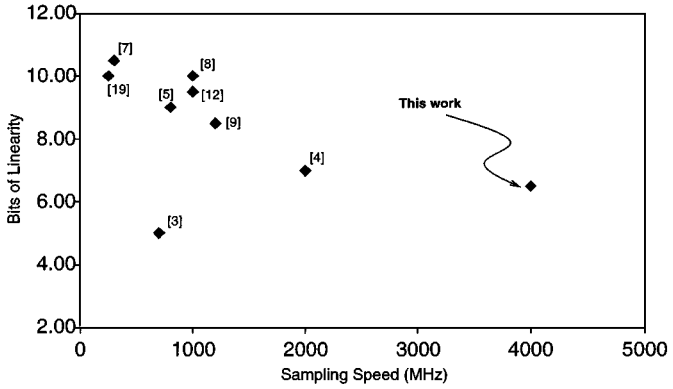

Fig. 2. Previously published work: resolution plotted against sampling speed [3], [4], [7], [8], [19], [9], [5], [12].

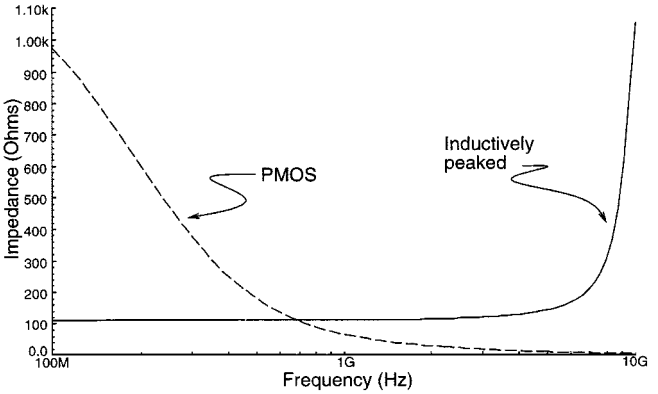

Fig. 4. Simulated output impedance of pMOS and L-R current sources.

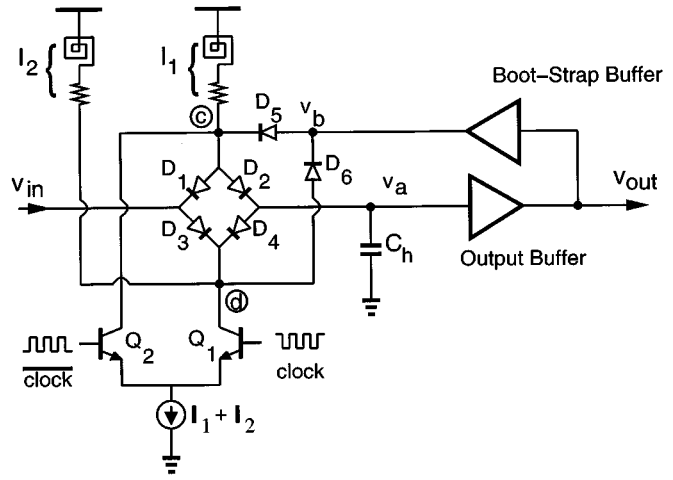

Fig. 3. Diode bridge with unity gain output and bootstrap buffers.

reverse biasing the diode bridge. At this time, v_a is disconnected from the input and maintained on the capacitor, C_h.

There is a straightforward tradeoff between the size of the hold capacitor, which determines the droop rate and hold time, and the bandwidth of the circuit. To maintain a wide bandwidth (greater than 10 GHz), a relatively small, 325 fF, hold capacitor was used. The droop rate was approximately 8 mV/ns; and in a differential design this could be significantly decreased. The sampled kT/C thermal noise from this capacitor is approximately 12 nV, which is 65.7 dB below the maximum input signal of 600 mV and well within the design goal.

B. Current Source Design for THA Applications

The current sources, I_1 and I_2 in Fig. 3, play an important role in the operation of the THA supplying approximately 14 mA to the diode bridge. Extending the sampling frequency and minimizing the distortion of the bridge requires the impedance of the current sources to remain large at high frequencies. A relatively high impedance will reduce the switching time and distortion of the circuit.

The inherently large drain–gate and drain–substrate capacitance associated with a pMOS current source transistor makes it difficult to maintain the high impedance of the circuit at microwave frequencies. A lower current source impedance will reduce the input bandwidth and degrade the aperture of the bridge; preliminary simulations indicate that pMOS current sources would not be effective at input bandwidths much above 1 GHz. Fortunately, high-quality-factor inductors are available in a Si/SiGe HBT technology, creating the possibility of employing series inductance to raise the impedance of the circuit at high frequencies, improving the overall performance.

For these reasons, a series L-R circuit is employed to increase the impedance at higher frequencies and simulations demonstrate that the input bandwidth, switching speed, and distortion of the diode bridge were improved through use of this approach. Fig. 4 shows the improvement of the simulated output impedance of a pMOS current source device compared to the L-R circuit implemented in this technology. The impedance of the pMOS current source decreases substantially after 1 GHz, while the impedance of the inductively peaked current source increases very beneficially. In this simple way, the output impedance of the current sources is improved with very little penalty in dc current consumption or noise performance.

An improved current source will not only improve the input bandwidth, but it will also increase the peak sampling rate. Remember, it is necessary to maintain currents I_1 and I_2 at a roughly constant level when the THA changes from the track to the hold mode and back again. During the transition from track to hold mode, the voltage at node *c* should drop and the voltage at node *d* should increase very quickly. Any capacitance at the current source will slow this transition and lengthen the aperture of the THA, limiting the sampling speed of the THA (see Section III-B) [13]. Simulations show that the aperture is substantially decreased from approximately 600 ps with the pMOS current source to less than 100 ps with the inductively peaked current source; the peak sampling bandwidth is improved by roughly a factor of six with this approach (see Fig. 5).

III. Track-and-Hold Distortion Analysis

The linearity of track-and-hold circuits often degrades at higher frequencies due to the frequency-dependent errors that tend to accumulate. Signal-dependent delays, modulation of the track-hold aperture, and pedestal distortion are the main concerns. This section will analyze some of these errors, and suggest techniques for their minimization.

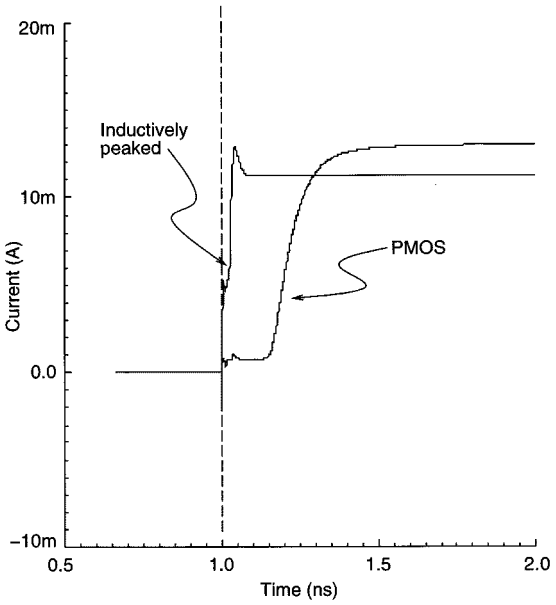

Fig. 5. Apertures of THA with inductively peaked and pMOS current sources.

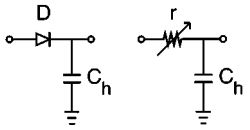

Fig. 6. Amplitude-dependent delay error model.

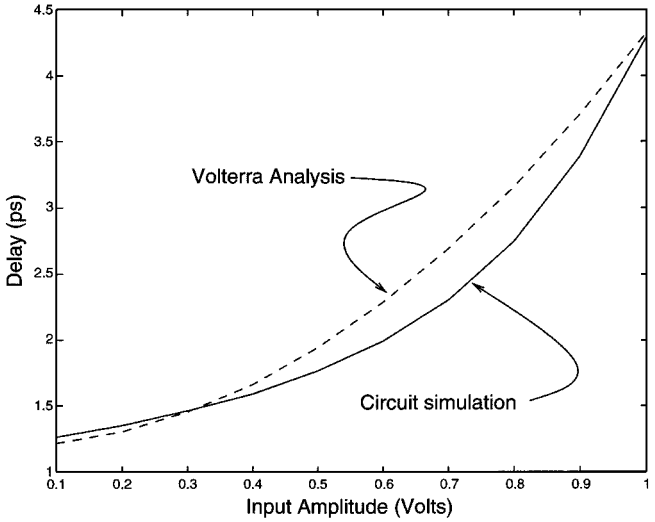

Fig. 7. Amplitude-dependent delay—Volterra analysis and circuit simulated.

A. Amplitude-Dependent Delay Error and Distortion

During the track mode, the current I_1 is evenly distributed through both sides of the diode bridge and the voltage at the output is a delayed version of the input voltage. The delay is partly a result of the linear *RC* delay through the bridge and partly a result of a complex phase term produced by higher order distortion terms. So the voltage on the hold capacitor will approximately equal the input voltage, except that there will be a small signal-dependent delay due to nonlinear distortion.

This delay error can affect the value of the signal at the time the signal is sampled, resulting in unacceptable distortion in the sampled signal. It can be analyzed using the simplified model seen in Fig. 6, with the input of the diode bridge filtered through a low-pass transfer function due to the hold capacitor. Using Volterra analysis where $v_{\text{out}} = H_1(j\omega) \circ v_{\text{in}} + H_2(j\omega) \circ v_{\text{in}}^2 + H_3(j\omega) \circ v_{\text{in}}^3 + \cdots$, the following simplified results were found for the nonlinear transfer function of the diode bridge in the track mode.

$$H_1(j\omega) = \frac{1}{1 + j\omega C_h V_t / I_d} \tag{1}$$

$$H_2(j\omega) = \frac{-V_T}{2I_d^2} \frac{\omega^2 C_h^2}{(1 + j\omega C_h V_t/I_d)^2(1 + 2j\omega C_h V_t/I_d)} \tag{2}$$

$$H_3(j\omega) \approx \frac{jV_t}{3I_d^3} \frac{\omega^3 C_h^3 (1 - j\omega C_h V_t/I_d)}{(1 + j\omega C_h V_t/I_d)^3 (1 + j5\omega C_h V_t/I_d)}. \tag{3}$$

If $v_{\text{in}} = A\cos(\omega t)$, the cubic term will contain a complex first-order term in $A\cos(\omega t)$. This term will alter the phase of the fundamental output in an amplitude-dependent manner, resulting in the signal-dependent delay seen in Fig. 7.

Using the same results, we find that the third-order harmonic distortion is

$$HD_3 \approx \frac{jV_t}{12I_d^3} \frac{\omega^3 C_h^3 (1 - j\omega C_h V t/I_d)}{(1 + j\omega C_h V t/I_d)^2 (1 + j5\omega C_h V t/I_d)} \circ v_{\text{in}}^2 \tag{4}$$

where C_h is the hold capacitor, I_d is the dc current, and ω is the frequency in radians per second. Not surprisingly, higher frequency signals will produce more distortion, and increased dc current will help to minimize the distortion. These results quantify the well-known tradeoff between current and distortion and AM-PM conversion in the diode bridge. The hold capacitor and bias current were chosen using this result to minimize these effects.

B. Aperture Error

As the THA moves into the hold state, the current flowing through the diode bridge will go to zero during a finite amount of time, known as the "aperture" [13]. Reduced capacitance in the current sources contributes to a shorter aperture and a larger signal bandwidth. If the aperture is greater than a small fraction of single cycle of the input signal, that signal cannot be resolved by the track-and-hold.

Unfortunately, the aperture can be modulated by the input signal creating nonuniform sampling and distortion. The aperture is determined by the currents flowing into and out of nodes *c* and *d* (see Fig. 8). The input signal injects a small current proportional to dv_{in}/dt, into nodes *c* or out of node *d*, depending on whether the input has a positive or negative slope. A current injected into node *c* will lengthen the aperture whereas a current drawn from node *d* will shorten the aperture. This input-dependent current will modulate the hold aperture and can be shown to be proportional to C_h/I_o [13]. Thus, a smaller hold capacitor or increased dc current through the diode bridge will help reduce the aperture error.

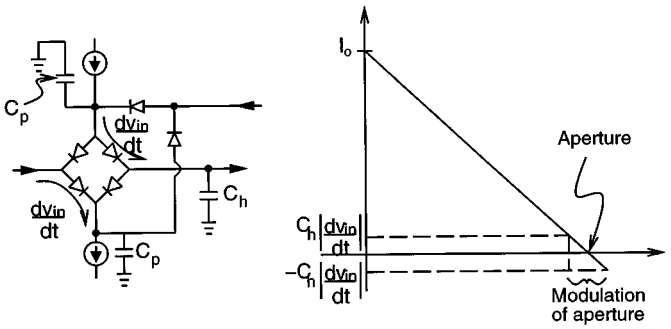

Fig. 8. Aperture distortion.

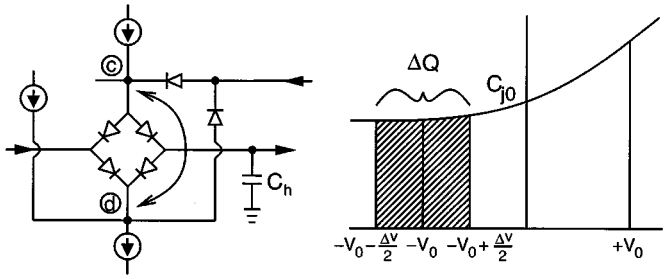

Fig. 9. Hold pedestal distortion in diode bridge.

C. Pedestal Distortion

During the track phase while the diodes in the diode bridge are forward biased, charge is stored across the diode junction and discharged when the circuit switches to the hold phase. If $v_a = v_b$, (see Fig. 9), the change in charge in diodes $D_1 \rightarrow D_4$ will be identical to the change in diodes D_5 and D_6 and no charge will be added or removed from the hold capacitor, C_h. Because of an inherent delay through the unity gain buffers, $v_a \neq v_b$, and the charge on the hold capacitor will change proportionally to the difference between the two voltages. The change in voltage across D_1, D_2, D_3, and D_4 as the THA moves into the hold phase is Δv. This Δv will add or remove charge from the hold capacitor C_h. $\Delta v = 2(v_a - v_b)$ and if $v_b = v_a \exp(-j\omega\tau)$, where τ is the delay through the bootstrap amplifier, then $\Delta v \approx 2v_a\omega\tau$ for small values of $\omega\tau$. The small-signal diode junction capacitance model gives

$$C_j = \frac{C_{jo}}{(1 - V/V_d)^n} \tag{5}$$

where C_{jo} is the zero-bias junction capacitance (approximately 2.2 fF/μm^2 for this process) and n is $\approx$ 1/2 [15]. The charge mismatch between diodes D_1 and D_2, and D_5, and diodes D_3 and D_4, and D_6, sum to create the total charge distortion added to the hold capacitor, ΔQ. This charge is found to be approximately

$$\Delta Q \cong C_{jo}V_d' \left[\frac{\Delta v}{\sqrt{2}V_d'} + \frac{\Delta v^3}{128\sqrt{2}V_d'^3} \right] \tag{6}$$

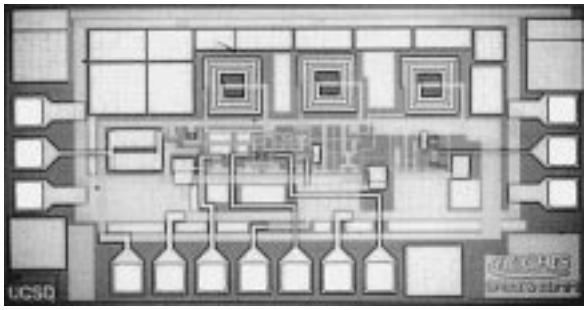

Fig. 10. Die photo of track-and-hold.

where V_d' is $V_d - kT/q$. This distortion is added to the output voltage yielding $\Delta V_{\text{out}} = \Delta Q/C_h$. The output voltage is therefore

$$V_{\text{out}} \cong v_a \left(1 + \sqrt{(2)}\frac{C_{jo}}{C_h}\omega\tau\right) + v_a^3 \frac{C_{jo}}{C_h} \frac{(\omega\tau)^3}{16\sqrt{2}V_d'^2} \tag{7}$$

and the gain compression and harmonic distortion are found to be

$$Gain = 1 + \sqrt{2}\frac{C_{jo}}{C_h}\omega\tau \tag{8}$$

$$HD3 = \frac{1}{4}\frac{a_3}{a_1}v_{\text{in}}^2 \approx \frac{1}{4}\frac{A^2\frac{C_{jo}}{C_h}(\omega\tau)^3}{16\sqrt{2}V_d'^2}v_a^2. \tag{9}$$

This distortion is signal dependent and must be reduced to maintain high signal-to-distortion levels. It can be minimized in this case by minimizing the Schottky diode junction capacitance, and by minimizing the delay through the bootstrap buffers that determines the voltage v_b. The latter was accomplished by careful design of the high-frequency feedback circuit, as described in Section V, resulting in a delay of less than 15 ps.

As mentioned in Section III-B, the current delivered by the passive current sources will change as the circuit moves from the track mode to the hold mode. Even though the current through the diode bridge in the track mode is not equal to the current through the clamp diodes in the hold mode, the circuit will exhibit no pedestal distortion. The symmetry of the THA allows the current through the diodes, and hence the diode voltage, to be different for the clamp diodes and bridge diodes without introducing distortion.

IV. Experimental Results

The track-and-hold circuit was implemented in a production 0.5-μm Si/SiGe BiCMOS process [16], [17]. Total power consumption was approximately 550 mW, including the 50-Ω output buffer, with a power supply voltage of 5.2 V. A die photograph of the complete chip is shown in Fig. 10. The chip measured 2 $\times$ 1 mm including probe pads.

The measured input 3-dB bandwidth of the circuit in the track mode exceeds 10 GHz. For an 8-GHz input and sampling frequency of 4 GHz, the measured IIP3 was 26 dBm and the measured IIP2 was 24 dBm (see Fig. 11). The IIP2 was the major

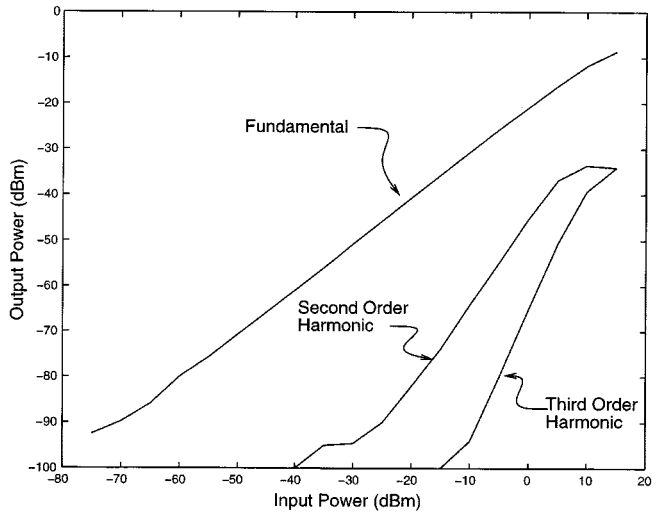

Fig. 11. Fundamental, second-order, and third-order intermodulation curves as a function of input power.

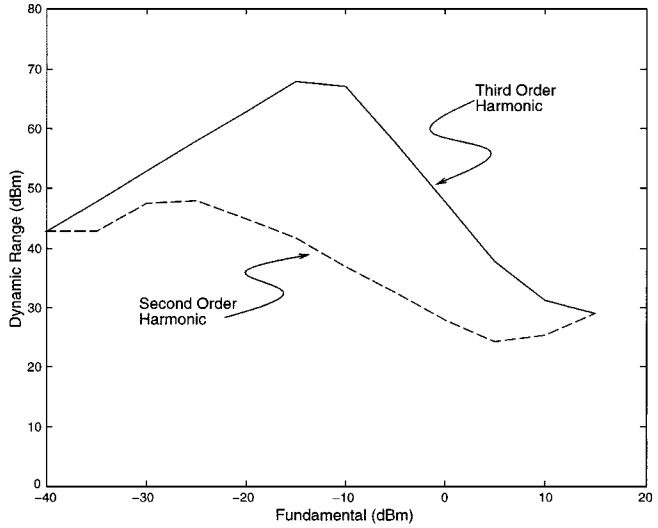

Fig. 12. Difference between fundamental and distortion terms.

source of distortion, but can be reduced significantly at the expense of a doubling of the dc power with a differential design [13], [12]. In a 10-GHz bandwidth, the maximum spurious free dynamic range (SFDR) between the second-order distortion and the fundamental is approximately 30 dB or approximately 4.7 bits (see Fig. 12). If we consider only the third-order distortion term, the SFDR between the third-order distortion and the fundamental in a 10-GHz bandwidth is 41 dB or ≈ 6.5 bits.

The input to the circuit is broadband impedance matched to 50 Ω with a measured voltage standing-wave ratio (VSWR) of less than 1.4:1 for frequencies up to 10 GHz. An output driver similar to the one in [18] was used to drive a 50-Ω load impedance. The gain through the track-and-hold was -12 dB; the large track mode attenuation was a product of the high series resistances in the silicon Schottky diodes.

The measured hold-mode droop rate was approximately 8 mV/nS for a 2.1-GHz input and 1.0-GHz clock (see Fig. 13). The droop rate can be substantially reduced with a differential design.

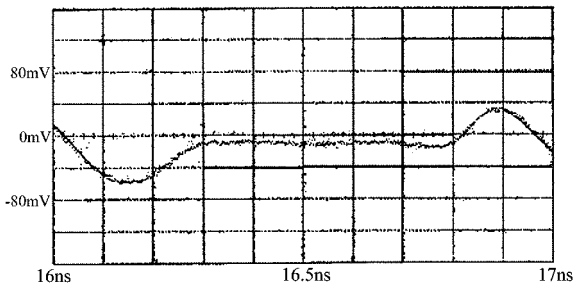

Fig. 13. Hold phase with 1-GHz clock and 2.1-GHz input signal.

V. Conclusion

An improved design has been presented for a track-and-hold circuit achieving wider bandwidth and lower distortion than previous circuits implemented in silicon technology, with performance comparable to the best GaAs-based track-and-holds. A standard diode-bridge design was used with an improved current source approach using series inductive loading to reduce the aperture time and lower distortion. to extend performance to higher frequencies. The aspects of the track-and-hold design that lead to distortion at high frequencies were analyzed, and improvements in the circuit implemented to minimized these effects. The circuit exhibited an track-mode bandwidth in excess of 10 GHz. This circuit can be used as a building block for next-generation ultrawide bandwidth satellite communication systems.

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He was co-recipient of the 1996 Lawrence A. Hyland Patent Award of Hughes Electronics for his work on low-noise millimeter-wave HEMTs, and the 1999 IBM Microelectronics Excellence Award for his work in Si/SiGe HBT technology.