NOISE POWER OPTIMIZATION OF MONOLITHIC CMOS VCOS

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ABSTRACT

A small-signal and large-signal analysis was performed on a CMOS microwave VCO and the key contributors to its phase noise were determined. These analyses were verified for a 2.0 GHz, fully integrated L-C VCO in 0.6μm CMOS technology and a phase noise of -103dBc/Hz at 100KHz frequency offset with DC power consumption of 22mW was obtained. These noise analyses can be used to optimize the phase noise of the VCO for a given power consumption.

I. INTRODUCTION

Voltage controlled oscillators (VCOs) are very important building blocks for radio transceivers, since their performance usually sets the limits on the dynamic range and the jamming sensitivity of a radio transceiver. Designing a spectrally pure high frequency VCO in technologies like CMOS is very attractive for its possible use in integrated wireless transceivers. However monolithic implementations of these VCOs at RF frequencies have been known to have poor phase noise.

The optimization of monolithic VCO performance has largely been done empirically to date. What is required is an accurate analytical technique that identifies key contributors to the phase noise, which can be used to optimize the phase noise performance of the VCO. We provide such an analysis here and demonstrate good agreement for a fully monolithic circuit.

II. CIRCUIT DESCRIPTION

The schematic of the test VCO circuit is shown in Fig. 1, based on [1]. Transistors M_1 and M_2 act as negative resistance generator to overcome the loss in the L-C tank circuit.

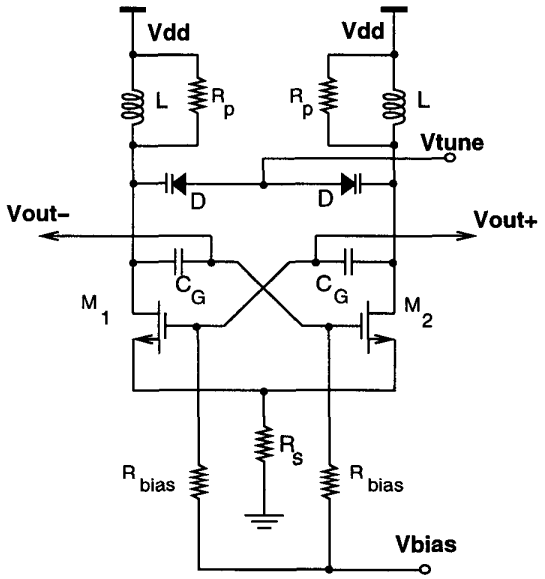

Figure 1: Schematic of the LC CMOS VCO.

The inductor is constructed as a multilevel on-chip spiral inductor and the variable capacitance is implemented by a p+/n-well varactor diode. The network of capacitor C_G and resistor R_{bias} is used to keep devices M_1 and M_2 in the saturation region most of the time during an oscillation cycle, so that the loaded Q of the tank circuit is maintained. Capacitor C_G is a poly to n-well capacitance and R_{bias} and R_s are unsilicided poly resistors. The output is buffered by common source MOSFET devices (not shown) which are loaded externally. Input $Vbias$ is used to control the VCO power consumption and oscillation amplitude. The technology of implementation is HP 0.6μm digital CMOS process offered through MOSIS. Fig. 2 shows the photograph of the fabricated circuit. All the components used in the VCO were also embedded in test structures to enable RF modeling.

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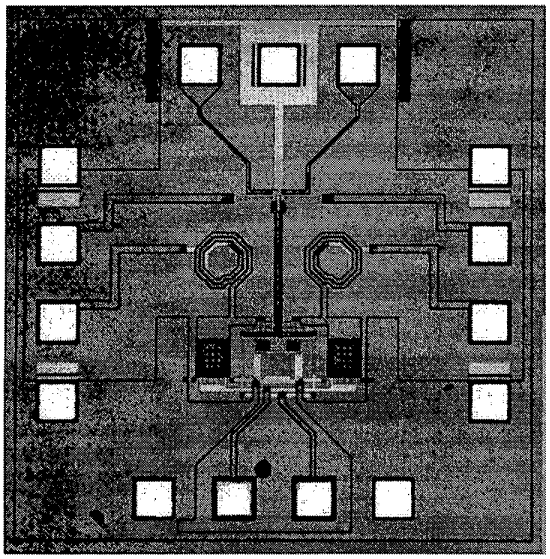

Figure 2: Photograph of the fabricated circuit.

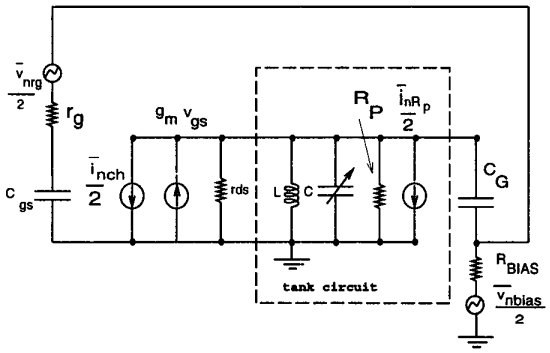

Figure 3: Noise generators in the VCO differential half circuit.

III. LINEAR ANALYSIS OF THE NOISE SPECTRUM

The differential half circuit of the VCO with noise generators is shown in Fig. 3. The gate-to-drain capacitance as well as the coupling of the channel noise to the gate are ignored (since operating frequency is about one-tenth of the device f_T). Then the main noise generators in the circuit can be listed as:

1. **Thermal Noise of the Parasitic Gate Resistance:** $\overline{v^2_{nrg}} = 4kTr_g df$

2. **Thermal Noise of the MOSFET Channel:** $\overline{i^2_{nch}} = \frac{8kT}{3} g_m df$

3. **Thermal Noise of the Parasitic Resistance in the Tank:** $\overline{i^2_{nRp}} = \frac{4kT}{R_p} df$

4. **Thermal Noise of R_{bias}:** $\overline{v^2_{nbias}} = 4kTR_{bias} df$

The approximate closed loop transfer function to the output node V_{out} is computed for each of these noise generators acting independently. The resultant approximate expressions for noise power spectral densities (PSD) at a small frequency offset of f_m from the center frequency f_o, are listed in Table I.This assumes that: (1) resistor R_{bias} is large enough to be neglected in comparison to the total capacitance parallel to it at RF frequencies (2) the impedance of the tank near resonance can be approximated as,

$$Z_{tank}(f_o + f_m) \approx R_P(1 - j(2Q_L)\frac{f_m}{f_o}) \quad (1)$$

Since all these noise generators are uncorrelated, these contributions are added together to obtain the total noise power at a frequency offset of f_m (denoted by S_{vv}). If the RMS oscillation signal at the output, V_{rms}, is found from simulations on the circuit, then total single-side-band noise to carrier ratio is given by,

$$\Gamma(f_m) = 10log_{10}\left[\frac{S_{vv}(f_m)}{V^2_{rms}}\right] \quad (2)$$

Which expands to,

$$\Gamma(f_m) = 10log_{10}\{\frac{1}{g^2_m}\left(\frac{f_o}{2Q_L f_m V_{rms}}\right)^2 |H_{filter}|^2 \frac{4kT}{R_P}(1+F)\} \quad (3)$$

where,

$$F = \frac{2}{3}g_m R_p + g^2_m r_g R_p + \frac{g^2_m R_P}{(2\pi)^2 R_{bias} C^2_G f^2_o} \quad (4)$$

Where $f_{filter} \approx 1/(2\pi R_{bias} C_G)$. The form of the Eq.(3) is similar to "Leeson's Equation" [2], but no empirical parameters (such as the excess noise factor) are required in Eq.(3). In fact, the value of excess noise factor (F) in Leeson's Equation is easily determined as in Eq.(4)

IV. NONLINEAR ANALYSIS OF NOISE SPECTRUM

The linear model is not expected to accurately describe the VCO operation for all conditions. This is because the linear model predicts exponentially increasing amplitude of oscillation at start-up, which is ultimately limited by mechanisms that are nonlinear in nature.

Noise Source	Approximate Transfer function
i_{nrp}	$\frac{1}{g^2{}_m}\left(\frac{f_o}{2Q_L f_m}\right)^2 \lvert H_{filter}\rvert^2 \frac{\overline{i^2}_{nrp}}{4}$
v_{nrg}	$\left(\frac{f_o}{2Q_L f_m}\right)^2 \lvert H_{filter}\rvert^2 \frac{\overline{v^2}_{nrg}}{4}$
v_{nrbias}	$\left(\frac{1}{2Q_L f_m}\right)^2 \lvert H_{filter}\rvert^2 \left(\frac{1}{R_{bias}C_G}\right)^2 \frac{\overline{v^2}_{nrbias}}{4}$
i_{nch}	$(\frac{f_o}{2Q_L f_m})^2 \frac{1}{g_m^2} \frac{\overline{i^2}_{nch}}{4}$

Table I: Approximate closed loop transfer functions from each noise generator to the output. $H_{filter} \approx \frac{C_G}{(C_G+C_{gs})}$

During an oscillation cycle, the parameters used in Eq.(3), such as g_m, R_p and f_o, change as the bias point of the MOSFET and the varactor diode changes. The noise generated is thus acted upon by a network which is time varying. This system has been shown to be a Linear Time Variant (LTV) system for small noise input by [3] and [4].

A. Hajimiri and T. Lee[3], have shown that such a system can be modeled by its time varying impulse response $h_\phi(t, t_1)$ from each noise generator to the excess phase at the output. The function $h_\phi(t, t_1)$ is the excess output phase $\phi(t)$ that results when an impulse is applied from a noise generator to the circuit at time t_1. The function $h_\phi(t, t_1)$ is periodic function of t_1 and is a step function with respect to t.

The impulse responses $h_\phi(t, t_1)$ were determined by simulation for every noise generator (instead of using just one composite noise generator as used in [5]). For these simulations, the extracted model of the VCO was used with the HSPICE simulator. The VCO was operated at 2.15GHz and after the oscillation waveform reached steady state, a voltage (or current) impulse was injected at the noise source and resultant phase shift from the unperturbed waveform was measured. Twenty such parametric simulations were performed with the impulse injection time moving across one period of the VCO. Simulation tolerances and time steps were maintained at very accurate levels and the typical impulse energy used was $1pC$(or $500pVsec$).

Fig. 4 shows one such example of $h_{\phi,R_s}(t_1)$ for a noise generator in the tail resistance R_s of the differential pair. Fourier series coefficients c_{iRs} of $h_{\phi,R_s}(t_1)$ were determined. The resultant phase noise contribution at a frequency offset of f_m due to R_s can then be estimated by using the expression,

$$\Gamma(f_m) \approx 10\log\left[\frac{4kTR_s\sum_{i=0}^{\infty} c_{iR_s}^2}{4f_m^2}\right] \qquad (5)$$

The same process is repeated for other noise generators in the circuit and all the noise contributions were added in power.

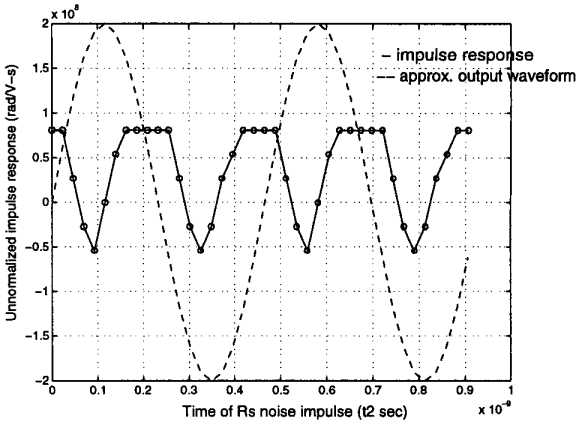

Figure 4: Time varying impulse response to the excess phase for a noise generator in the tail of the differential pair.

V. CIRCUIT OPTIMIZATION FOR THE BEST NOISE PERFORMANCE

Based on the linear and nonlinear analyses, following inferences can be drawn for reducing the phase noise of the VCO.

1. *A high loaded Q of the tank circuit is essential from Eq.(3).* Hence the inductors used in the design were constructed out of series connection of three octagonal levels of metal (7-turns, L = 4.05nH, Q = 3.3 at 2GHz). The varactor diodes were constructed out of an array of p+/n well junctions connected in parallel to increase their Q. Capacitor C_G and R_{bias} maintain the loaded Q during most of the time in an oscillation cycle.

2. *Reducing the contribution of resistances.* To reduce the contributions from the gate resistance (r_g), the MOSFET gate fingers were shorted from both sides (Fig. 5). A high value of C_G reduces f_{filter} in Eq.(4), thus reducing the noise contribution from R_{bias}.

3. The impulse response of the noise generator in the tail current setting resistor, shown in Fig. 4, shows high DC offset compared to the impulse responses of other noise generators. This high average value indicates that $\frac{1}{f}$ noise in this branch up-converts to the $\frac{1}{f^3}$ noise region near the oscillation frequency [3].This is basically suggesting that the current noise in this branch gets up-converted near the carrier as the MOSFET devices start switching. Hence a small resistor was used as the tail current generator instead of a MOSFET current source.

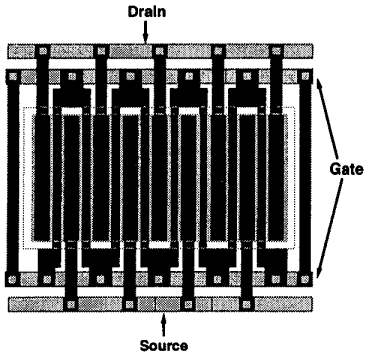

Figure 5: Layout of the reduced gate resistance MOSFET.

Table II: The comparison of predicted phase noise values and the measured phase noise values.

I_{DC} (mA)	Γ(100KHz) Linear SSB (dBc/Hz)	Γ(100KHz) Measured SSB (dBc/Hz)	Γ(100KHz) LTV SSB (dBc/Hz)
5.15	-100.52	-98.83	-90.6
5.78	-102.59	-99.83	-93.95
7.39	-103.29	-103.33	-95
10.6	-102.15	-94.33	-94.38

VI. EXPERIMENTAL VERIFICATION OF THE MODELS

Measurements were performed on unpackaged VCO dice using a Alessi RF probe station and the VCO spectrum was analyzed by HP8565E spectrum analyzer with HP85671A phase noise utility. Fig. 6 shows one noise spectrum of the VCO as the function of the frequency offset from the carrier frequency. The values of the SSB phase noise, measured at a frequency offset of 100 KHz, as the function of current consumption, are listed in Table II. The components of the tank were modeled at these frequencies and these values were used in Eq.(3) and Eq.(5). These predictions are also listed in Table II.

It is clear that the predictions by both the models come close to the measured values. The discrepancies can be partially attributed to the highly simplified nature of both the analyses, to the uncertainties surrounding the values of some components as well as to the imperfect limiting action offered offered by the output devices at RF frequencies. The predictions of the linear model seem to be excellent at relatively low power consumption whereas it tends to underestimate the phase noise at high currents.

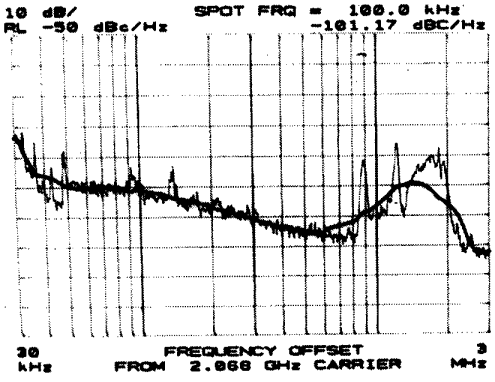

Figure 6: Measured phase noise spectrum of the VCO.

VII. CONCLUSION

We have presented linear and LTV analysis for a radio frequency, fully integrated, CMOS VCO. We have shown that the analysis comes very close to the observed values of phase noise in spite of the integrated nature of the VCO. The contribution of each noise generator to the output can be separately estimated and optimized. Such analyses can be helpful to predict noise performance of the VCO during the design phase and also for studying VCOs.

VIII. REFERENCES

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