Abstract

Next-generation wireless communication will require improved transmitter technology for a variety of applications, from advanced handsets to improved base stations. The UCSD Center for Wireless Communications has embarked on an ambitious program to develop improved power amplifier devices, architectures, and circuits for next-generation wireless communications applications. This article summarizes some emerging power-amplifier technologies for future communication systems, including new linearization approaches, power management techniques, and new semiconductor devices.

Device and Circuit Approaches for Improved Wireless Communications Transmitters

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Wireless communications systems continue to explode in importance in both the commercial arena and the military domain. However, while data rates are increasing to accommodate video and data as well as voice traffic, there is a conflicting need to reduce power consumption and extend battery lifetime. New semiconductor device technologies and circuit architectures hold the promise of significantly mitigating this conflict. This article summarizes the results obtained from an ongoing research program at the University of California of San Diego Center for Wireless Communications to optimize the performance of power amplifier (PA) technology for wireless applications.

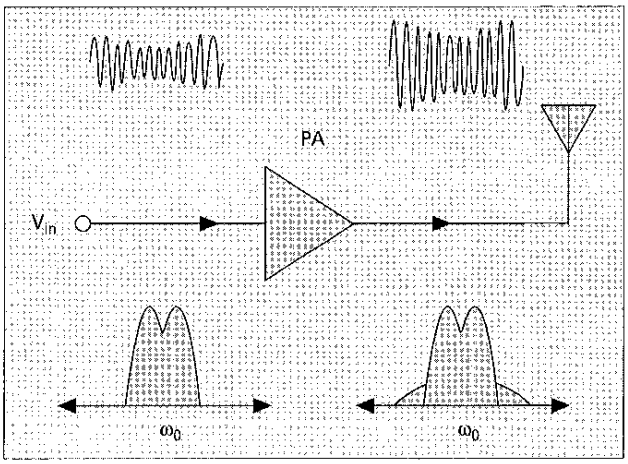
Power amplifiers have some of the most challenging requirements of all the aspects of a wireless transceiver. They have to produce a high-power narrowband signal at the antenna port, while at the same time drawing as little dc power as possible (resulting in high *power-added efficiency*). Multiple signals, closely spaced in frequency, are passed through the amplifier, and the spectral regrowth and intermodulation that results from these multiple signals create severe limitations on the output power.

The next section will review typical PA requirements, with particular focus on the wireless handset. Base station applications will also be reviewed where appropriate.

Power Amplifier Requirements

The transmission of high-power radio frequency signals through the antenna port of a handset or base station is fundamentally limited by the distortion generated by the PA, and the dc power consumed by that amplifier. In most cases distortion can be reduced, but only at the expense of increased dc power dissipation. The distortion in the PA results in spectral regrowth of the output signal: an increase of the transmitted bandwidth and a corruption of the desired signal within the original bandwidth. This is illustrated schematically in Fig. 1. This spectral regrowth arises from the fact that any nonlinear operation on a waveform containing multiple frequencies creates *new* frequencies at sums of integral multiples of the original frequencies. Some of these new signals are at frequencies adjacent to the original signal, and can create significant corruption of the *desired* signals at these intermodulation frequencies.

Although PA distortion creates problems for *all* communications systems, it is especially detrimental to *mobile* wireless communications systems, where the wide variations in received power together with spectral regrowth can corrupt adjacent channels in a particularly extreme manner. This is due to the fact that received power, by either the base station or the handset, varies dramatically with both time and frequency due to the presence of multipath, shadowing, and other time-varying effects; received signal levels can vary by over 60 dB in the



■ **Figure 1.** *Nonlinear operation of a transmitter power amplifier results in spectral growth of the original signal, corrupting adjacent channels.*

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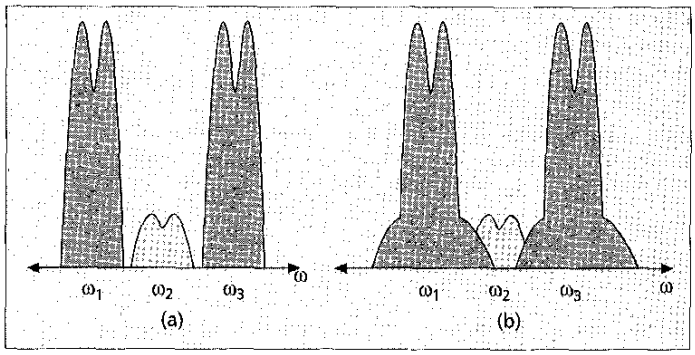
millisecond time frame. As a result, the spectral regrowth of a *large*-amplitude channel can corrupt the desired signal in a *small*-amplitude adjacent frequency band, as shown in Fig. 2.

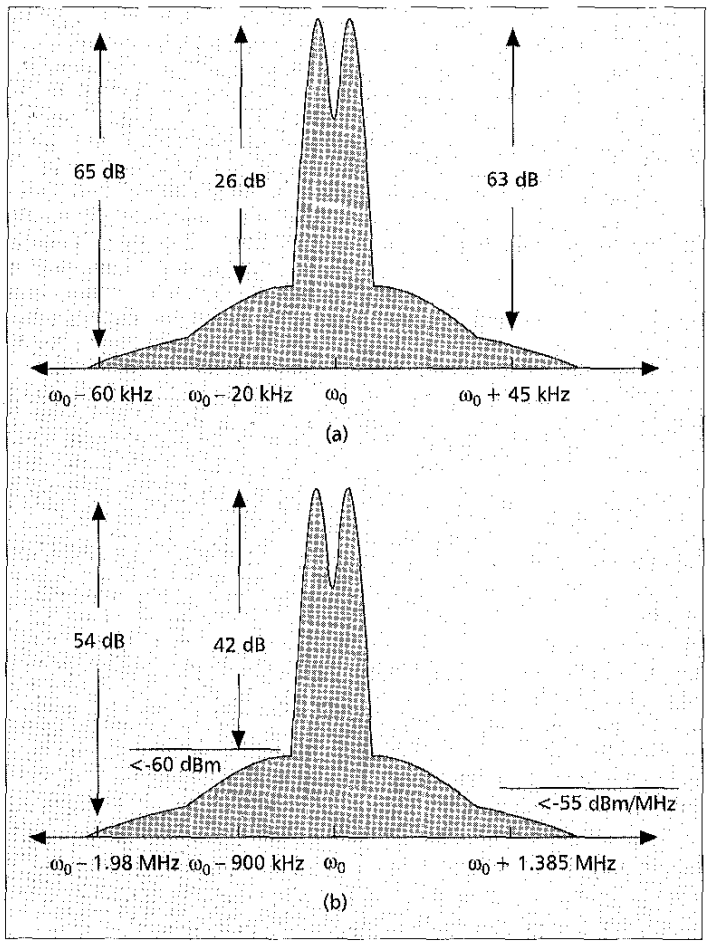
The amount of allowed spectral regrowth varies between wireless communications standards, and is a complex function of channel spacing, modulation format, and fading environment. As an example, the *adjacent channel power rejection* (ACPR) requirement — a measure of spectral regrowth — is shown in Fig. 3 for several wireless communication standards. For example, the United States domestic analog (AMPS) standard utilizes a frequency-division multiple access scheme, with a unique frequency allocated to each user during active periods. The spacing between the channels is 30 kHz, so the PA must have sufficiently small spectral regrowth that there is insignificant radiated power 30 kHz from the center of the transmitted channel, with a carrier frequency of approximately 850 MHz. In particular, the AMPS standard specifies that the spectral regrowth will be less than 26 dBc at a frequency only 20 kHz removed from the desired frequency. The PA must be very linear indeed!

At the same time, the IS-95 digital (CDMA) standard multiplexes many different users into a single 1.25 MHz wide-bandwidth signal, but this signal must coexist with adjacent



■ **Figure 2.** *Performance of power amplifiers in multichannel transmitters: a) ideal response; b) response corrupted by adjacent channel interference.*

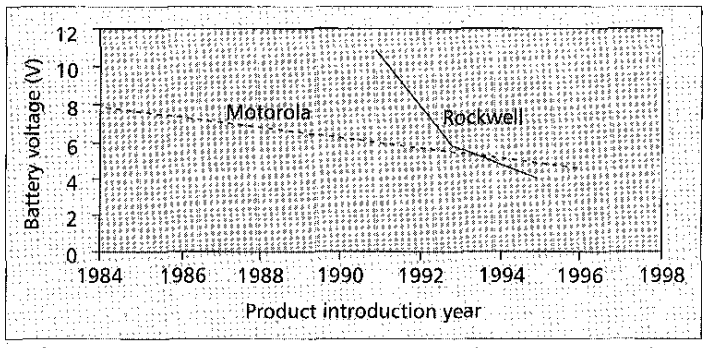
analog carriers as well as, potentially, other CDMA signals at differing carrier frequencies. In this case the linearity requirements can be more severe, as shown in Fig. 3b, because the wider bandwidth of the modulated signal will lead to wider bandwidth distortion products, although the minimum channel spacing remains nearly the same. In this case, the specifications require that the spectral regrowth be less than 42 dB below the carrier at frequencies between 900 kHz and 1.98 MHz away from the carrier, and less than 54 dB below the carrier at frequencies greater than 1.98 MHz from the carrier. In addition, there is an *absolute power* specification of less than –60 dBm in a 30 kHz bandwidth greater than 900 kHz from the carrier, or less than –55 dBm in a 1 MHz bandwidth at frequencies greater than 1.385 MHz away from the carrier. All of these specifications require a high degree of linearity in the transmitter PA.



■ **Figure 3.** *Adjacent chaennel requirements of: a) the analog AMPS cellular standard; b) the IS-95 CDMA standard.*

At the same time that the PA must maintain a high degree of linearity, a conflicting goal is to obtain an order of magnitude reduction in energy consumption in wireless communication systems and, as a result, a dramatic drop in battery weight. While battery technology itself is advancing, the increase in battery energy density over time is much slower than that of typical digital or analog integrated circuit (IC) technology. Figure 4 shows the historical drop in dc power supply voltage in representative handheld commercial communication systems [1]. An important factor is the reduction in battery voltage, which has gone from 7 V to 3 V over the last five years. The lower battery voltage is conducive to lower power dissipation in the digital parts of the communication system. For the radio frequency portions, however, a lower power supply voltage often creates serious challenges in order to maintain the necessary power-added efficiency and linearity of the PAs. In fact, the most daunting challenge facing radio frequency technologists today is the dilemma of increasing power-added efficiency while maintaining amplifier linearity in the face of steadily dropping dc power supply voltages.

To achieve the objective of dramatically lower power dissipation in the communication systems, while at the same time maintaining linearity of the PA, a variety of areas must be addressed. Modulation techniques are required that employ the lowest possible amount of energy and bandwidth per bit, and can be implemented with efficient power-amplifier circuits (which tend to be nonlinear). Transistors with very low on-resistance are needed for efficient power handling with low battery voltage.



■ **Figure 4.** *Historical values of commercial wireless system power dissipation and battery voltage vs. time.*

Devices that are inherently more linear are needed for both transmitter and receiver. We have developed a number of concepts to increase output PA efficiency, while maintaining adequate linearity.

High-Frequency Dc–Dc Converters for Active Power Management of Power Amplifiers

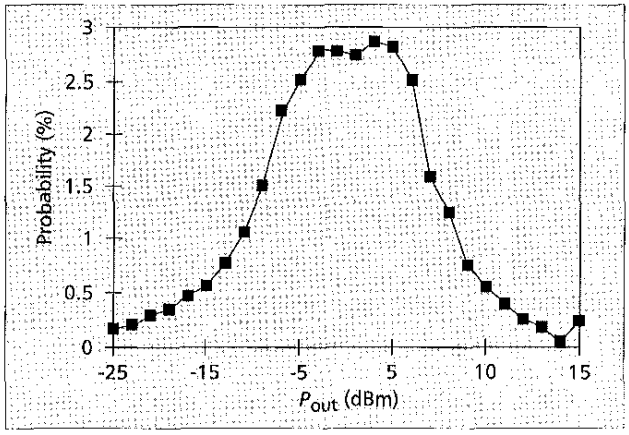
Power amplifiers need to function over a wide range of output power levels, as determined by the variable signal envelope associated with most modulation formats, together with fading statistics and varying mobile-to-base-station distances. This is especially true of CDMA systems, where handset powers are varied on a continuous basis to minimize the effects of the near–far problem [2]. For example, although the peak handset output power in an IS-95 CDMA handset is required to be over 300 mW, the radiated output power is often below 1 mW, and its time-average value is near 10 mW, as shown in Fig. 5 [3]. Power amplifier efficiency typically drops rapidly at the reduced power levels, leading to low overall average system efficiency. We have addressed strategies to improve PA efficiency, particularly at low power levels, which can dramatically improve overall system efficiency. To improve the situation, the dc current, dc voltage, or both can be varied as the output power changes. Fig. 6 schematically shows how the dc bias point of an amplifier can be varied as the power is reduced from its maximum (saturated) value to a much smaller value in response to lowered output power requirements.

The most straightforward way to vary the bias conditions is to alter the transistor dc drain (or collector) current. In class AB mode the current waveform is asymmetric, and the dc average current varies automatically with output power level. In the limit of class B operation, the dc bias varies according to the square root of output power, and the power efficiency varies as $P^{0.5}$ over a narrow range (albeit at some cost in linearity). Dynamic gate biasing (changing bias conditions as a function of input power by using an input signal envelope sensitive biasing network) can be used, and has been demonstrated in several recent PAs [4]. It is also possible to vary the dc drain or collector supply voltage in accordance with the output power level. The most desirable solution is to simultaneously vary dc bias current (through the gate or base voltage) and drain or collect supply voltage.

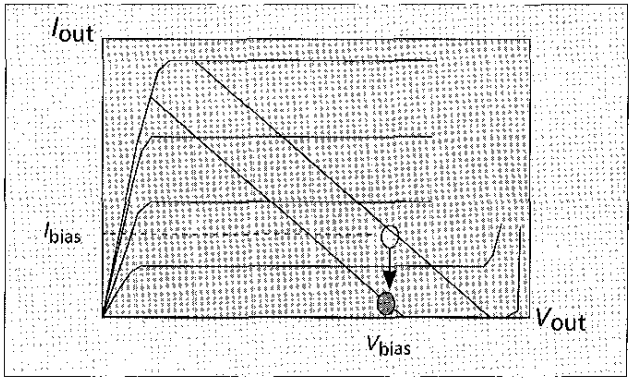
To enable changing the voltage supply with output power, we have implemented dc–dc converters of small size, in a technology (GaAs heterojunction bipolar transistor, HBT) which can be integrated monolithically with the PA itself. A schematic is shown in Fig. 7. The dc–dc converter employs a high switching frequency (10–20 MHz), which allows its output to be modulated rapidly to track the changing envelope of the output signal. Typical waveforms in cellular handsets have envelope variations in the 50 KHz–2 MHz range, according to different standards. The high switching rate of the converter also permits small inductors and capacitors to be used in the device, while minimizing ripple.

The converter uses a boost topology, providing an output voltage in the range 3–10 V for an input voltage of 3.3 V. The converter employs a power HBT, capable of handling up to 1A of current. The inductor, Si Schottky rectifier, and output capacitor are external elements. The circuit incorporates a pulse-width modulator in order to allow a dc input control voltage to regulate the output voltage. Efficiency of the converter is dependent on the output load conditions, and is typically in the range 65–75 percent.

With the dc–dc converter, the overall amplifier structure is that shown in Fig. 7. The input signal power is sensed with an envelope detector, which controls the value of V_{cc} for the PA stage. The value of the V_{dd} voltage was chosen to be somewhat larger than the amplitude of the RF signal swing at the drain of the device. Figure 8 shows the efficiency of the combined system as a function of output power. The value shown incorporates the inefficiency of the dc–dc converter as well as that of the amplifier. At the highest output power levels, the amplifier alone is more efficient, since there is no loss associated with the voltage converter. At lower power levels the sys-



■ **Figure 5.** *Time histogram showing the transmitted power profile of an IS-95 CDMA handset. [3].*

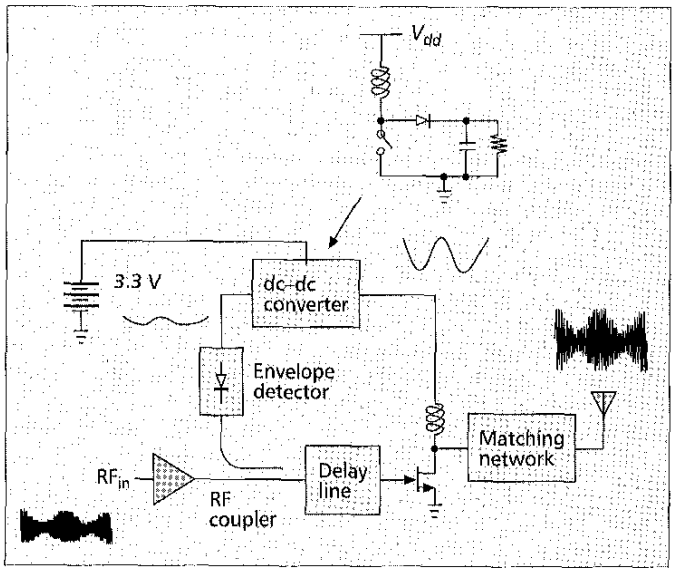


■ **Figure 6.** *A schematic representation of output transistor characteristics and load line. The dc bias conditions at maximum power are shown, as well as desirable directions in which to vary the bias at lower output power levels.*

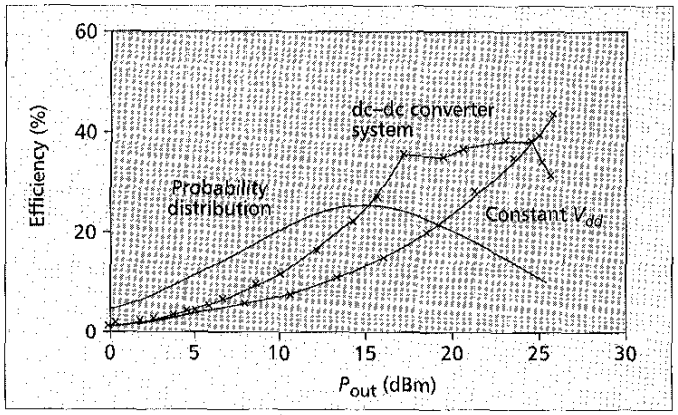
tem with the dc–dc converter is superior, because of the ability to tailor the power supply voltage optimally. By using the dc–dc converter with the PA, a significant improvement of overall efficiency results because the net energy consumption of the system is dominated by the low-power regime, where the amplifier alone is highly inefficient. After averaging the energy consumption weighted by probability of usage, the amplifier overall efficiency was increased by a factor of x 1.4. Further increases should be possible, with optimized ICs which integrate dc–dc converter and PA (together with an external inductor).

As the input power varies and the drain voltage of the RF output transistor changes correspondingly, in general the RF gain also varies. It is critical to avoid introducing distortion by the power supply time-dependence. To accomplish this, and to optimize the efficiency of the amplifier, we also controlled the gate bias voltage V_{gg} in accordance with the signal level. The overall gain can be flattened to within ±1 dB up to saturation; the resulting linearity has been shown to be adequate for IS-95 requirements.

Another possibility which is being pursued is to utilize digital switching or a combination of digital switching and analog dc–dc converters to optimize the efficiency and linearity of the amplifier by properly changing the bias voltage at the collector and base of an HBT or the drain and gate of an HFET. Such switching between different battery cell voltages can result in significant efficiency and linearity enhancement even for a two-stage switching. The possibility of employing integrated MEMs switches which consume very little power is being considered. A detailed analysis indicates that significant improvements in efficiency while maintaining complete linearity for class A amplifiers can be achieved with stepwise digital control.



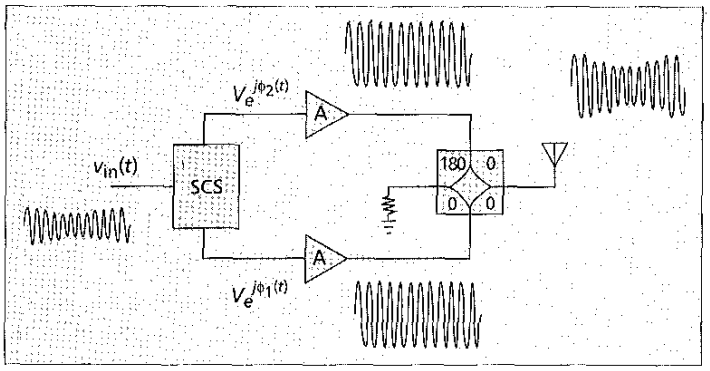
■ **Figure 7.** *A block diagram of the power amplifier employing a dc–dc converter.*



■ **Figure 8.** *The measured efficiency of the amplifier operated at constant V_{dd} value and with a dc–dc converter (to provide V_{dd} variable with input power). Also shown is a representative profile of power usage probability.*

Bandpass Delta-Sigma Power Amplifiers

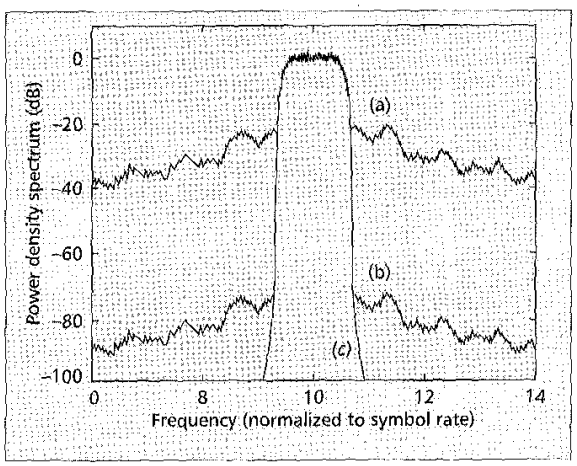
An additional approach to high efficiency is to use a switching mode amplifier, in which the output transistor is either *on* or *off*, since it dissipates little power in either condition. A key issue is how to use such amplifiers to replicate the variable envelope signals of most wireless systems. Audio frequency class S amplifiers succeed in achieving this using pulse-width modulated binary input signals. While this approach cannot be used directly in the microwave region because of the high clock frequency involved, we have found that the output of bandpass delta-sigma modulators can be used [5]. The simulated amplifier efficiency is on the order of 70 percent for 850 MHz amplification using GaAs HBTs.



■ **Figure 9.** *A schematic diagram of the LINC architecture.*

Outphasing Power Amplifier Design

The use of outphasing concepts for efficient linear PAs dates back to the 1930s for AM transmission [6], was revived in the 1970's under the rubric of LINC (linear amplification with nonlinear components) [7], and is shown schematically in Fig. 9. It has the theoretical advantage of producing extremely high efficiency and linearity using nonlinear — and hence very efficient — PAs, which are operated constant envelope and out-of-phase in such a manner that the *sum* of their outputs is the desired linear signal. However, the architecture itself is intrinsically sensitive to mismatches in the paths of the two amplifiers, both in-phase and amplitude. In addition, the output



■ **Figure 10.** *Improvement in adjacent channel power with DSP-based predistortion for LINC architecture; a) 5 percent gain and phase mismatch without correction; b) with correction; c) no gain or phase imbalance.*

power of the amplifiers that is not delivered to the antenna is dissipated in the summing port of the hybrid coupler, reducing the potential power-added efficiency [8].

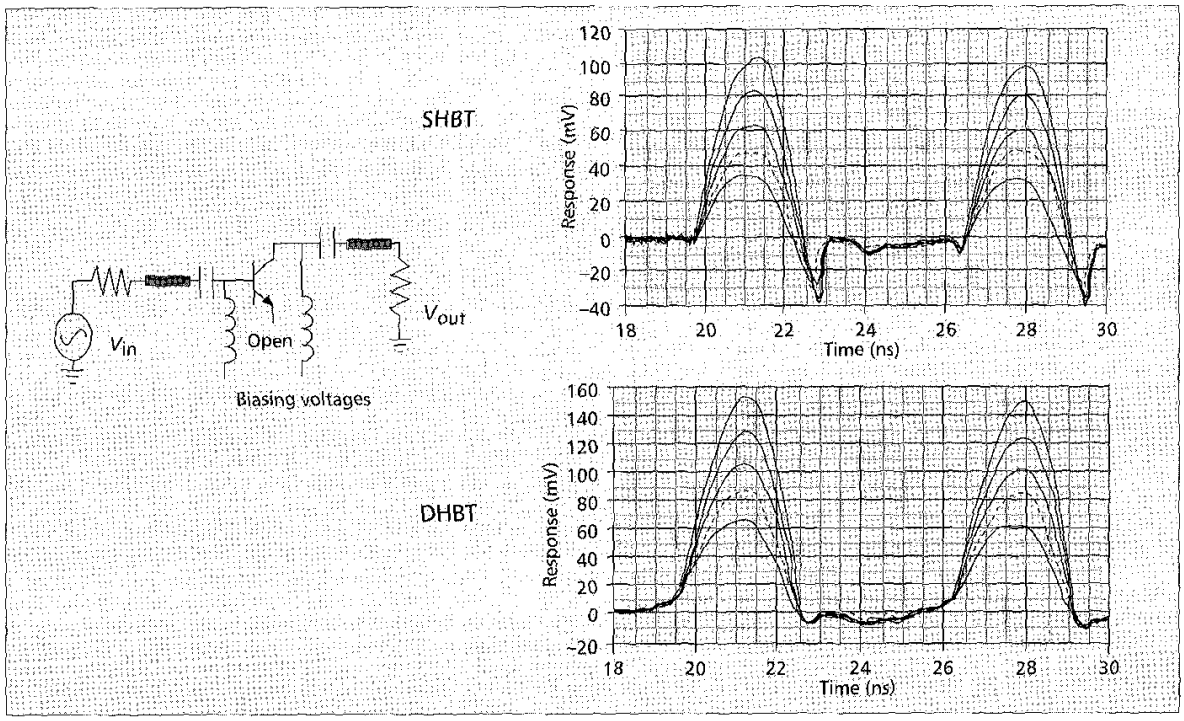
However, some of this wasted power can be recycled back to the battery using a high-speed switching network, with a significant potential improvement in overall system power-added efficiency. The mismatch effects on the linearity of the system can be minimized using sophisticated (DSP) algorithms to pre-distort the signal to reduce the spectral regrowth that results from gain and phase mismatch effects. An example of the improvement that can be achieved in adjacent channel rejection is shown in Fig. 10. Like the bandpass delta-sigma PAs, improvements to the LINC architecture may lead to the simultaneous realization of highly efficient *linear* PAs for handset and base station applications.

Bipolar Transistors with Reduced Saturation Charge Storage

GaAs-based HBTs provide significant advantages of high drive capability and high power density along with high frequency response. If they are operated in the saturation regime, however, such as in a switching mode amplifier, they suffer from charge storage, which dramatically slows their frequency response. We have shown that, with a suitable double heterojunction (DHBT) device, having a wide bandgap collector as well as emitter, this saturation charge storage is suppressed. Figure 11 shows the reverse recovery characteristics of a conventional HBT and those of the new DHBTs, with sinusoidal excitation. The absence of the negative-going current pulse is an indication of higher transistor speed. GaInP DHBTs also have a lower "knee voltage" (Vcesat) than their single heterojunction counterparts. These characteristics make them very attractive for next-generation PAs. With the DHBTs, amplifier design has more freedom to use a very low Vcc regime of transistor operation, including the switching mode. This facilitates implementation of class F, class D and class S amplifiers.

Summary

This article has covered a variety of advances, which individually or together promise to yield dramatic improvements in efficiency and linearity of PAs for RF and wireless applications.



■ **Figure 11.** *Waveforms of reverse recovery of DHBTs and SHBTs showing the absence of saturation charge storage.*

Acknowledgments

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Biographies

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PETER M. ASBECK (M'75) received the B.S. and Ph.D. degrees from the Department of Electrical Engineering, Massachusetts Institute of Technology, Cambridge, in 1969 and 1975, respectively. He was with Sarnoff Research Center, Princeton, No, and Phillips Laboratory, Briarcliff Manor, NY, where he worked in the areas of quantum electronics and GaAlAs/GaAs laser physics and applications. In 1978, he joined Rockwell International Science Center, Thousand Oaks, CA. where he was involved in the development of high-speed devices and circuits based on III-V compounds and heterojunctions. He investigated the influence of GaAs substrates on the behavior of field-effect transistors. He participated in the effort to develop heterojunction bipolar transistors based on GaAlAs/GaAs and InAlAs/InGaAs materials systems, and has contributed in the areas of physics, fabrication, and circuit applications of these devices. In 1991, he joined the University of California at San Diego, La Jolla, as Professor in the Department of Electrical and Computer Engineering. His research interests include the development of high-speed heterojunction transistors and optoelectronic devices.

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ARUN JAYARAMAN was born in Madras, India in 1968. He received his Bachelor's degree in Electronics and Communication Engineering from the Indian Institute of Technology, Madras in 1991. He received his M.S. and Ph.D. degrees in Electrical Engineering from the University of California, San Diego in 1993 and 1997 respectively. His Ph.D. thesis involved the design of RF bandpass delta-sigma ADCs using AlGaAs/GaAs heterojunction-bipolar transistors. From 1995 to 1996 he was employed at Pacific Communication Sciences, Inc. where he was responsible for the design of mixed-signal ASIC blocks including voice-band codecs and Gm-C filters. During 1997 to 1998 he has been employed at the Wireless Communications Division of Rockwell Semiconductor Systems designing RF front-end components including LNAs, mixers and frequency synthesizers. He is currently employed in the Digital Infotainment Division of Conexant Systems Inc., engaged in the design of integrated frequency synthesizers for wideband applications.

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