High-Efficiency Power Amplifier Using Dynamic Power-Supply Voltage for CDMA Applications

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Abstract— Efficiency and linearity of the microwave power amplifier are critical elements for mobile communication systems. This paper discusses improvements in system efficiency that are obtainable when a dc–dc converter is used to convert available battery voltage to an optimal supply voltage for the output RF amplifier. A boost dc–dc converter with an operating frequency of 10 MHz is demonstrated using GaAs heterojunction bipolar transistors. Advantages of 10-MHz switching frequency and associated loss mechanisms are described. For modulation formats with time-varying envelope, such as CDMA, the probability of power usage is described. Gains in power efficiency and battery lifetime are calculated. An envelope detector circuit with a fast feedback loop regulator is discussed. Effects of varying supply voltage with respect to distortion are examined along with methods to increase system linearity.

Index Terms—Dynamic supply RF amplifier, envelope restoration amplifier, 10-MHz dc–dc converter.

I. INTRODUCTION

RF POWER amplifiers used for wireless communications with spectrally efficient modulation formats require high linearity to preserve modulation accuracy and limit spectral regrowth. To minimize distortion, they are typically operated in Class-A or Class-AB mode. Unfortunately, the operation of Class-A or Class-AB RF amplifiers at less than their maximum output power leads to reduced power efficiency. For example, the power efficiency of a Class-A amplifier decreases with output power P_{out} (relative to its peak value $P_{\text{out max}}$) in proportion to $P_{\text{out}}/P_{\text{out max}}$. Similarly, for a Class-B amplifier, the efficiency varies as $(P_{\text{out}}/P_{\text{out max}})^{1/2}$. Class-AB amplifiers have output power variations intermediate between these values. Thus, there is customarily an inherent tradeoff between linearity and efficiency in the amplifier design.

The dual requirements of high linearity and high efficiency have been under intense investigation recently for two reasons. First, the current trend is to operate portable wireless phones at only 3.5 V (corresponding to one Li-ion cell, whose voltage
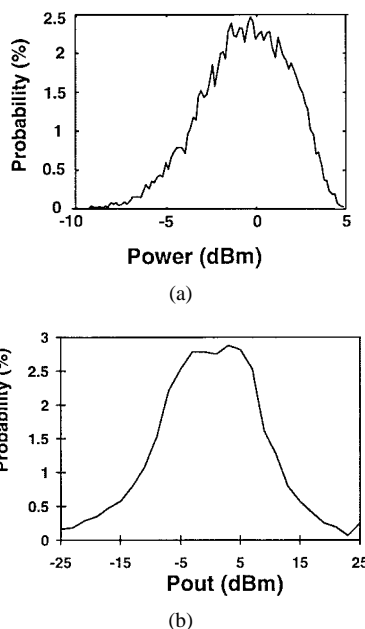
Fig. 1. Power output probability distribution for CDMA modulation under: (a) short time variations and (b) long time variations.

drops to 3.2 V near end of life). Under these circumstances, nonlinearities associated with RF device saturation effects become prominent and efficiency drops. Second, to allow for the required variation of RF signal envelopes with modulation schemes such as QPSK or multicarrier signaling, amplifiers have to operate with large peak-to-average power outputs, usually of 5 dB or greater. Specifications such as IS-95 dictate finite distortion levels, limiting the adjacent channel power ratio (ACPR) measured in a 30-kHz bandwidth at 885 kHz from the center of the CDMA spectrum to be no more than -26 dB relative to the average in-band power measured in the same bandwidth. Fig. 1(a) shows the probability distribution of the RF envelope power for a CDMA reverse link waveform (OQPSK modulation) on a time scale corresponding to the inverse of the modulation bandwidth (of order microseconds).

Variations in output power also occur over a slower time scale for CDMA transmission (as well as for all most other cellular protocols) in order to accommodate variable distance between mobile and base, as well as multipath and shadow fading. In many wireless systems, an active feedback control is used to adjust the RF output from the portable transmitter to limit interference effects and save battery lifetime. Fig. 1(b) shows this slower probability distribution (or power usage
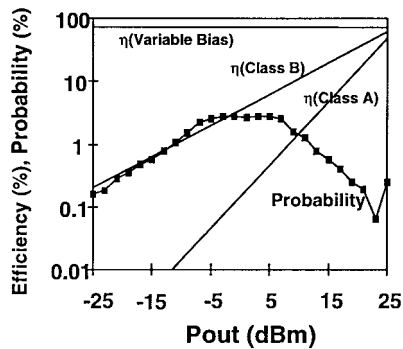
Fig. 2. Variation of efficiency with output power for various amplifier configurations. Also shown is the output power probability distribution for CDMA signals.
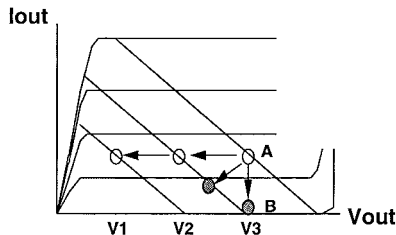

Fig. 3. RF power amplifier transistor current versus voltage characteristics, illustrating representative RF load line and various dc-bias strategies. Point A is the quiescent bias point for Class-A amplifiers and point B for Class-B amplifier. Moving from $V1$ to $V3$ by varying supply voltage yields higher efficiency.

profile) compiled from field tests on CDMA wireless transmission.[1] In Fig. 2, the power usage profile is plotted together with the efficiency versus output power for various amplifier configurations. It is seen that even though the maximum output power capability of the amplifier is approximately 0.5 W, operation at this level occurs only a small fraction of the time. The most probable output power is only 1 mW. At this point, where most of the transmission takes place, a Class-A amplifier has only 0.1% efficiency, while a Class-AB amplifier is typically only 2% efficient.

The variation of efficiency with output power for the amplifiers can be understood by considering the transistor biasing within the power amplifiers. Fig. 3 shows representative output current versus output voltage characteristics for the output transistor. In Class-A amplifiers, the dc current and voltage are kept constant as the output power varies. Consequently, the input dc power is constant, and the efficiency is proportional to RF output power. In the Class-B amplifier, the dc-current bias varies in proportion to the output RF current and, thus, changes according to the square root of output power. The corresponding voltage is kept constant. Another option is to vary the supply voltage in accordance with the output signal level. If both dc voltage and current are varied optimally, then the efficiency of the amplifier can, in principle, be kept high even as the output power decreases (as shown in Fig. 2 for the "variable bias" case). Amplifiers designed to accomplish have been called "envelope tracking" amplifiers.

[1] Cellular Data Group Stage 4 System Performance Tests, San Jose, CA, July 1997.
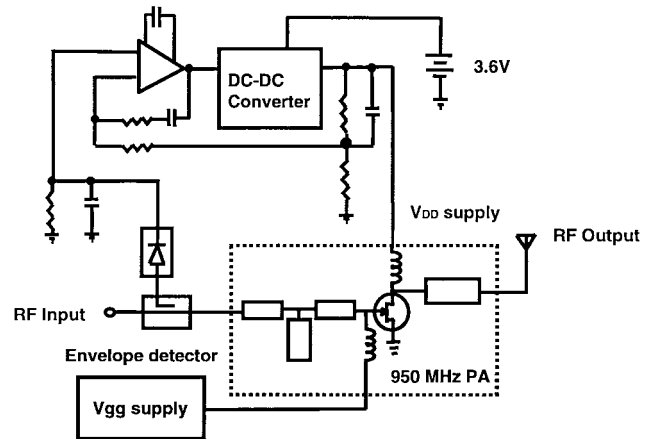

Fig. 4. Schematic diagram of RF amplifier system.

To implement variable voltage bias, Buoli [1] developed a linear regulator power drive, whereby the V_{DD} supplied to a final MESFET amplifier varied with the RF envelope. To save power, this voltage was obtained from a dual source; a minimum voltage of +7 V was fed to the amplifier, which could be overridden by a linearly controlled voltage between 7–12 V, which followed the signal envelope. Although the higher voltage was provided by virtue of a relatively inefficient fast video-type amplifier controlling a linear-pass transistor, the savings in overall system power was up to 45%. Power was saved since, for small signals, the energy source was the 7-V supply (and not the 12-V supply). The dynamic 7–12-V source was used to take care of the peaks required by the modulation format. A related technique for raising the efficiency, due to Raab [2], comprises a Class-S high-level amplitude-modulation scheme, where the modulator takes the form of a step-down buck regulator operating at 200 kHz. The signal input to the RF stage is hard-limited to preserve only the phase information. The envelope of the output signal is controlled by the varying dc supply voltage of the RF stage. This dc voltage is regulated by pulsewidth modulation of the buck regulator. In this system, the maximum frequency of modulation depends strongly on the switching frequency of the buck regulator. Sampling theory requires that this switching frequency be at least twice that of the highest modulation frequency required. In practice, it is usually seen that a factor of ten is required to minimize the effects of filter ripple components. With typical dc–dc converters, the switching frequency (usually below 1 MHz) is not high enough to allow rapid modulation of the supply voltage for many RF amplifier communication purposes.

In this paper, we present a high-efficiency power-amplifier topology for use in a portable microwave communications system. Here, a boost dc–dc converter is used to provide the supply voltage to a MESFET power amplifier. The overall amplifier configuration is shown in Fig. 4. By sensing the RF envelope to be amplified, and providing a dynamically adjusted V_{DD} to the amplifier by means of the dc–dc converter, overall system efficiency may be increased. By using a boost converter operating at 10 MHz, two advantages are obtainable over a step-down approach. First, power amplifiers operate more

efficiently with higher V_{DD} or V_{CC} values due to the finite saturation voltage of the RF amplifier transistor. Secondly, as the input voltage drops, due to battery depletion, the required high-voltage level can still be maintained, even as the battery is running toward exhaustion. If a step-down converter is used, the highest voltage can only be that of the battery itself—limiting the available power output.

The use of a switching frequency of 10 MHz has several benefits as well. First, all filter components may be reduced in value and size. This allows for inductors that contain few turns, thus reducing resistive losses. In addition, capacitors may be simple ceramic surface mount devices, easily located on the power circuit layout. This lends itself to miniaturization of the power converter. A second benefit of higher frequency switching is that the dynamic response of the power supply has greater bandwidth. An operating frequency of 10 MHz allows for less than 1-μs transient response. This is required when attempting to follow a rapidly modulated envelope, as in CDMA modulation. For example, with IS-95 signals, the modulation bandwidth is 1.22 MHz.

To properly gauge the effect of efficiency improvement, it is necessary to account for the probability distribution of power usage as a function of the output power P_{out} [4], [5]. As shown in Fig. 2, the probability density $p(P_{\text{out}})$ of the power usage on a decibel scale is approximately Gaussian [6]. From this, the average input power consumed by the RF amplifier system (from the battery) can be calculated as

$$\langle P_{\text{in}} \rangle = \int_0^{+\infty} p(P_{\text{out}}) P_{\text{in}}(P_{\text{out}}) \, dP_{\text{out}}. \qquad (1)$$

Likewise, one may calculate the average RF output power obtained from the amplifier as

$$\langle P_{\text{out}} \rangle = \int_0^{+\infty} p(P_{\text{out}}) P_{\text{out}} \, dP_{\text{out}}. \qquad (2)$$

The average power-usage efficiency is defined here as

$$\eta_{\text{ave}} = \frac{\langle P_{\text{out}} \rangle}{\langle P_{\text{in}} \rangle}. \qquad (3)$$

This provides a numerical method for comparison of RF power systems, which corresponds directly with battery energy consumption. It implicitly includes the power conversion efficiency of the dc–dc converter.

II. MESFET AMPLIFIER AND ENVELOPE DETECTOR

A GaAs power MESFET amplifier was constructed using hybrid microstrip techniques. The load impedance at the output of the MESFET was adjusted to approximately 50 Ω. With a maximum drain voltage peak-to-peak swing of 20 V, an output power of 1 W at 950 MHz could be obtained under continuous wave (CW) excitation. To achieve this, and stay within the specifications of IS-95, a maximum power-supply voltage V_{DD} of 10 V was required. In addition, to increase the linearity of the amplifier, a dynamically adjusted gate voltage V_{GG} was employed, which lowered the amplifier gain at higher power output. An envelope detector was constructed using an on-board directional coupler, which was terminated in a
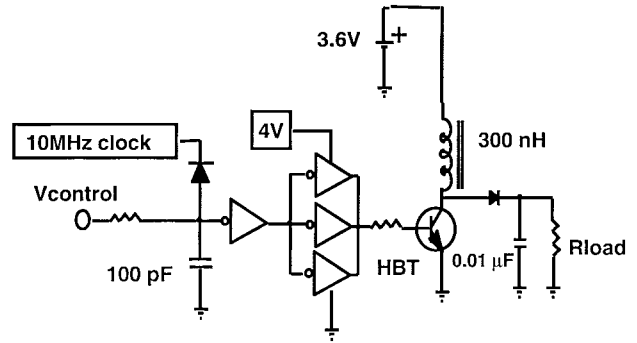

Fig. 5.   Schematic diagram of boost converter with driver.

microwave diode. The output voltage of this detector followed the incoming RF envelope and yielded 2 V at full input power (15 dBm).

III. DC–DC BOOST CONVERTER

The boost or ringing-choke converter used is schematically shown in Fig. 5. Here, energy is stored in a magnetic field during the on-time of the switch. During the off-time, this energy is released and used to charge the output capacitor to the peak of the ring voltage and provide energy to the load. With the condition that the *maximum* ON time is 50% of the switching period, and that the operation of this converter is in the *discontinuous* mode, the maximum inductor value that can be used for energy storage is

$$L_{\text{max}} \approx V_{\text{in}}^2 / 8 f P_{\text{out}}. \qquad (4)$$

Larger values limit the peak current and energy. This assumes a linear current ramp during the ON time and a rapid decreasing ramp in the OFF time. Here, f is the operating frequency and P_{out} is the maximum output power of the converter. It can be seen that by increasing the operating frequency, the value of inductance can be reduced. Moreover, the inductor value varies as the square of the input battery voltage. For single-cell operation, power output of 1 W, and operating at 10 MHz, inductor values may be as small as tens of nanohenries. Boost converters have a pole in their output transfer function, which limits dynamic response and is dependent on the value of the energy-storage output capacitor and the load resistance

$$f_{\text{dynamic}} = 1/(2\pi R_{\text{out}} C_{\text{out}}). \qquad (5)$$

By raising the switching frequency, the output capacitance may be reduced for a fixed-output ripple magnitude, increasing the composite amplifier bandwidth.

The power switch is the heart of the dc–dc converter. In this study, AlGaAs/GaAs heterojunction bipolar transistors (HBT's) were used due to their ability to provide extremely fast switching at moderate power. The slowest transistors used had f_t greater than 1 GHz [7] and could switch 1 A with a fall time of less than 2–4 ns.

Boost regulators of this topology have efficiency largely limited by the voltage drops across their semiconducting elements. Power losses include several components: $P_{\text{dc loss}}$ associated with voltage drops in the semiconductor devices and

inductor, $P_{\text{ac loss}}$ associated with dynamic power dissipated in the switch during on-off transitions, and $P_{\text{drive loss}}$ associated with the drive circuits.

In summary, we have

$$P_{\text{loss}} = P_{\text{dc loss}} + P_{\text{ac loss}} + P_{\text{drive loss}}. \qquad (6)$$

The largest contributor to $P_{\text{dc loss}}$ (and the only one considered here) is the HBT switch. In the devices used, $V_{\text{CE}_{\text{sat}}}$ was nearly 0.8 V (a substantial portion of the incoming battery potential). If I_{peak} represents the peak of the current ramp (nearly 1.4 A), and $t_{\text{on HBT}}$ the conduction time of the power switch (50% maximum), this loss is

$$P_{\text{dc loss}} = V_{\text{CE}_{\text{sat}}} I_{\text{peak}} t_{\text{on HBT}} f/4. \qquad (7)$$

Values of $P_{\text{dc loss}}$ of 0.28 W were observed for 1-W output power. DC losses due to the inductor and conductor resistance were not considered in the analysis due to the relatively large conductors used. There are two main contributors to the ac switching loss. First, the ac switching loss in the transistor is the result of current still flowing through the collector as the transistor is turning off and V_{CE} is rising above $V_{\text{CE}_{\text{sat}}}$. Defining V_{peak} as the ring-up collector voltage peak, the transistor ac loss $P_{\text{ac loss}}$ may be computed approximately by [8]

$$P_{\text{ac loss}} = V_{\text{peak}} I_{\text{peak}} t_{\text{fall HBT}} f/6. \qquad (8)$$

In many conventional lower frequency power-supply designs, the ac transistor loss is comparable to the dc loss. With HBT power transistors, the ac loss is very small due to the fast rise and fall time. The maximum turn-off time associated with the AlGaAs HBT $t_{(\text{fall HBT})}$ was estimated by oscilloscope measurements to be less than 3 ns, at a current peak of $I_{\text{peak}} = 1.4$ A. There is additional ac loss due to the charging and discharging of the Schottky rectifier capacitance and other stray capacitances located on the printed circuit board. Assuming that this total electrostatic energy is wasted every cycle, we find a loss $P_{\text{capacitance loss}}$ of

$$P_{\text{capacitance loss}} = CV_{\text{peak}}^2 f. \qquad (9)$$

Other sources of inefficiency stem from power consumed in the driver circuitry. The power HBT driver stage was required to provide over 35-mA input current to the drive switch due to its rather low current gain ($\beta \approx 45$). With a driver voltage supply V_{drive} of 4 V, the power consumed is

$$P_{\text{drive loss}} = V_{\text{drive}} I_{\text{peak}} t_{\text{on HBT}} f/\beta \qquad (10)$$

or approximately 60 mW at full duty cycle.

The measured efficiency of the dc–dc converter was found to be in the range of 65%–74% for output powers in the range of 0.2–1 W.

IV. TOTAL SYSTEM AND FEEDBACK LOOP

A one-pole filter with characteristic frequency of 1 MHz was used to provide a reference signal into an operational amplifier (LM301) that regulated the boost converter. By adjusting the feedback, the regulator provided the optimum voltage to the
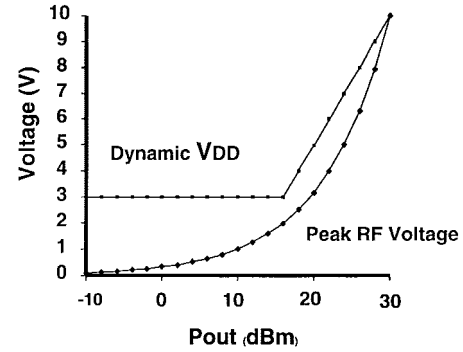

Fig. 6. Dynamic supply voltage and V_{peak} swing of drain waveform versus P_{out}.

RF amplifier. The correspondence between dc–dc converter output (V_{DD} supply) and RF power out is shown in Fig. 6. Also included is the peak swing of the drain voltage of the RF device. The amplifier was tuned so that 1-W CW output was obtained with an input voltage of $10V_{\text{DC}}$. The slope of the V_{DD} versus P_{out} curve was set so that the ACPR level was satisfied across the range of operation. The minimum output voltage from the converter was 3.0 V (battery voltage minus the Schottky diode drop), which was produced when the pulsewidth was reduced to zero.

The drive circuitry, shown in Fig. 5, is a complete pulsewidth-modulated converter. A clock operating at 10 MHz and 50/50 duty cycle generates the frequency reference pulses by which the boost regulator is synchronized. To obtain the required base drive pulse, a high-speed CMOS digital inverter IC (MC74AC04N) was used. One inverter is used as a voltage comparator, while three others form the base drive to the main switching transistor. One feature of this circuit is that as the control voltage is raised, the time to achieve activation of the inverter is shortened, thereby increasing the ON time of the power switch. The clock output "low" truncates the drive pulse.

The base is driven through a 50-Ω limiting resistor with a diode shunt across to provide charge removal during the falling edge of the drive pulse. To improve speed and raise system efficiency, the inverter was run from a 4-V source. This can be derived as a bootstrapped supply via a tap off the boost inductor. The entire apparatus was constructed on a simple G-10 backside-grounded printed circuit board. Not included in the block diagram of Fig. 4 is the operational amplifier circuitry used to provide the varying V_{GG}. A simple summing amplifier was used, which converted the positive-going envelope detector waveforms to a negative voltage, which varied from -2.1 to -2.4 V as the V_{DD} voltage varied from 3 to 10 V. This reduction of gain as a function of V_{DD} voltage improved system linearity and limited distortion over the full range of the amplifier [9], [10]. The measured RF gain is shown in Fig. 7.

Efficiency tests were made on the complete RF system. Fig. 8 compares the dc power efficiency between an amplifier with constant V_{DD} supply voltage (10 V) and one with dynamic V_{DD} and V_{GG} voltages. From (3), the long-term
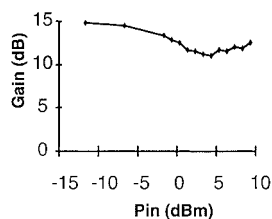
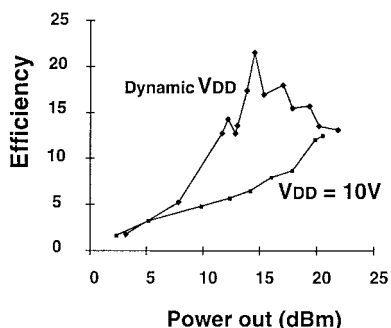Fig. 7. Measured RF gain of the system versus P_{out} for sinusoidal signals.

Fig. 8. Measured efficiency versus output power for dynamic supply amplifier and for a comparable amplifier with fixed V_{DD}.

power usage efficiency is calculated to be

$$\eta = 3.89\% \quad (V_{DD} = 10 \text{ V})$$
$$\eta = 6.38\% \quad (V_{DD} = \text{Dynamic}).$$

The results correspond to an increase in power usage efficiency of a factor of $1.64\times$. A battery powering this amplifier would last 64% longer when used in conjunction with the dc–dc converter scheme. Other probability of use distributions may yield different average efficiencies and different efficiency gains from the use of the dc–dc converter.

V. SYSTEM BANDWIDTH AND LINEARITY

To avoid loss of modulation efficiency and spectral regrowth, the amplifier must exhibit adequate linearity. A requirement for linearity is that the V_{DD} supplied to the RF amplifier is in-phase with the envelope and of sufficient magnitude to prevent clipping. To achieve this, a fast loop response in the dc–dc control section is mandatory. The dynamic response of the dc–dc converter for a step change in control voltage is shown in Fig. 9. From this, it is evident that modulation up to 1 MHz is possible for moderate-output level changes. The rise time for this output voltage change is noticeably shorter than the fall time, consistent with the fact that the only sink mechanism for the output is due to the output load discharging the filter capacitor. Since the rise time of the step change depends on the energy storage in the inductor, it is not sensitive to output load values unless its maximum power capability is exceeded. In addition, as far as linearity is concerned, overshoots in V_{DD} voltage are acceptable at the expense of power dissipation.

A frequency-domain view of the amplified CDMA waveform is shown in Fig. 10. This output was recorded using a standardized resolution bandwidth of 30 kHz, consistent with specifications for IS-95. This waveform shows an ACPR of
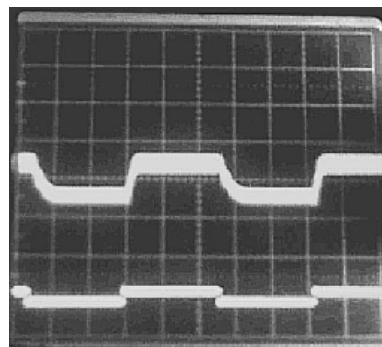

Fig. 9. Measured dynamic response of dc–dc converter Top trace: V_{out} 2 V/cm. Bottom trace: $V_{control}$. Horizontal: 1 μS/cm.
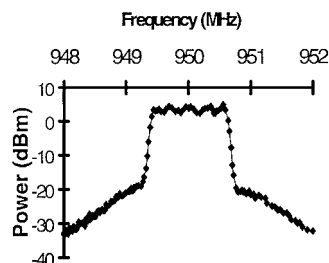

Fig. 10. Measured output spectrum with CDMA input signal at maximum power.

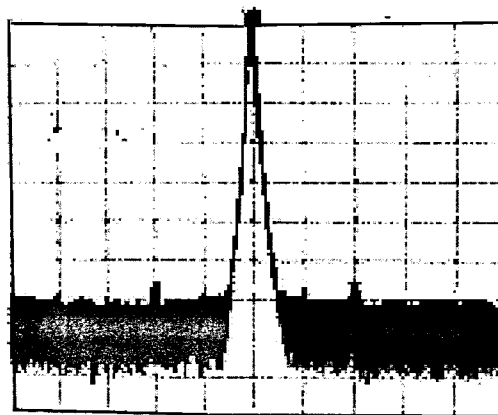Fig. 11. RF output spectrum with sinusoidal input showing sidebands caused by 10-MHz ripple on V_{DD}. Vertical: 10 dBm/cm. Horizontal: 1 μS/cm.

greater than 26 dB. One potential concern involved the ripple output of the 10-MHz converter. In order to increase response time, the output capacitor was reduced in size, which, in turn, increases the output ripple. It was found that very little conversion of V_{DD} amplitude to RF gain variation resulted. This is shown in Fig. 11 where CW spectrum is displayed along with the 10-MHz created sidebands. Each spur is less than -60 dBc.

VI. SUMMARY

A highly efficient microwave power amplifier was implemented using a GaAs MESFET amplifier and dc–dc boost converter. By dynamically controlling the supply voltages, an efficiency increase of over $1.64\times$ was achieved compared

with a constant voltage system. DC–DC converter switching operation at 10 MHz allowed wide-bandwidth and small-sized components. By utilizing a fast feedback loop regulation scheme and dynamic gate bias, the ability to meet CDMA IS-95 specifications for ACPR was realized.

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Pin-Fan Chen (S'93), for photograph and biography, see this issue, p. 1437.

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Lawrence E. Larson (S'82-M'82-SM'90), for photograph and biography, see this issue, p. 1403.