SiGe Profile Design Tradeoffs for RF Circuit Applications

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Abstract— **We present the first experimental results for new SiGe profile designs which were developed explicitly for improving minimum noise figure (NF_{min}) without sacrificing gain, linearity, frequency response, or the stability of the SiGe strained layer. A measured NF_{min} of 0.2dB at 2.0GHz with an associated gain (G_{assoc}) of 13dB at noise matching, and a linearity efficiency ($OIP3/P_{DC}$) of 10 were obtained for the best low-noise profile, all of which represent substantial improvements in RF performance over the Si BJT and control SiGe HBT design point, and were accomplished without sacrificing SiGe film stability. The fundamental SiGe profile design tradeoffs associated with emerging SiGe RF circuit applications are discussed.**

I. Introduction

RF applications generally impose more serious device design constraints than digital applications. SiGe HBT technology, because it has higher intrinsic performance than Si BJT technology at similar process complexity, and delivers better cost-performance than GaAs technology, has recently emerged as a contender for the RF market. Existing SiGe profile design points are only optimized for high f_T and f_{max} at high current densities [1]. RF transceiver building blocks such as LNA's and mixers, however, often require very low broad band noise, high RF gain, and excellent RF linearity, thus complicating the device design. The fundamental question we address in this paper is the following: given a constraint of maintaining constant film stability, at a given technology generation (i.e., fixed geometry and doping), what is the optimum Ge profile shape that minimizes NF_{min} without sacrificing gain, linearity, or frequency response? To most efficiently attack the problem, we began with extensive 2-D device simulations using MEDICI [2]. These simulations used 2-D models of the SiGe control profile based on the device layout and measured SIMS, which were carefully calibrated to data for not only β, f_T, and f_{max}, but also the Y-parameters, NF_{min}, and G_{assoc}. A new approach [3] [4] for generating all of the noise parameters (NF_{min}, Y_{opt}, R_n) as well as G_{assoc} from simulated (or measured) Y-parameters was developed for this purpose, and gives excellent agreement with measured noise data.

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II. SiGe Profile Design Tradeoffs

To realize high f_T and f_{max} at high J_C as required by high-speed digital applications, the Ge profile needs to be extended into the neutral collector to minimize the f_T roll-off at high J_C due to the high-injection heterojunction barrier effect [5]. LNA's in RF transceivers, however, typically operate at relatively low J_C where NF_{min} is minimized (as much as 10x lower in J_C). From the theory of linear noisy two-port networks, NF_{min} is fundamentally determined by the equivalent input current and voltage noise sources [4]:

$$< i_n^2 >= 2qI_B + \frac{2qI_C}{|h_{21}|^2} \quad (1)$$

and

$$< v_n^2 >= 4kTR_B + \frac{2qI_C}{|y_{21}|^2} \quad (2)$$

where y_{21} and h_{21} are the AC transconductance and AC current gain at the frequency of interest, respectively. For a given technology generation (transistor geometries and constant doping), the base resistance R_B and y_{21} at a given J_C are fixed, thus fixing $< v_n^2 >$. $< i_n^2 >$, however, can be reduced by increasing β (to reduce I_B) and increasing f_T (to increase h_{21}). Consequently NF_{min} can be reduced. A high f_T at low J_C and particularly a high β at low J_C are therefore critical in reducing NF_{min} for constant base doping and transistor geometry. From our simulations, we found that for constant film stability (integrated Ge dose), a significant improvement in NF_{min} over the SiGe control profile can only be realized in practice by pushing the edge of the Ge retrograde in the collector significantly closer to the EB junction (surface), and then using the additional Ge to increase the band offset at the EB junction (for higher

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β) and increase the Ge grading (for higher f_T) [6]. We are thus forced to trade high-J_C performance for improved NF_{min}. Two such low-noise Ge profiles (LN1 and LN2) which maintain the stability of the SiGe control profile but have significantly lower NF_{min} in simulation (by 0.2dB) are shown in Fig. 1. All of the SiGe profiles are unconditionally stable to defects generation, as shown in Fig. 2. The two low noise profiles have f_{max} values comparable to the SiGe control in simulation. The excellent linearity of the Si BJT and SiGe control devices are expected to be retained in the two low noise profiles, because the linearity is primarily determined by the EB and CB depletion capacitances, and insensitive to the diffusion capacitance (base transit time) in this technology [7].

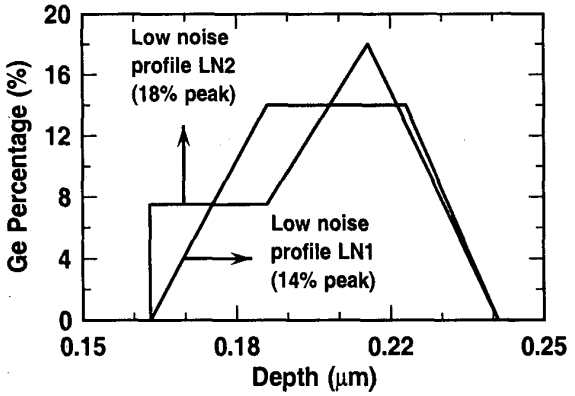

Fig. 1. Schematic of the two low noise profiles designed that are both unconditionally stable.

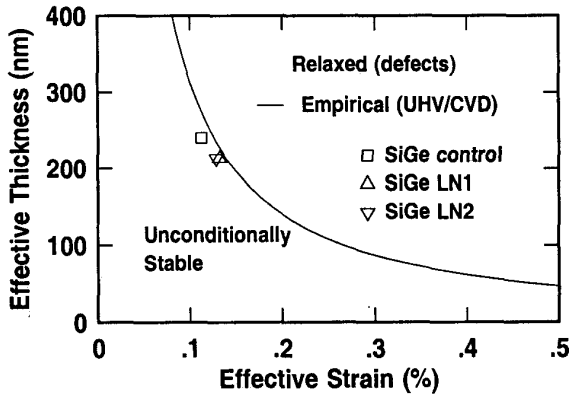

Fig. 2. Stability of the SiGe control design point and the two low noise profiles. All of these profiles are unconditionally stable.

III. Experimental Results

For unambiguous comparisons all four profiles were fabricated in the same wafer lot in a state-of-the-art 0.50μm SiGe HBT technology [1] using UHV/CVD growth and identical processing conditions. DC charactersitics were measured using an HP4155, and S-parameters were measured using a HP8510C network analyer from 2 - 40GHz, from which f_T and f_{max} were extracted. The noise parameters were measured from 2 - 18GHz using an NP-5 on-wafer measurement system from ATN Microwave Inc., and two-tone load-pull measurements were made at 1.9GHz with 1MHz tone spacing.

TABLE I
Summary of Device Electrical Characteristics

Performance	Si BJT	SiGe control	SiGe LN1	SiGe LN2
β at V_{BE}=0.7V	67	114	350	261
V_A(V)	19	60	58	113
$BV_{CEO}(V)$	3.5	3.2	2.7	2.7
R_{Bi} ($k\Omega/\square$)	12.8	9.8	10.3	10.7
peak f_T (GHz)	38	52	52	57
peak f_{max} (GHz)	57	64	62	67

Table I summarizes the measured transistor parameters of the four fabricated profiles. The penalty in BV_{CEO} over the SiGe control for LN1 and LN2 is due to the higher β, and should not impact LNA designs, which see finite source impedance (i.e., not an 'open'). The measured $\beta_{DC} - I_C$ and $f_T - I_C$ curves of a 20μm^2 (0.5x20x2 stripe) unit cell device are shown in Figs. 3-4, and bear-out the expected high injection design trade-off. The two low noise profiles, LN1 and LN2, have a higher β_{DC} and f_T at low J_C, but the SiGe control and Si BJT devices have a weaker (better) f_T roll-off at high J_C, as designed. This design tradeoff translates into a significant improvement of the NF_{min} across the range of J_C of interest to LNA and mixer circuits over the Si BJT and SiGe control profiles, as shown by the measured NF_{min} data in Fig. 5 . The LN1 profile achieves an impressive NF_{min} of 0.2dB at 2mA, 0.2dB lower than the SiGe control profile. The measured delta's between profiles are consistent with our simulations. The associated gain at noise matching is still above 13dB at NF_{min} for all of the profiles (Fig. 6), and the two low noise profiles have f_{max} comparable to the SiGe control (Fig. 7).

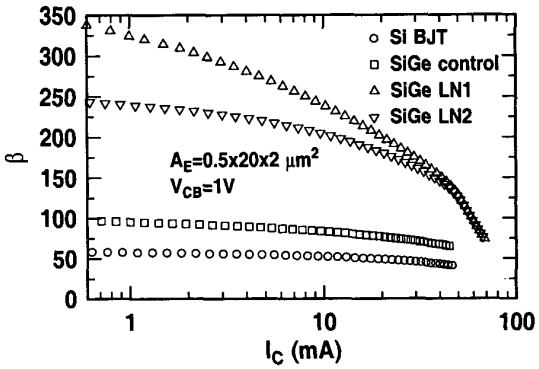

Fig. 3. Measured dc current gain versus collector current of the fabricated Si BJT, SiGe control, and the SiGe low noise profiles.

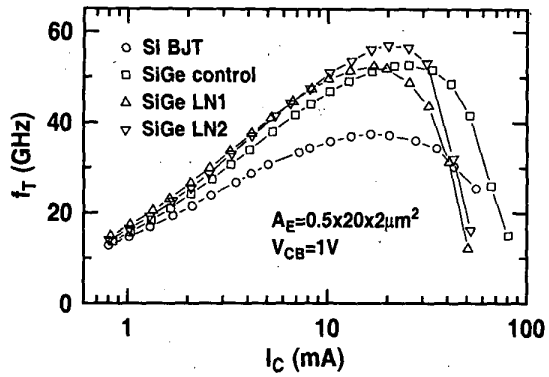

Fig. 4. Measured f_T versus collector current of the fabricated Si BJT, SiGe control, and the SiGe low noise profiles.

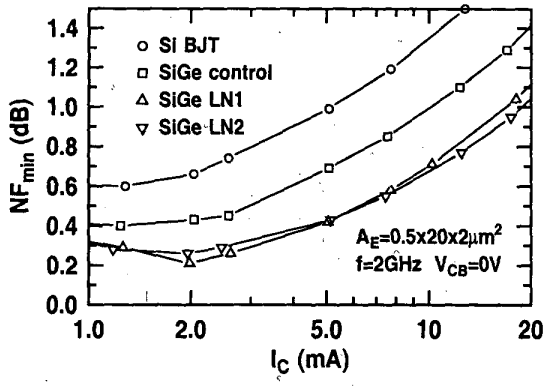

Fig. 5. Measured minimum noise figure (NF_{min}) versus collector current at 2GHz for the fabricated Si BJT, SiGe control, and the SiGe low noise profiles.

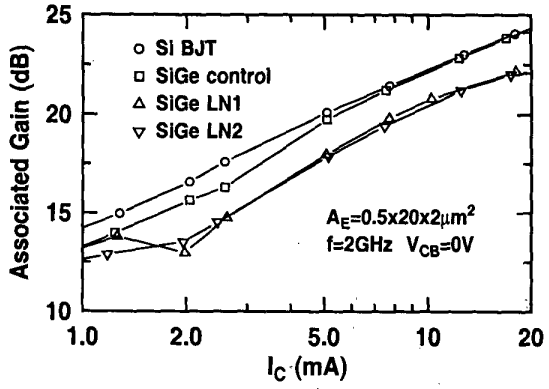

Fig. 6. Measured associated gain versus collector current at 2GHz for the fabricated Si BJT, SiGe control, and the SiGe low noise profiles.

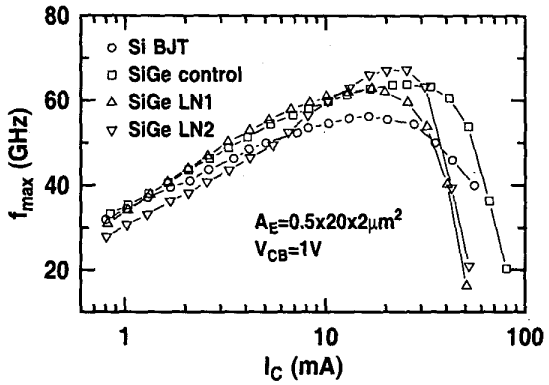

Fig. 7. Measured f_{max} versus collector current at 2GHz for the fabricated Si BJT, SiGe control, and the SiGe low noise profiles.

Two-tone load-pull measurements were performed at 1.9GHz with 1.0MHz tone spacing on the $20\mu m^2$ (0.5x20x2 stripe) unit cell device to determine the linearity. The input 3rd order intermodulation intercept point (IIP3) for a two-tone input is used as a figure-of-merit, and was extracted in the low input power region where the 3rd order intermodulation slope is 3:1. The measured IIP3 is affected by the source and load termination, and thus load-pull data sheds light on the variation of linearity with impedance for each profile. Figs. 8-9 and 10-11 show the measured IIP3 and power gain contours on the load impedance Smith chart for the SiGe control device, and the low noise profile LN1, respectively. The maximum IIP3 achieved is 3dBm (SiGe control) and 3dBm (LN1), with the maximum gain of 17dB (SiGe control) and 20dB (LN1), at 1.9GHz for I_C=3mA and V_{CE}=3V. An excellent linearity efficiency (defined as OIP3/P_{DC} to account for the differing load states at maximum gain and maximum IIP3) of 7 and 10 is achieved for the SiGe control and the low noise SiGe profile LN1, respectively, and is comparable to GaAs HEMT (10) and GaAs HBT technology (11) [8]. Preliminary measurements on RF harmonic mixers fabricated with the identical low noise profiles (LN1 and LN2) also show improved noise and linearity over the SiGe control profile, indicating that these device improvements translate to the circuit level.

IV. Conclusions

The fundamental SiGe profile design tradeoffs for RF circuit applications have been addressed. A higher DC current gain and a higher f_T at low J_C are shown to be critically important for reducing NF_{min} for a given transistor geometry and doping. By applying careful SiGe profile optimization, significant improvement in RF performance can be achieved. Using a newly developed simulation approach, new SiGe profiles were designed explicitly for improving minimum noise figure (NF_{min}) without sacrificing gain, linearity, frequency response, or the stability of the SiGe strained layer. A measured NF_{min} of 0.2dB at 2.0GHz with an associated gain (G_{assoc}) of 13dB at noise matching, and a linearity efficiency ($OIP3/P_{DC}$) of 10 were obtained for the best low-noise profile, all of which represent substantial improvements in RF performance over the Si BJT and control SiGe HBT design point, and were accomplished without sacrificing SiGe film stability.

V. Acknowledgments

The wafers were fabricated at IBM Microelectronics, Essex Junction, VT. We would like to thank D. Ahlgren and B. Meyerson for their contributions to this work.

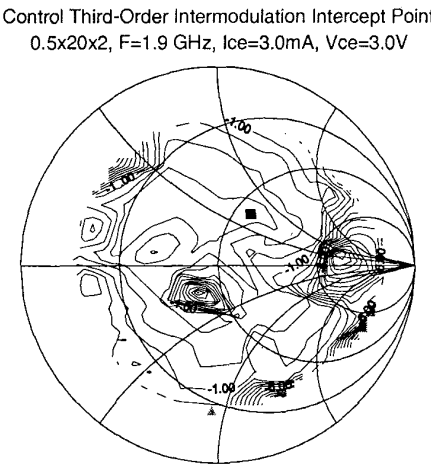

Fig. 8. Measured IIP3 contour on the load impedance Smith chart for the SiGe control device.

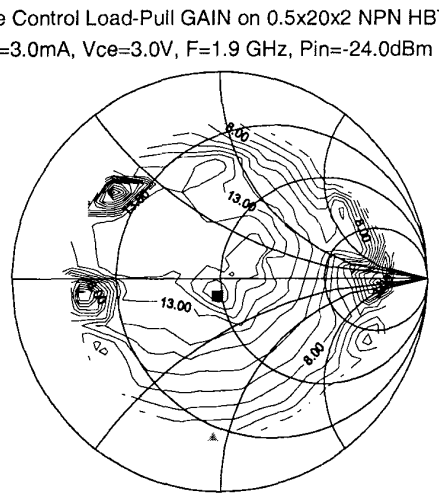

Fig. 9. Measured power gain contour on the load impedance Smith chart for the SiGe control device.

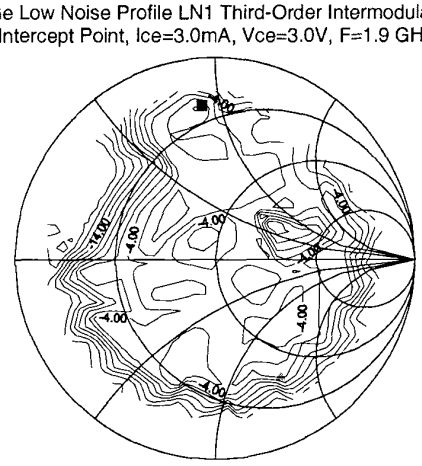

Fig. 10. Measured IIP3 contour on the load impedance Smith chart for the low noise profile device LN1.

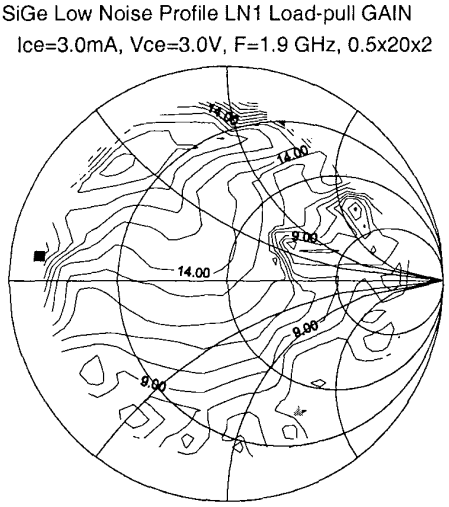

Fig. 11. Measured power gain contour on the load impedance Smith chart for the low noise profile device LN1.

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