A Si/SiGe HBT Timing Generator IC for High-Bandwidth Impulse Radio Applications

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Abstract

A precise timing generator is presented which forms the heart of a wideband impulse radio or radar system. The circuit is implemented in a 45 GHz Si/SiGe HBT technology, and can produce a pulse inside a 100 ns window with an accuracy of 2 ps and a jitter of less than 10 ps. The integrated circuit contains a mixture of analog, digital, and RF functions, consumes 0.5 W, and operates at a clock rate of up to 2.5 GHz.

Introduction

The traditional use of sinusoidal carriers for wide-bandwidth wireless communications applications suffers from many problems including extreme sensitivity to multi-path propagation effects and time dependent fading [1]. One solution to this problem is to employ a completely different modulation scheme - consisting of very narrow impulses - that spreads the carrier over an extremely broad bandwidth. These so-called impulse radios utilize randomization of the resulting pulse positions in time to "spread" the carrier over a wide bandwidth. Advancing or retarding the pulses in time modulates the resulting signal with information. Spreading the carrier over a sufficiently wide bandwidth allows the radio to adhere to FCC Type 15 regulations. A comparison between a traditional wireless communications system and an impulse radio system is shown in Fig. 1. There are many theoretical and practical advantages to this technique including insensitivity to muti-path effects and high coding gain [2].

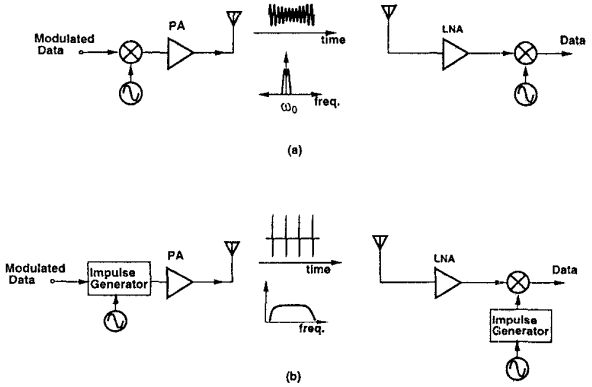

Figure 1: Comparison of (a) traditional narrowband radio architecture and (b) wideband impulse radio architecture.

Successful implementation of such a radio requires the precise generation of very narrow pulses with low jitter. Jitter in the time delay of the transmitted pulses is modeled as an additive white Gaussian noise process in the receiver, and decreases the received signal-to-noise ratio [2]. However, until now, there was no low-cost technique to generate the precision pulse trains required to take full advantage of the technique. Existing impulse radios utilize a hybrid approach to realize the fine timing required [3]. These devices require a high dc power - typically in excess of 5 W - and exhibit poor reproducibility and jitter. This new device acts as a programmable time delay generator specifically tailored for producing extremely stable, low-jitter pulses for an impulse radio application.

Impulse Radio Design

Impulse radio transmitters emit ultra-short Gaussian monocycles with tightly controlled pulse-to-pulse intervals. Typical pulse widths are between 0.20 and 1.50 nanoseconds and pulse-to-pulse intervals are between 25 ns and 1000 ns. In this particular case, the mean pulse interval is 100 ns. These short monocycles are inherently ultra-wideband. Hence, the system is intrinsically insensitive to narrowband jamming and interference. The system uses pulse position modulation; the pulse-to-pulse interval is varied on a pulse-by-pulse basis in accordance with an information signal and a channel code. The receiver directly converts the received RF signal into a baseband digital or analog output signal. A front-end cross correlator coherently converts the electromagnetic pulse train to a baseband signal in one stage. A typical impulse radio is shown in Figure 2. Since there is no intermediate frequency stage, the system complexity is reduced. A single bit of information is generally spread over multiple monocycles. The receiver coherently sums the proper number of pulses to recover the transmitted information.

By shifting each monocycle's actual transmission time over a large time frame in accordance with a code, one can channelize pulse trains. Pseudo-random noise codes (PN codes) are used for this purpose. For multiple access, each user has a pseudo-random noise code sequence. Only a receiver operating with the same pseudo-random noise code sequence can decode the transmission. In the

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frequency domain, this pseudo-random time modulation makes the signal appear very "noise-like".

Besides channelization and energy smoothing, the pseudo-random time modulation also makes a time modulated radio highly resistant to jamming. This is critical as all other signals within the band occupied by a time modulated signal act as jammers to the time modulated radio. Since there are no unallocated bands available above 1 GHz for time-modulated systems, radios will have other signals (interfers) within their operating band. A radio's resistance to these interferers is related to its processing gain, and time modulated radios have enormous processing gain. An impulse system transmitting the 8 kHz information bandwidth with a 2 GHz channel bandwidth has a processing gain of 250,000 or 54 dB.

Rayleigh, or multipath fading, is less of a problem for time modulated systems compared to frequency modulated systems. The only way for significant multi-path problems to exist is if the path length traveled by the interfering pulse is less than the product of the pulse width and the speed of light - roughly one-foot in this case.

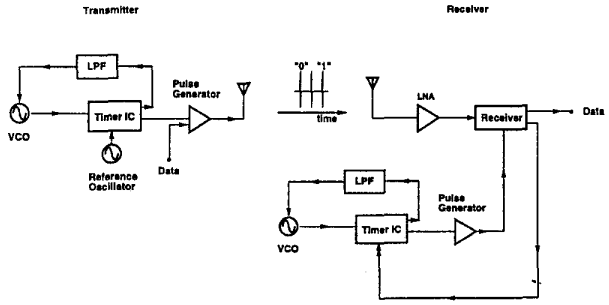

Figure 2. Typical impulse radio configuration

Circuit Design

A simplified block diagram of the complete circuit is shown in Fig. 3. It consists of a set of high-speed presettable counters and comparators, which produce an output pulse at a time interval determined by the pseudo-random input word. The clock input is phase-locked to an external reference at 10 MHz through an on-chip phase-frequency detector. A 16-bit control word results in 1.52 ps impulse positioning accuracy with a 2 GHz clock. The logic blocks were implemented using standard CML design techniques. The high-speed Si/SiGe HBT technology allows the circuit to operate in excess of 2 GHz while consuming approximately 200 μA per gate. The pulse output buffer is implemented by a 50Ω doubly terminated differential pair in order to minimize reflections at the board level. In addition, the use of synchronous logic throughout minimized the accumulated jitter of multiple series logic gates at critical nodes in the circuit.

The critical analog circuit design portion of the chip was the fine delay generator which was implemented by a vector modulator with external I/Q control and a low hysteresis comparator. Linearity of the delay tuning requires sinusoidal inputs to the polyphase filter with low harmonic content. On-chip passive filtering was required to remove the harmonics from the square wave output of the coarse delay pulse. The harmonic content was reduced to less than 40 dB below the fundamental by the use of these filters.

A quadrature vector modulator forms the basis of the fine timing generator. It consists of an I/Q polyphase filter, phase splitter [4], precision four-quadrant multiplier/summer, and low hysteresis comparator. A diagram of the modulator is shown in Figure 4. The fine delay jitter was reduced by minimizing the noise contribution of each device in the chain and maximizing the speed of all the key blocks. The accuracy of the delay generator was improved by pre-filtering the clock prior to the polyphase filter to minimize the error due to the harmonics of the clock signal [5]. The error in the zero-crossings can be estimated by

$$\Delta T \approx \frac{\sum_{n=1}^{\infty} a_n \theta_n(t)}{\sum_{n=1}^{\infty} a_n n \omega_t} \qquad (1)$$

where, a_n is the amplitude of the n^{th} harmonic and $\theta_n(t)$ is the phase deviation.

The output of the polyphase filters was fed to a high-linearity multiplying/summing network, which performed the quadrature scaling and summing and is shown in Fig. 5. Temperature compensated current references were used throughout the design in order to minimize gain variations with temperature which would translate directly into timing drift in this implementation.

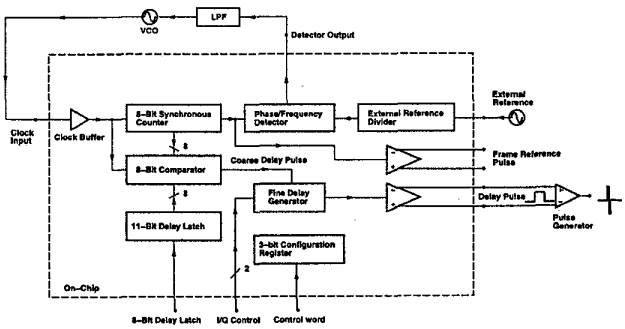

Figure 3. Simplified block diagram of high-speed Si/SiGe HBT timing generator IC.

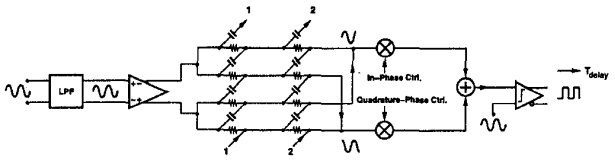

Figure 4. Quadrature vector modulator schematic diagram.

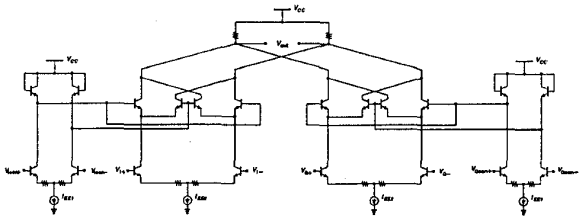

Figure 5. Simplified multiply/summing schematic for vector modulation.

Experimental Results

The circuit was fabricated in the IBM 0.5μm Si/SiGe HBT technology, with HBT f_T and F_{MAX} in excess of 45 GHz. The process also includes high value MIM capacitors, 0.4μm PMOS devices, and polysilicon resistors [6]. In order to achieve the best possible performance at the board level the device was "flip-chip" mounted onto an FR4 board using the IBM "C4" process, where the average bump inductance is approximately 50 pH. The 1500 device IC operated from a 5V supply, and dissipated approximately 0.5W when operating at full speed.

The timer IC was tested at the system level configured as a "radar," with one timer at the transmitter and one timer at the receiver, as shown in Fig. 2. An external digital interface modulated the time intervals in a pseudo-random fashion, and the overall *system* jitter was measured with a Hewlett Packard 5472OA/54721A to be approximately 20 ps. The total system jitter can be expressed as

$$J_{system}^2 = J_1^2 + J_2^2 + J_3^2 + J_4^2 + J_5^2 + J_6^2 + J_7^2 \qquad (2)$$

where,

- J_1 is the jitter associated with the transmit clock
- J_2 is the jitter associated with the transmitter timer IC
- J_3 is the jitter associated with the transmitter pulse generator
- J_4 is the jitter associated with the receiver clock
- J_5 is the jitter associated with receiver timer IC
- J_6 is the jitter associated with receiver pulse generator
- J_7 is the jitter associated with downconversion mixer

The delay as a function of input word, as well as the jitter associated with the timer IC itself, were measured - also with a Hewlett Packard 5472OA/54721A - and the jitter was determined to be less than 8 ps, which is close to the fundamental limit of the sampling head of the oscilloscope. All of these measurements were made by averaging digitized data from one thousand pulses in the test set-up, along with the built-in oscilloscope histogram function.

The coarse delay control utilizes a digital technique, but the fine delay generator employs analog control for precise positioning of the output pulse. The absolute accuracy and linearity of the actual output delay as a function of the input delay control word is not crucial, since these errors can be calibrated out during system initialization.

However, minimizing the variation of the delay over *temperature* is essential, since these errors cannot be calibrated out in a straightforward manner. Fig. 6 plots the variation of the output pulse delay from two delay generators as the temperature is varied from 0°C to 60°C.

The analog control voltage is generated by two 8-bit external DAC's producing the I and Q controls for the quadrature modulator. The worst case variation is 20 ps which is acceptable for most applications. Since they can be calibrated out, matching the delay between differing devices is less important than minimizing delay variations over temperature. Fig. 7 plots the measured variation of the fine output delay pulse from five differing ASIC's. The worst case variation between devices is approximately 50 ps. The measured jitter of the timing generator less than 10 ps.

Conclusions

An ultra-precise timing generator has been presented for application to wide-band impulse radios and radars. The circuit is implemented in a Si/SiGe HBT technology, and can produce a pulse inside a 100 ns window with an accuracy of 2 ps and jitter of better than 10 ps. This is the first ASIC developed for the generation of extremely wide bandwidth pulses for impulse radio applications, substantially reducing the cost and improving the performance of this new communications technology.

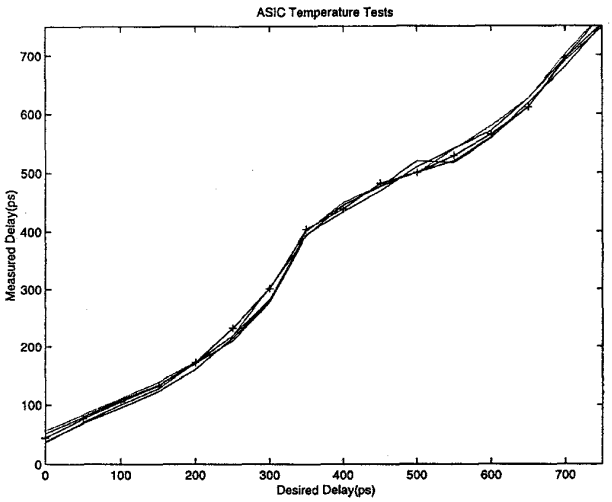

Figure 6. Measured variation of the fine output delay pulse with temperature. The worst case variation is approx. 20 ps over the range 0°C to 60°C.

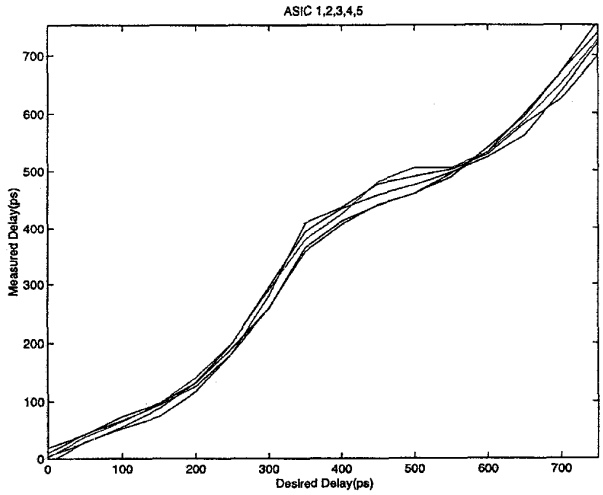

Figure 7. Measured variation of the fine output delay pulse from five different ASIC's. The worst case variation is approx. 50 ps.

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