ENERGY CONSTRAINED RF TRANSCEIVERS FOR MOBILE WIRELESS COMMUNICATIONS

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ABSTRACT

Several new approaches are presented for the reduction of power dissipation in wireless transceivers for mobile wireless applications. In most cases, the power dissipation of the circuit can be dramatically lowered without a significant reduction in circuit dynamic range or linearity. These techniques involve the use of active bias circuits to continuously optimize the performance of the circuit under varying bias levels.

I. INTRODUCTION

With the explosive growth of wireless communications, the airwaves are rapidly being filled with signals of varying strengths and frequencies. Immunity to jamming has become a significant concern to any communication system [1]. This is especially true for a mobile communication system, since it is difficult to predict the jamming environment the system will be exposed to. At the same time, the need for portability, and thus long battery life, requires the system to consume as little power as possible. From the perspective of radio transceiver design, this requires the simultaneous realization of *low-power* and *ultra-high-dynamic range* circuits — a near impossibility.

In a typical wireless transceiver design, as shown in Fig. 1 a narrow-band bandpass filter inserted before the low-noise amplifier can reject most of the jammers. However, a high filter rejection ratio incurs high insertion loss — a direct contributor of receiver sensitivity degradation. In addition, many close-in jammers are impossible to block given the size and cost restrictions of a mobile system. Fig. 2 illustrates some of the typically encountered broadband jammers as measured by a 2.5 GHz omni-directional antenna, which can vary depending on frequency, location, and environment.

At the same time, cellular systems such as IS-95 and GSM place a premium on reducing the effects of adjacent channel interference as well; an example of the dynamic range specifications typical of a GSM receiver are shown in Fig. 3. As a result of these environmental limitations, the receiver in a typical mobile system is designed to accommodate the *worst case* conditions in terms of dynamic range. To meet these demands, the LNAs, mixers, and active filters consume the most power in a receiver; unpleasant tradeoffs are usually required to balance dynamic range versus power consumption.

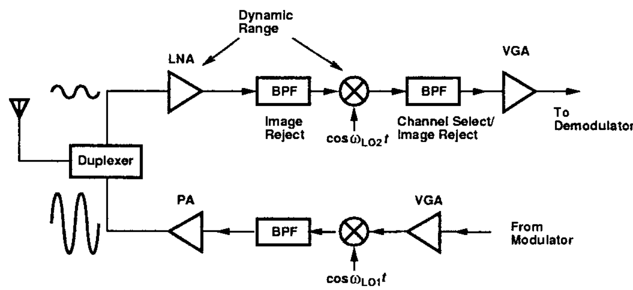

Figure 1: Block diagram of "typical" heterodyne transceiver illustrating dynamic range requirements of receiver and transmitter.

By contrast, handset transmitter power amplifiers are characterized by the need for modest output power requirements (typically 1W or less) but ideally require very high dc-to-rf conversion efficiency. Although the *peak* efficiency of the power amplifiers is often very high, their *average* efficiency can be miserably low, in part due to the wide variation in transmitted power required in a CDMA system. The adaptive power control circuit in a CDMA handset — required to minimize the "near-far" problem — results in a near-Gaussian transmitted power profile, as shown in Fig. 4. Most power amplifiers maintain a roughly constant dc power dissipation as the output power of the amplifier is reduced, hence the average dc efficiency of the amplifier suffers. In addition, handset amplifiers require relatively simple and low-cost solutions, due to the large consumer-based market that they must address.

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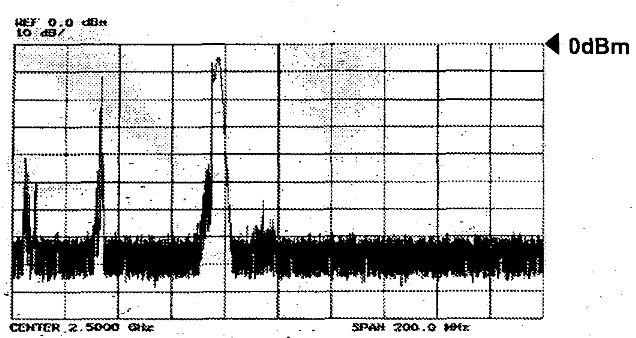

Figure 2: "Typical" jamming spectrum and power levels centered at 2.5 GHz. Note that the peak jamming power can approach 0 dBm. Some of the microwave energy is associated with unintentional jammers, such as microwave ovens.

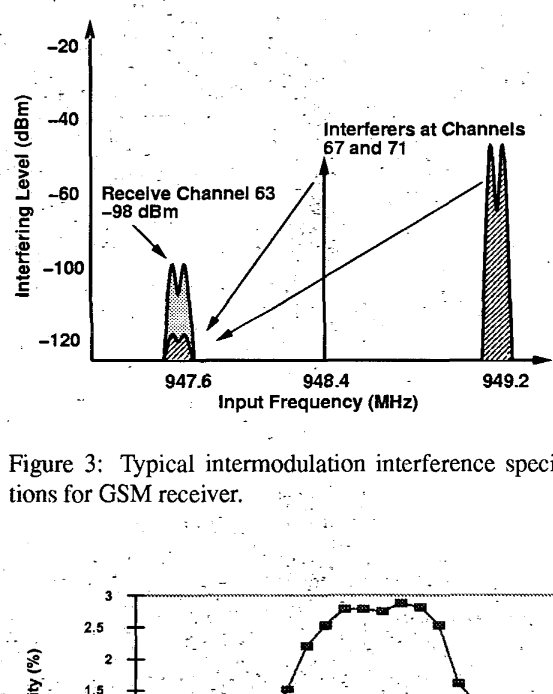

Figure 3: Typical intermodulation interference specifications for GSM receiver.

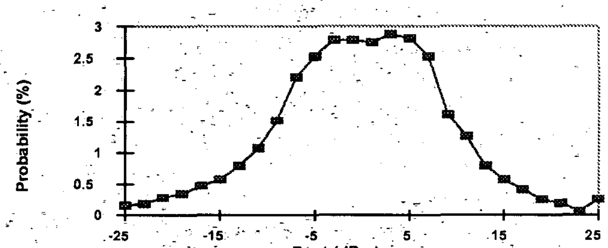

Figure 4: Measured profile of transmitted output power of CDMA handset [2].

A promising approach is to employ *energy constrained* design techniques for the radio frequency receiver and transmitter portions of the circuit. These designs partially circumvent these compromises by optimizing power consumption for the operating environment — a high dynamic range when the receiver is near or in compression, but low power consumption when the receiver is in small-signal operation where a large dynamic range is not necessary. For the transmitter, the goal is to utilize *only* that dc power consumption required to transmit the required power. This paper will present some preliminary results we have obtained on energy constrained optimization of radio frequency transceivers.

II. RECEIVER DESIGN APPROACHES

For an input RF power significantly below the compression point, or the point where significant intermodulation occurs, the linearity of a receiver is not a concern. Power consumption and noise figure are the primary considerations. But, as the input power rises, the intermodulation products increase rapidly and the noise figure of the receiver can degrade significantly. Hence, it is desirable for the receiver's third-order intercept point (IP3), to increase as the input power increases. Since linearity generally improves with increasing dc power, improving the IP3 of a given device would require higher power consumption. In wireless communication systems, the LNA only occasionally experiences high input power — when a strong jammer or adjacent channel is present. Under these circumstances, increasing the supply current to the LNA is a small price to pay to prevent loss of data or dropping the link. As an example, Fig. 5 plots the desired adjustment in transistor current under strong jamming conditions in order to maintain the desired dynamic range [3].

Under normal conditions, large input power levels drive the amplifier into Class-AB operation, which yields some improvement in linearity due to the higher power dissipation, but the improvement is not optimal due to the clipping of the drain current waveform. Instead, a temperature compensated power detector at the output of the amplifier can be employed to measure the signal level, and adjust the bias level accordingly. This variation is accomplished with the basic topology shown in Fig. 6 as implemented in a 2.5 GHz LNA. The design employs a two-stage cascaded configuration with a low-noise PHEMT at the input and a hetero-junction FET at the output. Two Schottky diodes in a dual package form the power detector. The bias control is composed of two operational amplifiers that compare the drain-source voltages (V_{DS}) and the power detector output voltage (V_{PD}).

With higher IP3 and lower NF in large-signal operation, the LNA achieves a 10.5dB improvement in spurious-free

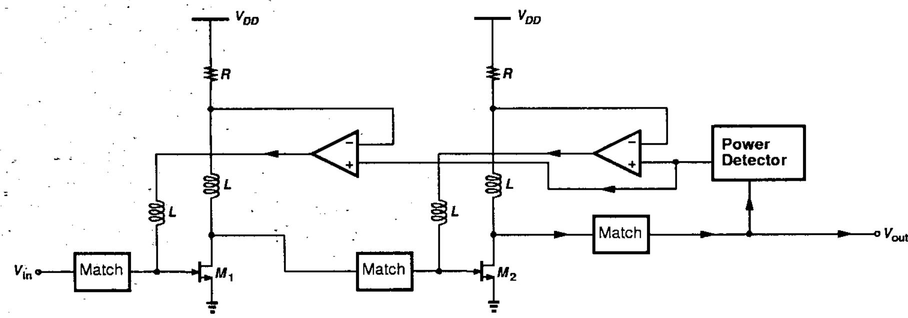

Figure 6: Simplified schematic of dynamically biased LNA.

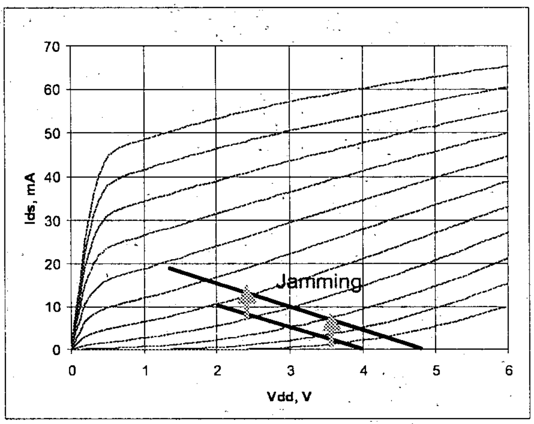

Figure 5: Optimized adjustment of LNA load-line in response to jamming to improve dynamic range.

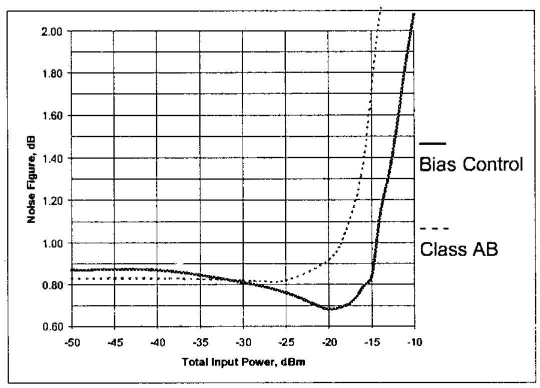

Figure 7: Variation in noise-figure with input power with the circuit of Fig. 6. A comparison to the operation of the circuit under Class-AB mode is included.[3]

dynamic range (SFDR) compared to nominal conditions, as shown in Fig. 7 and Fig. 8 [3]. The bandwidth used for calculating SFDR is 1.25MHz. The same LNA in Class AB could only obtain a 3.1dB improvement in SFDR. A typical LNA with fixed current consumption exhibits little, if any, increase in SFDR as the input power is increased. In all cases, the *nominal* power dissipation of the fixed and dynamically biased LNA's are the same.

III. TRANSMITTER DESIGN APPROACHES

The problem of energy optimized transmitter design is in some ways the same as that of the receiver; the optimum bias current and voltage depends on the output power requirements at any given instant in time. Traditional systems vary these parameters little, if at all, in response to the changing dynamics of the environment. An improved definition of power amplifier efficiency — one that accounts for the statistical nature of the transmitted power and the energy

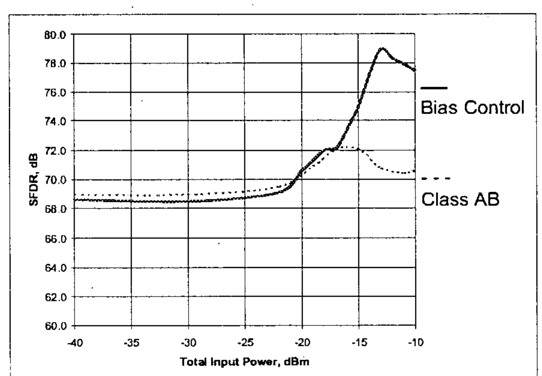

Figure 8: Variation in spur-free dynamic range variation with input power with the circuit of Fig. 6. A comparison to the operation of the circuit under Class-AB mode is included. [3]

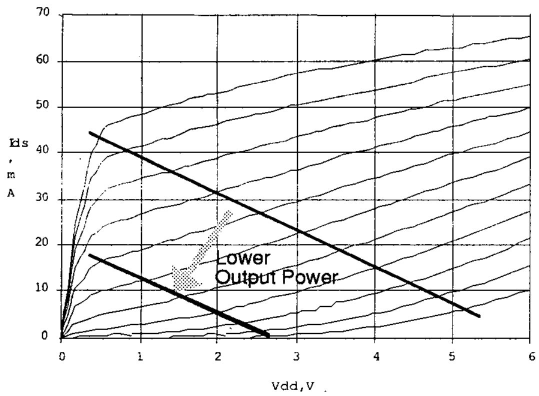

Figure 9: Optimized variation of power FET vias conditions as a function of output power variation.

efficiency of the power amplifier — is given by [4].

$$\overline{\eta} = \frac{\int_{-\infty}^{\infty} P_L g(P_L) dP_L}{\int_{-\infty}^{\infty} f(P_L) g(P_L) dP_L} \quad (1)$$

where $f(P)$ is the dc input power of the amplifier at output power P, and $g(P)$ is the probability of output of the amplifier at output power P. It was shown in [4] that the mean efficiency of a typical CDMA amplifier with this definition is only 7% !

In most cases, the most straightforward manner to vary the bias conditions is to alter the transistor dc drain (or collector) current. In Class AB-mode the current waveform is asymmetric, and the dc average current varies automatically with output power level. In the limit of class B operation, the dc bias varies according to the square root of output power and the power efficiency varies as $P^{1/2}$ over a narrow range (albeit at some cost in linearity).

Dynamic gate biasing (changing bias conditions as a function of input power by using an input signal envelope sensitive biasing network) can be used. It is also possible to vary the dc drain or collector supply voltage in accordance with the output power level. The most desirable solution is to simultaneously vary the dc bias current (through the gate or base voltage) and drain or collector supply voltage as shown in Fig. 9

IV. CONCLUSION

A variety of approaches have been presented for the minimization of the energy usage of a mobile wireless transceiver, without compromising system performance in a dynamic environment. These techniques exploit the potential ability to adapt the performance of the receiver in response to the received power, or the transmitter in response to the transmitted power. It is anticipated that this class of approaches will have a major impact on wireless transceiver design in the future.

V. ACKNOWLEDGMENTS

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VI. REFERENCES

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