A 16x16 Si/SiGe HBT Cross-Point Switch Architecture for High-Speed Switching Applications

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Abstract

A new architecture is presented for a high-speed 16x16 cross-point switch, based on a Si/SiGe HBT technology. The design incorporates a variety of improved circuit techniques to reduce dc power dissipation, improve speed, and reduce jitter. A 4x4 version of the switch was fabricated, with a bandwidth of approximately 8 GHz. The simulated maximum data rate of the 16x16 version is in excess of 10 Gbps with a power dissipation of approximately 2W.

I Introduction

A wide variety of emerging multimedia applications — integrating voice, data, and video traffic — require a new generation of high-speed switching networks. The hardware requirements for these networks include advanced fiber-optic electronics and cross-point switch designs, all operating at clock rates in excess of 10 Gbps.

Si/SiGe HBT technology offers an attractive semiconductor technology for the realization of these switching circuits, due to its high f_T (> 40 GHz), high f_{max} (> 50 GHz), and high level of integration in an advanced silicon technology [1]. However, new architectures and circuit designs are required in order to exploit the intrinsic high-speed performance of these devices for next generation applications. Some of the design considerations include reducing power dissipation and improving the maximum data rate, as well as minimizing jitter, propagation delay, and configuration timing setup overhead.

This paper reports on a preliminary design study of an improved cross-point switch architecture, based on Si/SiGe HBT technology. The design goal is a data rate in excess of 10 Gbps and power dissipation of less than 3W.

II Si/SiGe HBT Technology for High Data Rate Switching Applications

The outstanding high-frequency performance of Si/SiGe HBT technology has been well established by a variety of groups [1], [2]. In many applications, this speed performance advantage can be "traded-off" in a very satisfactory way for dramatically reduced power dissipation at a desired speed. It is at these low power levels where Si/SiGe HBT technology has a distinct advantage compared to Si BJT or CMOS technology. The germanium content within the base of the SiGe HBT leads to a device of superior performance compared with a similarly structured silicon-only epitaxial-base transistor. A good example of this improvements can be seen from the transistor data presented in Figure 1, which compares transistor f_T as a function of collector current for epi-base SiGe HBTs and Si BJTs of comparable base resistance (approximately $12k\Omega/\square$) [3]. In this case, the peak f_T's for the Si BJT and SiGe HBT are 38 and 50 GHz respectively. The epi-base SiGe HBT achieves higher f_T values than the epi-base Si BJT over its entire range of operation. In addition,

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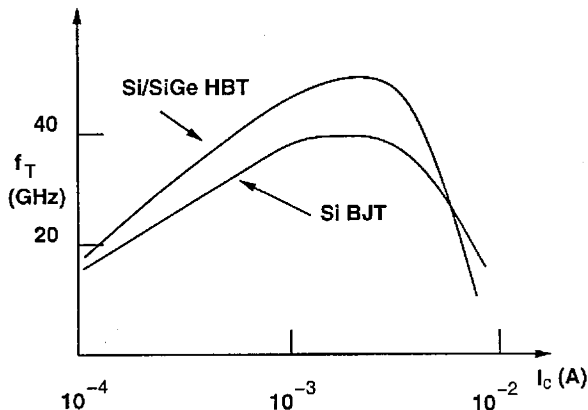

Figure 1: Comparison of f_T of Si BJT and Si/SiGe HBT for comparable epi base thickness and resisitivity.

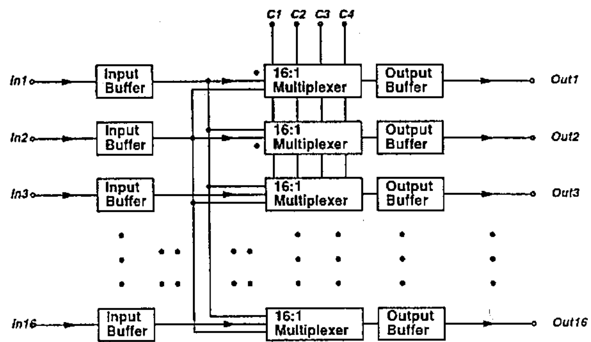

Figure 2: Si/SiGe HBT Cross-point switch architecture.

for a given required f_T *and* f_{MAX}, the SiGe HBT requires roughly one-third the collector current of an "equivalent" Si BJT, dramatically lowering the power requirements in those circuits that are required to operate at very high frequencies.

III-V-based devices in GaAs or InP technology will exhibit superior f_T and f_{MAX} compared to a Si/SiGe device for a specified geometry. Clearly, if maximum performance or speed is the *only* criteria, then III-V technology is the superior option. III-V-based devices will also exhibit superior breakdown voltage properties at a given speed due to their higher bandgap energies and mobilities. The well-known Johnson limit for speed vs. breakdown voltage in semiconductor devices results in much higher gain for the GaAs devices, even at the lower operating voltage, due to the higher electron mobility. However, the cost of III-V technology still greatly exceeds that of silicon technology, and the high levels of integration required for 16x16 and larger switches will require the use of a state-of-the-art silicon-based technology — like Si/SiGe — for the foreseeable future.

III Description of Architecture

The initial design that we report on here utilizes a non-blocking architecture, consisting of sixteen independent 16:1 multiplexers to allow each output to be independently connected to any input, as well as any input to be connected to any or all outputs. This basic architecture is very similar to existing cross-point switches implemented in silicon bipolar technology and GaAs MESFET technology [4]. A block diagram of the architecture is shown in Figure 2. The configuration control is updated in a serial fashion, where the four-bit output select word is latched, the four-bit input word select is latched, the load pulse is executed, and the process is then repeated for each output an additional fifteen times.

Some of the advantages of this architecture are its intrinsic high-speed, low dc power dissipation, and relatively low transistor count. However, it is more prone to cross-talk degradation of the jitter performance due to the full width of each of the signal buses on the multiplexer — 16 bits in this case. Each input can capacitively couple to every output through the multiplexer. Recently, a multi-level switch architecture was presented that provided improved jitter performance through the use of segmentation of the input signals at the block level [5]. In our case, improved isolation was achieved through the use of a common-base stage — to be described in the next Section — which improves the isolation from each multiplexer input to the output.

IV Transistor Level Circuit Design

The design of the switch at the circuit level requires careful attention to cross-talk issues resulting from input/output buffers, common lead inductances for the power supplies, and within the multiplexers themselves. Fully differential signal routing is utilized on-chip to minimize the effect of common-mode power supply variations. Power supply inductance is minimized though the use of "flip-chip" mounting techniques; in this case, each I/O has an typical inductance of only 50-100 pH. Flip-chip techniques are especially important for I/O intensive applications like cross-point switches, where data jitter due to packaging effects alone is expected to be significant.

At the 10 Gbps data rate envisioned for this switch, fully differential input and output signals are maintained at every high-speed I/O port. The outputs are "reverse-terminated" with 50Ω resistors on-chip to minimize ringing effects at the board level. This increases the power dissipation, but assures a high degree of interface signal integrity in the presence of an uncertain board impedance.

A greater problem arises from *on-chip* transmission line effects, which will result in unacceptable ringing on the signal lines at the 10 Gbps data rate envisioned for the switch. This problem is illustrated in Figure 3 on the next page, which shows the simulated response of the data "transmission line" with a 10 Gbps pulse. The transmission line is periodically loaded by output multiplexers, and appears to be a highly dispersive transmission line. The ringing is reduced through an optimized transmission line termination impedance, which in the ideal case would have a value of approximately Z_0 — the characteristic impedance of the transmission line. In a practical case, the optimized value of the termination is *frequency dependent* due to the dispersion in the transmission line [6]. In this case, a 50Ω line represented an optimimum tradeoff between power dissipation and ringing due to transmission line effects.

In order to minimize the data jitter, a cascode (grounded-base) stage was added to each multiplexer stage to improve the isolation of each individual input

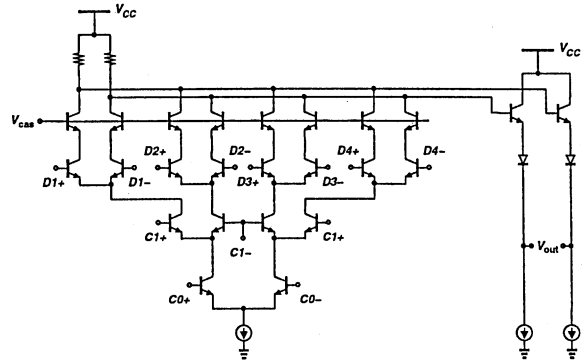

Figure 4: Design of 4:1 multiplexer.

from the output when it is disabled, as shown in Figure 4. This is especially problematic in a multiplexer architecture, because four inputs are separated from *each* output by only one device, and *all* inputs are separated from *every* output by at most two devices. As a result the jitter performance due to cross-talk on the chip is approximately

$$\tau_{jitter} \approx \sqrt{N}\alpha\tau_{rise} \quad (1)$$

where N is the number of inputs connected to an output, α is the isolation per stage, and τ_{rise} is the average rise time of each input. For example, at 10 Gbps, the average rise time is approximately 50 ps, and a 16x16 switch will require an α of approximately -40 dB to achieve less than 5 ps jitter. This resulted in a small increase in the power dissipation of the circuit, but the improvement in cross-talk is approximately 20 dB at these frequencies. A schematic of the multiplexer design is shown in Figure 5. A total of five 4:1 multiplexers are connected together to realize a complete 16:1 multiplexer.

V Simulation and Experimental Results

A 4x4 version of the crosspoint switch was fabricated in order to evaluate some of the isolation, I/O, and packaging concepts introduced here. The chip was mounted using the IBM "C4" process, which pro-

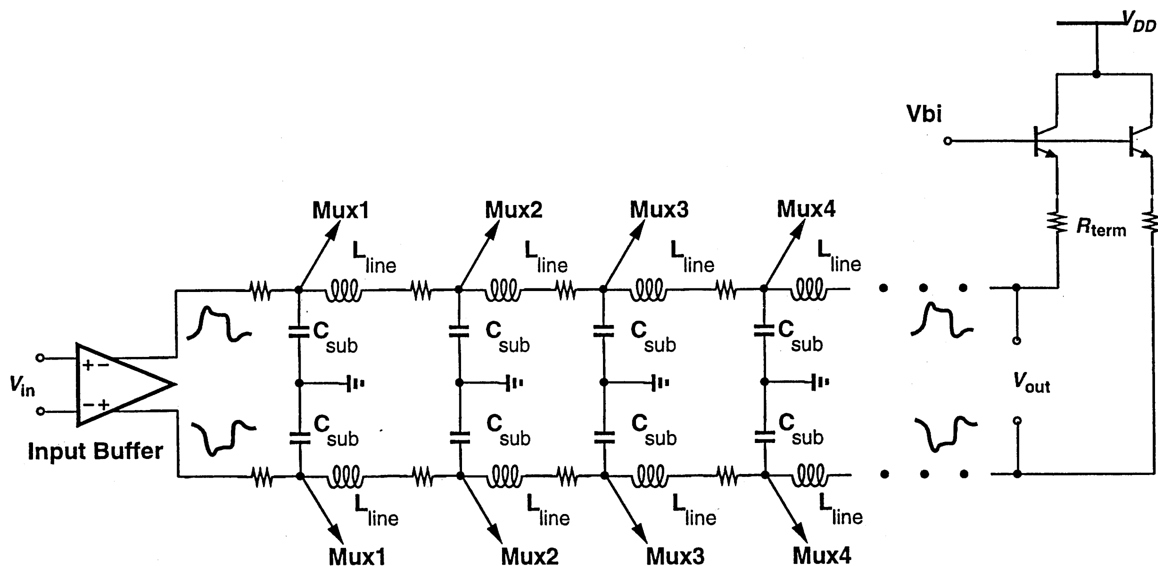

Figure 3: Pulse propagation limitations on high-speed multiplexer interconnects.

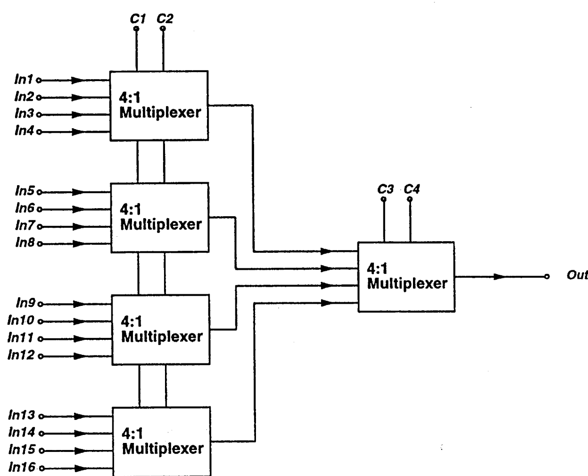

Figure 5: Architecture of 16-bit multiplexer.

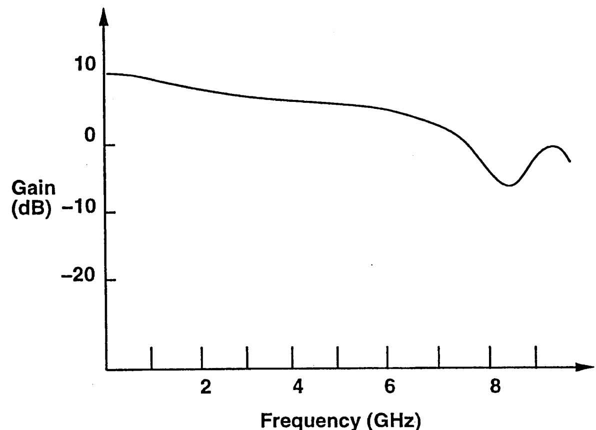

Figure 6: Measured frequency response of 4x4 Si/SiGe HBT cross-point switch.

vided a low inductance ($\approx$ 50 pH) interconnect environment at all ports. Figure 6 plots the measured frequency response of the packaged 4x4 switch, and aside from frequency dependent losses in the board level interconnect, the 3 dB bandwidth is approximately 7 GHz. Inter-port isolation was also evaluated on the test chip, and exceeded 35 dB at 15 GHz.

The 16x16 switch was designed to operate from a single power supply, with fully differential inputs and outputs. Figure 7 is a plot of the simulated propagation delay through the 16 x 16 cross-point switch (input port to 16:1 multiplexer to buffer output), with

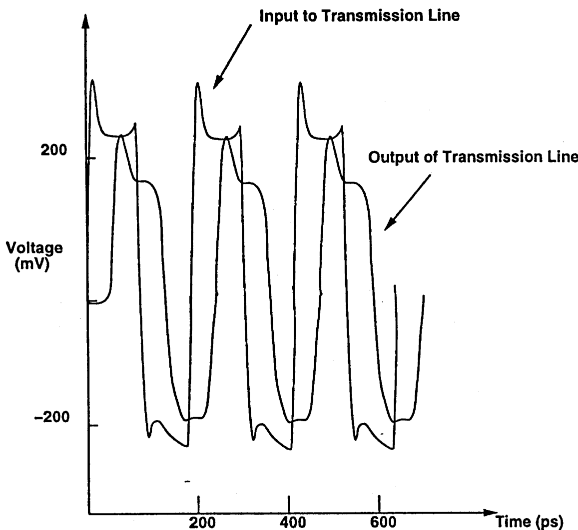

Figure 7: Simulated propagation delay through 16x16 Si/SiGe HBT cross-point switch.

a 5 Gbps input, showing an overall delay through the transmission line of 50 ps. The power budget of the chip currently allocates approximately 100 mA for the output buffers, 100 mA for the multiplexers and selection logic, and 50 ma for the input buffers, for a total power dissipation of approximately 1.5 - 2 W from a 6 V supply. This compares very favorably to commercially available implementations of cross-point switches, which require higher powers at lower speeds [7].

VI Conclusions

A new architecture has been presented for a 16x16 cross-point switch, implemented in a Si/SiGe HBT technology. Careful attention is paid to on-chip transmission line effects, and improved isolation techniques — all in an effort to reduce jitter to an absolute minimum. A 4x4 prototype switch was evaluated, with a bandwidth in excess of approximately 8 GHz. The simulated propagation delay through the 16x16 design is approximately 150 ps, consistent with 10 Gbps operation, and the estimated power dissipation is approximately 2W in a 50Ω environment.

References

[1] D.A. Sunderland, D.C. Ahlgren, M.M. Gilbert, S.-J. Jeng, J.C. Malinowski, D. Nguyen-Ngoc, K.T. Schonenberg, K.J. Stein, B.S. Meyerson, and D.L. Harame, "Manufacturability and applications of SiGe HBT technology," *Solid-State Electronics*, vol. 41, no. 10, pp. 1503–7, Oct. 1997.

[2] D. Nguyen-Ngoc, D.A. Sunderland, D.C. Ahlgren, S.J. Jeng, M.M. Gilbert, J.C. Malinowski, K.T. Schonenberg, K.S. Stein, B.S. Meyerson, and D.L. Harame, "A manufacturable poly-emitter graded-SiGe HBT technology for wireless and mixed-signal applications," *Applied Surface Science*, vol. 102, pp. 194–201, Aug. 1996.

[3] L.E. Larson, "High-speed Si/SiGe technology for next generation wireless system applications," *Journal of Vacuum Science & Technology B Microelectronics and Nanometer Structures*, vol. 16, no. 3, pp. 1541–8, May-June 1998.

[4] R. Savara and A. Turudic, "A 2.5 Gb/s 16*16 bit crosspoint switch with fast programming," in *IEEE GaAs IC Symposium*, New York, NY, USA, 1995, pp. 47–8, IEEE.

[5] A. Metzger, C.E. Chang, P.M. Asbeck, K.C. Wang, K. Pedrotti, A. Price, A. Campana, D. Wu, J. Liu, and S. Beccue, "A 10 Gb/s 12*12 cross-point switch implemented with AlGaAs/GaAs heterojunction bipolar transistors," in *IEEE GaAs IC Symposium*, New York, NY, USA, 1997, pp. 109–12, IEEE.

[6] E. Sokolowska, G. Fortin, N. Belabbes, M. Gagnon, C. Roy, and B. Kaminska, "Bidirectional analog 8*8 switch matrix with large input signal and over 1 Ghz bandwidth.," in *IEEE GaAs IC Symposium*, New York, NY, USA, 1997, pp. 236–9, IEEE.

[7] R. Savara, "A high speed and high precision 64*33 crosspoint switch IC," in *IEEE GaAs IC Symposium*, New York, NY, USA, 1997, pp. 105–8, IEEE.