DESIGN OF A HIGH DYNAMIC-RANGE VARIABLE-GAIN-AMPLIFIER FOR A DBS TUNER FRONT-END

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Abstract

An L-band high dynamic-range variable-gain-amplifier (VGA) for a direct down-conversion Direct Broadcast Satellite (DBS) tuner is presented. Measured performance is: gain -22 to +32 dB (54 dB range); input-referred 3rd-order intercept point (IIP3) ≥11 dBm (worst case); Noise Figure 13 dB. The DC operating voltage range is 5V±10%, and the ambient temperature range is -20°C to +70°C (approximately +30°C to +120°C junction temperature). Performance was measured from 950 to 2060 MHz.

Introduction

The challenge in the design of the VGA was to achieve a low Noise Figure in the high-gain state, a high linearity in the low-gain state, and a sufficiently gradual increase in Noise Figure and decrease in linearity with gain adjustment (roughly 1dB/dB). A current steering design was chosen for this amplifier [1], which allowed the design to be partitioned into three major design tasks: (A) a high-gain low-noise amplifier; (B) a low-gain high-linearity amplifier; and (C) the bias control circuitry to steer the amplifier currents for optimal performance.

High-gain Low-noise Portion of VGA

The high-gain amplifier portion of the VGA is made up of three cascaded stages of non-degenerated differential-pairs of NPN transistors with resistive loads. Each stage was designed to have approximately 12 dB gain by scaling the load resistor and current source values. PTAT (proportional-to-absolute-temperature) current sources were used to provide constant gain over temperature.

The primary means of achieving a low Noise Figure was by using no emitter degeneration, which increases thermal noise, and by using large size devices to lower the overall base resistance. The drawback of these two techniques is lower linearity and lower input impedance. However, linearity is not an issue at the very low input level under high gain operation (-74 dBm). The lower input impedance of the larger devices can be transformed to the desired 75Ω value using off-chip reactive matching.

Low-gain High-Linearity Portion of VGA

The linearity of the system was specified in terms of third-order product interferers rather than IP3, since there may be many third-order product combinations appearing in the RF band of interest. The linearity was specified such that the total power of all in-band third-order products would be at least 20 dB below the carrier of interest. Assuming that all carriers are balanced in amplitude, the total input power due to 32 channels at -20 dBm each is equal to:

$$P_{total} = -20\ \text{dBm} + 10\log(32) = -5\ \text{dBm} \qquad (2)$$

(all carrier phases incoherent), with a small statistical chance of all signals in phase producing:

$$P_{total} = -20\ \text{dBm} + 20\log(32) = +10\ \text{dBm} \qquad (3)$$

(when all carrier phases are coherent). The design was approached with a worst case assumption (+10 dBm input), which corresponds to 866 mV RMS into 75 Ω. The low-gain amplifier portion of the VGA was made up of three stages of emitter-degenerated differential-pairs of NPN transistors with resistive loads. The current sources and degeneration resistors were designed to ensure a linear response to the input voltage. The load resistors were chosen so that each stage would have approximately -8 dB gain.

Fig. 1 shows a schematic of one stage of the VGA with the high- and low-gain portions summed in the load resistors.

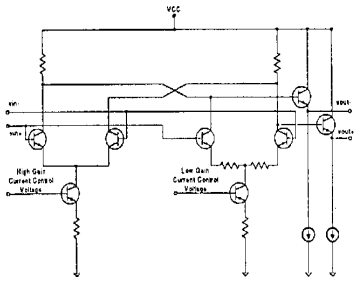

Fig. 1 Schematic of one stage of the VGA

Bias-control Circuitry

The VGA is varied by a 1 to 4V control voltage (lowest to highest gain), which is used to steer current between the high-gain and low-gain amplifiers. The total current must be PTAT to keep the non-degenerated pairs' gain constant over temperature. A block diagram of the bias control circuitry is shown in Fig. 2.

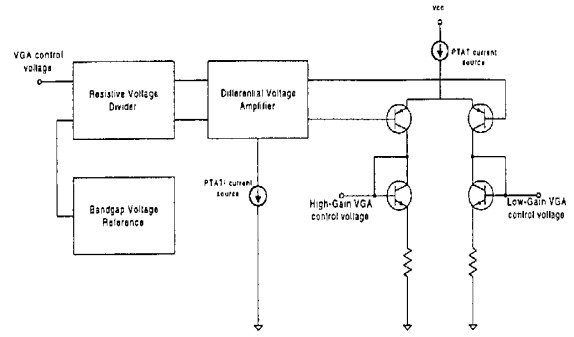

Fig. 2 Block diagram of VGA bias control circuitry

The VGA control voltage is divided down to a smaller range for input to a PNP differential pair that is used to set the current steering to set the VGA gain and linearity.

A. Resistive voltage divider

This portion of the bias circuitry is used to linearly reduce the control voltage from its initial range (1 to 4 V) to a range suitable for the following stage, which is a non-degenerated pair. The circuit, shown in Fig. 3, is simply a resistive voltage divider, relying on like resistors arranged in parallel and series to achieve a well-controlled ratio.

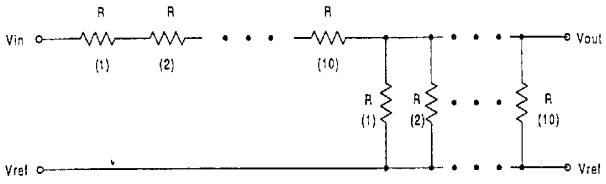

Fig. 3 Resistive voltage divider schematic

The reference voltage is generated by a band-gap voltage source followed by an operational amplifier; the input voltage is the control voltage. The transfer function of the divider is:

$$V_{out} = V_{ref} + \frac{1}{101}\left(V_{in} - V_{ref}\right) \qquad (1)$$

Thus the control voltage swing is reduced to approximately 30 mV from 3 V. The value of each resistor (R) is 1kΩ.

B. Voltage reference

This portion of the bias control circuitry is used to supply the reference voltage for comparison to the control voltage. A simplified schematic of the circuit is shown in Fig. 4.

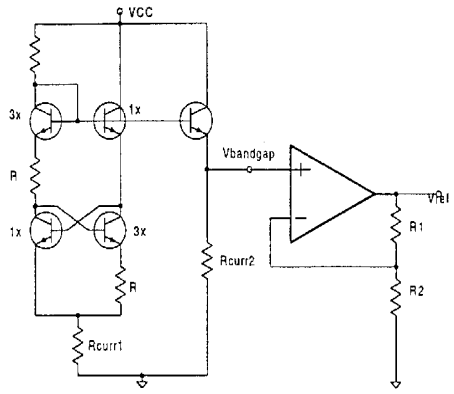

Fig. 4 Voltage reference circuit schematic

The band-gap reference voltage is generated by the circuitry on the left-hand-side of the figure [2]. The op-amp is used to buffer the output of the band-gap generator and to set the final reference voltage by the voltage divider network (R1 and R2).

C. PTAT current generator

The circuit generates a current that is proportional to absolute temperature (PTAT) [2]. A schematic of the circuit is shown in Fig. 5.

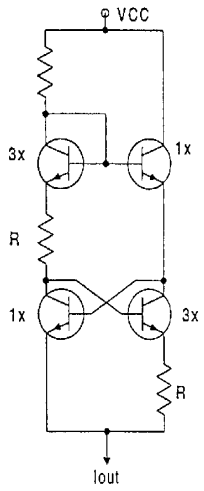

Fig. 5 PTAT current generator schematic

D. PTAT-squared current generator

This circuit converts a PTAT current to a one that is proportional to the absolute temperature *squared.* The current is mirrored to the following stage, a non-degenerated differential amplifier. A schematic of the circuit used to generate the current to be mirrored is shown in Fig. 6 [3, 4, 5].

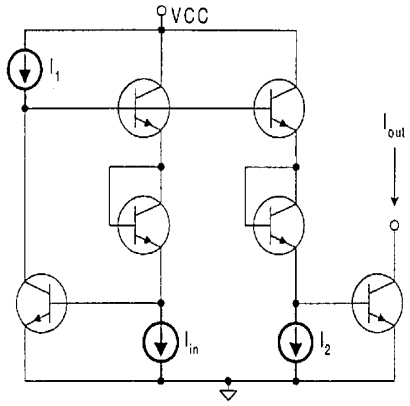

Fig. 6 Proportional-to-absolute-temperature-squared ($PTAT^2$) current generator

The output current, I_{out}, is expressed by the following equation:

$$I_{out}(T^2) = I_{in}^2(T)\frac{I_1}{I_2^2} \tag{2}$$

I_1 is made to be equal to I_2 and both are independent of temperature; I_{in} is made to be proportional to temperature. Therefore, I_{out} is proportional to the square of temperature. I_1 and I_3 are generated by mirroring the current through R_{curr2} in the band-gap voltage generator circuit. I_{in} is generated by mirroring the current in the PTAT current generator.

E. Temperature dependent voltage-output amplifier

This portion of the bias circuitry generates a differential voltage that is proportional to temperature by supplying a $PTAT^2$ current to a non-degenerated differential pair. The schematic is shown in Fig. 7.

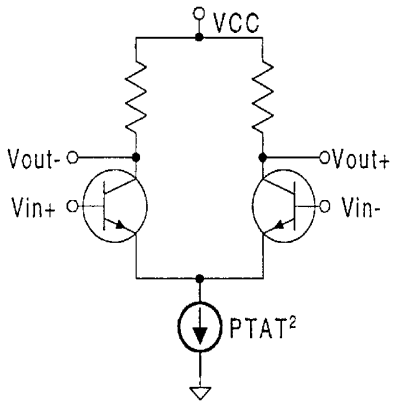

Fig. 7 Temperature dependent voltage-output amplifier

The amplifier produces a PTAT output voltage difference, due to the following relationships:

In the linear range (which we have ensured by reducing the incoming voltage swing to approximately 30 mV) the gain of a differential amplifier may be expressed as:

$$A_V = g_m R_L \tag{3}$$

where

$$g_m = \frac{I_C}{V_T} \tag{4}$$

Furthermore, the output voltage can be expressed as:

$$V_{out} = A_V \bullet V_{in}$$
$$V_{out}(T) = \frac{I_C(T^2)}{V_T(T)} R_L \bullet V_{in} \tag{5}$$

Since V_T is proportional to absolute temperature, if I_C is made to be proportional to absolute temperature *squared*, the output voltage will be proportional to temperature.

F. Current steering control circuit

This portion of the bias control circuitry converts the temperature dependent modified control voltage to control currents that supply the high- and low-gain RF amplifiers. A schematic of the circuit is shown in Fig. 8.

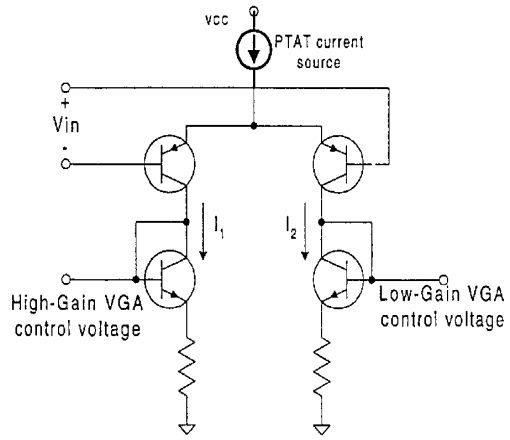

Fig. 8 Current steering circuit

The ratio of currents through the PNP differential pair is:

$$\frac{I_1}{I_2} = e^{V_{in}(T)/V_T(T)} \tag{4}$$

Therefore, the resultant ratio of currents is independent of temperature. This technique maintains a constant gain versus voltage characteristic over temperature. Other techniques achieve similar compensation [6].

IC Design, Layout, and Simulation Tools

The circuit was designed and fabricated in Maxim Integrated Products' GST-2 25 GHz Si-bipolar process. Schematic capture and simulations were done using Maxim's (Tektronix) Analog Design System (ADS). Layout, design-rule checking (DRC), back-annotation of parasitics, layout-versus-schematic (LVS), and electrical rules checking (ERC) were done using Maxim's QuickIC and QuERC design tools.

The layout of the IC is shown in Fig. 9. The overall dimensions are 0.6mm x 0.3mm.

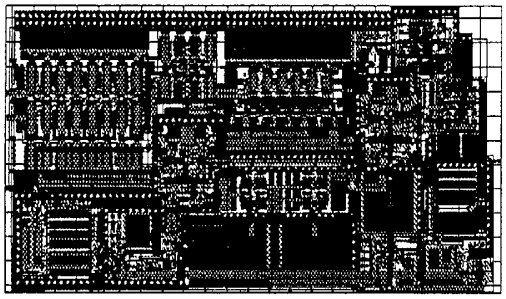

Fig. 9 Layout of Variable Gain Amplifier

The RF portion of the amplifier is across the upper part of the layout and the biasing circuitry is across the lower part. The inputs and outputs are differential.

Simulation Results

A. AC simulations

A simulation of gain versus frequency for the low and high gain states from 950 MHz to 2150 MHz is shown in Fig. 10. The lower trace corresponds to the minimum control voltage (1V) and the upper trace to the maximum control voltage (4V).

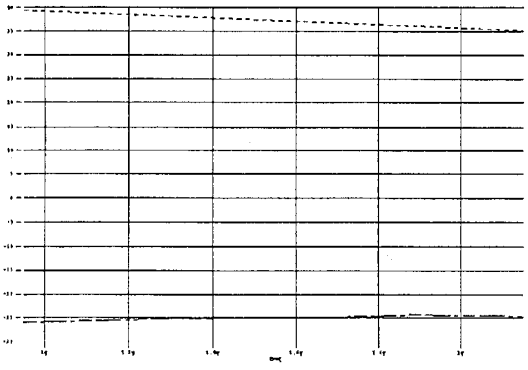

Fig. 10 Gain vs. frequency (low and high gain states)

The high gain is greater than 32 dB and the low gain is below -22 dB over the frequency range.

Fig. 11 shows the simulated gain versus control voltage for three frequencies (950 MHz, 1550 MHz, and 2150 MHz as indicated).

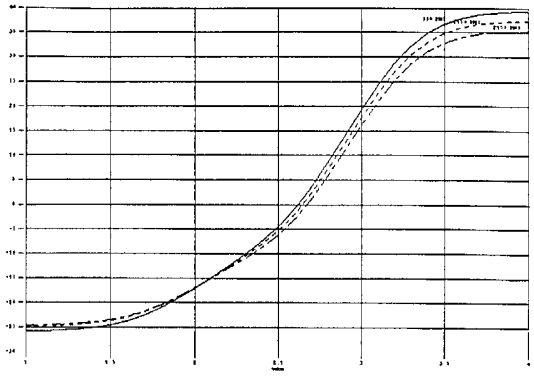

Fig. 11 Gain vs. control voltage (950 MHz, 1150 MHz, 2150 MHz)

Fig. 12 shows the simulated gain versus control voltage for three temperatures (40° C, 80° C, and 125° C as indicated) at 950 MHz. The simulation illustrates how the temperature ensures minimal variation of the characteristic over a wide range of junction temperatures.

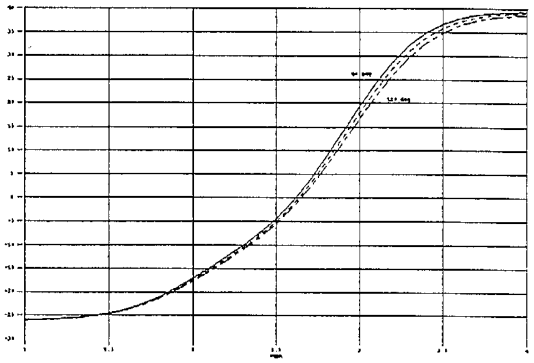

Fig. 12 Gain vs. control voltage at 950 MHz (40° C, 80 ° C, 120° C)

Fig. 13 shows the simulated VSWR (voltage-standing-wave-ratio) versus frequency in the high gain state. The low VSWR is achieved by using the impedance matching network shown in Fig. 14.

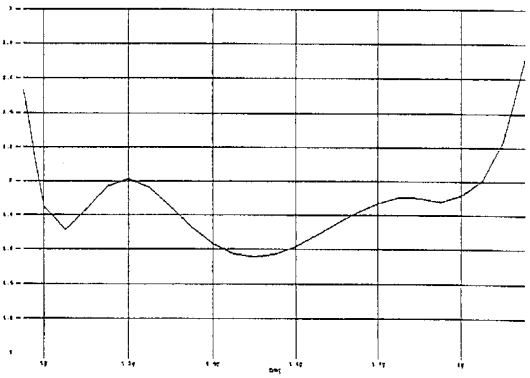

Fig. 13 VSWR vs. frequency (high gain state)

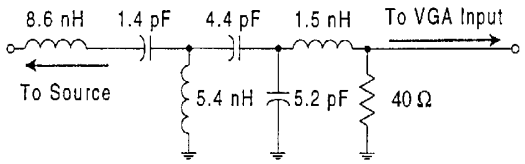

Fig. 14 Input matching network

Fig. 15 shows the simulated Noise Figure versus frequency in the high gain state.

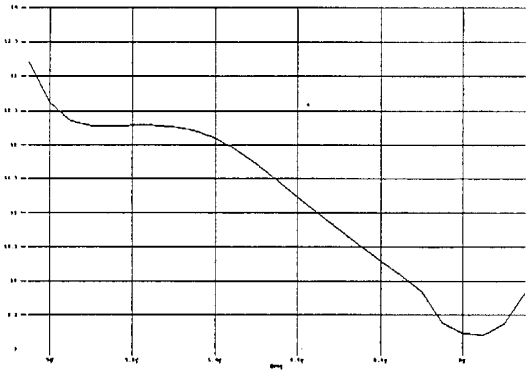

Fig. 15 Noise Figure vs. frequency at high gain setting

B. Transient simulations

In the transient simulations, the full maximum composite multiple tone input was used. In practice, the input will be 32 carriers, equally spaced from 950 MHz to 2150 MHz. To measure the linearity under this condition, a 31 carrier input was simulated, with the 32nd carrier empty. Then the output was examined and the ratio determined between the output power in the "empty" channel and an adjacent "present" channel. Energy in the "empty" channel output is due to non-linear mixing products of the "present" channels (primarily 3rd-order products).

Fig. 16 shows the simulated output versus frequency, in dBV, with maximum input tones (-20 dBm each) and minimum gain (-22 dB). The channels are spaced every 40 MHz between 950 MHz and 2150 MHz. The "empty" channel is centered at 1.52 GHz (approximately the center of the band). The ratio between the "empty" and adjacent "present" channels is greater than 20 dBc.

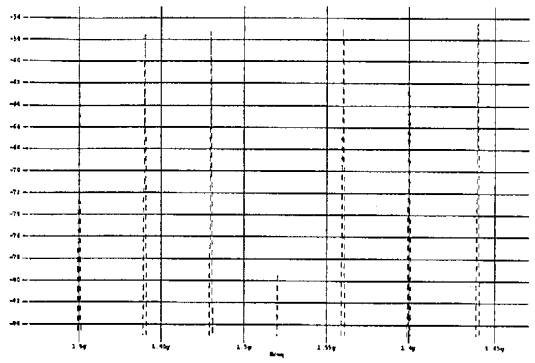

Fig. 16 Multiple tone output showing "empty" channel surrounded by "present" channels (energy at "empty" channel frequency is due to non-linear mixing products of "present" channels)

Measurements

The VGA was fabricated as part of a direct down-conversion tuner for a direct-broadcast satellite (DBS) receiver. A block diagram of the tuner is shown in Fig. 17.

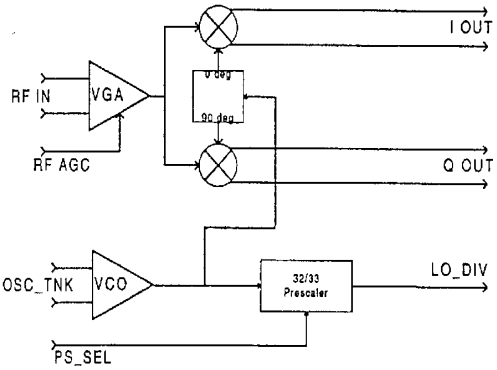

Fig. 17 Block diagram of direct down-conversion tuner for DBS receiver

All measurements of the VGA performance were made at the I and Q base-band outputs of the tuner. Each mixer's gain is 10 dB, which results in the measured gain range of the RF-to-base-band-output chain of -12 dB to +42 dB (rather than -22 dB to +32 dB).

A. Gain Range

The gain versus frequency (960 MHz to 2060 MHz) of the RF-to-base-band chain was measured over the complete gain range. Fig. 18 shows the gain versus control voltage 950 MHz and Fig. 19 shows the plot for 2060 MHz.

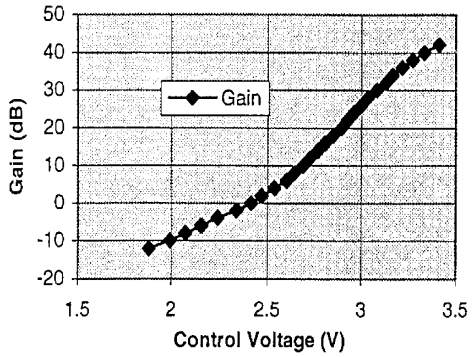

Fig. 18 Measured gain vs. control voltage (960 MHz)

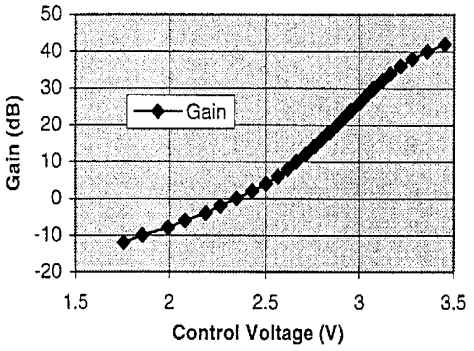

Fig. 19 Measured gain vs. control voltage (2060 MHz)

B. Noise Figure

A plot of Noise Figure versus frequency of the tuner for the high gain case is shown in Fig. 20. The measurement was performed at the high gain operating point. The measurement is a double-side-band mixer measurement; the actual single-side-band Noise Figure is 3 dB higher (approximately +13 dB across the band).

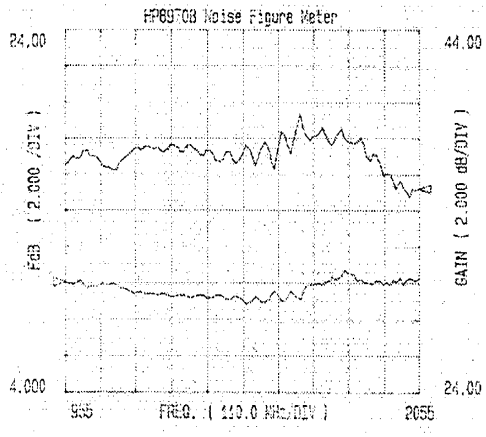

Fig. 20 Measured Noise Figure vs. frequency (high gain case)

Measurements of Noise Figure versus gain showed a degradation of less than 1 dB per 1 dB of gain.

C. Input 3rd-Order Intercept Point

The input referred 3rd-order intercept point was measured at the low gain point at the high and low frequencies as follows:

(1) The VGA control voltage was set so that with one -20 dBm input signal, the tuner gain was equal to -12 dB.

(2) The maximum composite for 32 tones at -20 dBm is -5 dBm (refer to equation 2). Therefore, the 2-tone analysis was performed with a composite input of -5 dBm, i. e. each of the two tones was set to -8 dBm.

(3) The difference between one fundamental and its adjacent 3rd-order product (in dB) was recorded.

(4) The input-referred IP3 was calculated as: input power at one fundamental frequency (-8 dBm) plus one-half the dB difference between the fundamental and third order product.

Results of a sample measurement are reproduced below:

f_{LO}=950 MHz $V_{in,LO}$=70 mV
f_{RF1}=959 MHz $P_{in,RF1}$=-8 dBm
f_{RF2}=961 MHz $P_{in,RF2}$=-8dBm
Fundamental to 3rd-order product difference: 42 dB
IIP3=-8dBm+(42 dB/2)
IIP3 (at 960 MHz) =+13 dBm

f_{LO}=2050 MHz $V_{in,LO}$=70 mV
f_{RF1}=2058 MHz $P_{in,RF1}$=-8 dBm
f_{RF2}=2060 MHz $P_{in,RF2}$=-8dBm
Fundamental to 3rd-order product difference: 38 dB
IIP3=-8dBm+(38 dB/2)
IIP3 (at 2060 MHz) =+11 dBm

Multiple devices were tested and the worst case IIP3 of any device at any frequency was +11 dBm.

Table 1 shows the degradation in IIP3 with increasing gain, which is approximately 1 dB/dB or less.

Table 1 Measured IIP3 vs. tuner gain

Tuner gain	IIP3
-12 dB	+13 dBm
-7 dB	+7.5 dBm
-2 dB	+2 dBm
+3 dB	-2 dBm
+8 dB	-4.5 dBm
+13 dB	-7.5 dBm
+18 dB	-10.5 dBm
+23 dB	-13 dBm

+28 dB	-16.5 dBm
+33 dB	-21 dBm
+38 dB	-25 dBm
+42 dB	-26.5 dBm

Conclusions

An L-band high dynamic-range variable-gain-amplifier (VGA) for a direct down-conversion Direct Broadcast Satellite (DBS) tuner was presented. Measured performance is: gain -22 to +32 dB (54 dB range); input-referred 3rd-order intercept point (IIP3) ≥11 dBm (worst case); Noise Figure 13 dB. The DC operating voltage range is 5V±10%, and the ambient temperature range is -20°C to +70°C (approximately +30°C to +120°C junction temperature). Performance was measured from 950 to 2060 MHz.

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References

(1) P. Gray and R. Meyer, *Analysis and Design of Analog Integrated Circuits, 3rd Edition*, pp. 708-709, John Wiley & Sons, New York, 1993.

(2) B. Gilbert, Lecture Notes.

(3) B. Gilbert, "General technique for N-dimensional vector summation of bipolar signals," Electronics Letters, vol. 12, pp. 504-505, September 16, 1976.

(4) E. Seevinck, *Analysis and Synthesis of Translinear Integrated Circuits*, Elsevier, Amsterdam, 1988.

(5) I. Koullias, S. Forgues, and P. Davis, "A 100 MHz IF amplifier/quadrature demodulator for GSM cellular radio movile terminals," *IEEE Bipolar Circuits and Tech. Mtg.*, 1990.

(6) G. Sahota and C. Persico, "High dynamic range variable-gain amplifier for CDMA wireless applications," *IEEE ISSCC Conf. Digest.*, pp. 374-375, Feb., 1997.