EFFICIENCY AND LINEARITY IMPROVEMENT IN POWER AMPLIFIERS FOR WIRELESS COMMUNICATIONS

P.Asbeck, G.Hanington, P.F.Chen, and L.Larson
University of California, San Diego, La Jolla, CA

Abstract

A key issue limiting power efficiency in wireless communication power amplifiers is the variation in signal level that must be accommodated. This paper discusses the importance of and techniques for varying the amplifier dc current and power supply voltage as a function of signal level. A high speed dc-dc converter operating from a 3.3V source, implemented with GaAs HBTs, is described. The efficiency of a 2Ghz power amplifier using the dc-dc converter is shown to increase by 40%, averaged over signal power variations characteristic of IS-95 CDMA systems.

Introduction

Efficiency of power amplifiers for wireless handsets is a critical concern for prolonging battery life. For systems with QPSK or other spectrally efficient modulation formats, linearity is also a key requirement. For acceptable linearity, generally output power must be backed off from its peak value, with a resulting drop in efficiency. Amplifiers also often need to function over a wide range of output power levels, as determined by fading statistics and varying mobile-to-base-station distances [1]. Power amplifier efficiency typically drops rapidly at the reduced power levels, leading to low overall system efficiency. This paper describes strategies to improve PA efficiency, particularly at low power levels, which can dramatically improve the overall system efficiency.

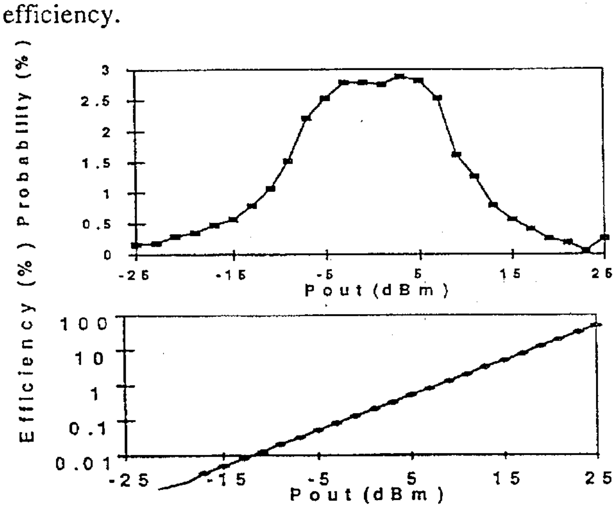

Fig.1: (a) Probability distribution of transmitted power level for a representative CDMA handset. (b) Efficiency of an ideal Class A amplifier as a function of output power level.

Figure 1 shows a representative probability distribution for the transmitted power of a CDMA handset. Although the peak output power is over 300 mW, the average output power is below 10mW. The figure also shows the drain (or collector) efficiency of an ideal Class A amplifier as a function of the output power, P. The proportionality of efficiency to output power stems from the fact that the dc current and voltage are both independent of output power. To improve the situation, the dc current, dc voltage or both must be varied as output power changes. Figure 2 schematically shows how the dc bias point of an amplifier can be varied as the power is reduced from its maximum (saturated) value.

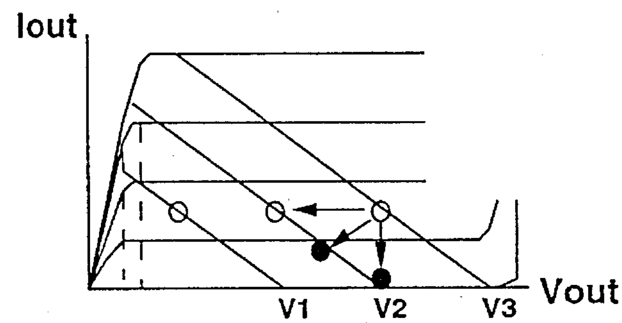

Fig.2: Schematic representation of output transistor characteristics and load line. The dc bias conditions at maximum power are shown, as well as desirable directions in which to vary the bias at lower output power levels.

Variable Bias Current

The most straightforward manner to vary the bias conditions is to alter the dc drain (or collector) current. In Class AB-mode the current waveform is asymmetric, and the dc average current varies automatically with output power level. In the limit of class B operation, the dc bias varies according to the square root of output power. As a result, power efficiency varies as $P^{0.5}$ over a narrow range (albeit at some cost in linearity). Dynamic gate biasing (changing bias conditions as a function of input power by using an input signal envelope sensitive biasing network) can also be used. The number of gate (or emitter) fingers in a composite large power transistor can be varied to optimize the current consumption (while also changing input and output impedance). The limit on dc bias current reduction is set by the tradeoff of linearity and efficiency. This technique is used in many presently available power amplifiers. Figure 3 shows, for example, the bias current and efficiency as a function of output power for a commercial HBT-based power amplifier. The $P^{0.5}$ regime is clearly visible.

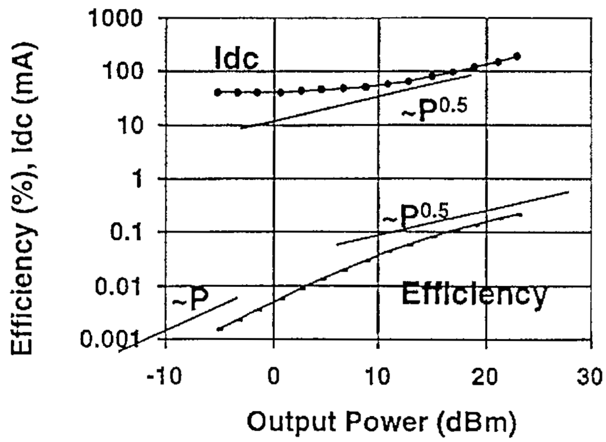

Fig.3: Measured dc input current and efficiency vs output power for a commercial CDMA power amplifier.

Variable Power Supply Voltage

It is also possible to vary the dc supply voltage in accordance with the output power level [2,3]. The most desirable solution is to vary simultaneously dc bias current and supply voltage.

To enable a changing voltage supply with output power, we have implemented dc-dc converters of small size, in a technology (GaAs HBT) which can be integrated monolithically with the power amplifier itself [4]. The dc-dc converter employs a high switching frequency (10-20MHz), which allows its output to be modulated rapidly to track the changing envelope of the output signal. Typical waveforms in cellular handsets have envelope variations in the 50KHz-2MHz range, according to different standards. The high switching rate of the converter also permits small inductors and capacitors to be used in the device, while minimizing ripple.

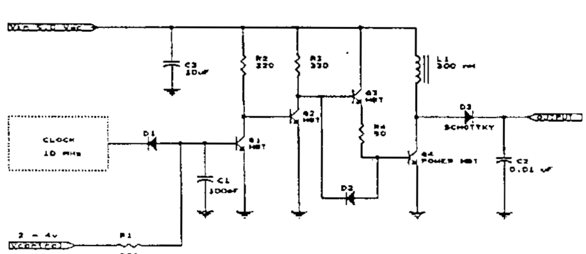

Fig.4: Circuit schematic for the dc-dc converter.

The circuit schematic for the dc-dc converter is shown in fig.4. A boost topology is used, providing an output voltage in the range 3V to 10V, for an input voltage of 3.3V. The converter employs a power HBT, capable of handling up to 1A of current. The inductor, Si Schottky rectifier and output capacitor are external elements. The circuit incorporates a pulse-width modulator in order to allow a dc input control voltage to regulate the output voltage.

Efficiency of the converter is dependent on the output load conditions, and is typically in the range 65-75%, as shown in fig.5. The output voltage could be modulated at high rates, with time constants below 1 μsec.

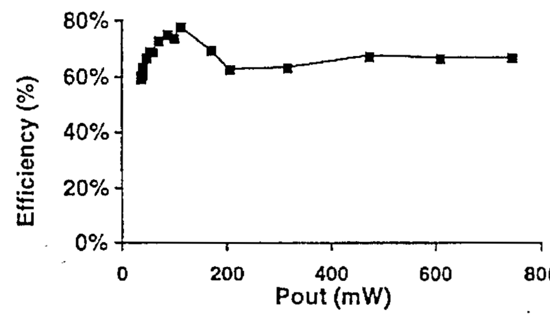

Fig.5: Measured efficiency of the dc-dc converter under various load conditions.

Amplifier Structure and Performance

The utility of the dc-dc converter was demonstrated for an amplifier of the structure shown in fig. 6. The input signal power was sensed with an envelope detector, which controlled the value of Vcc for the power amplifier stage.

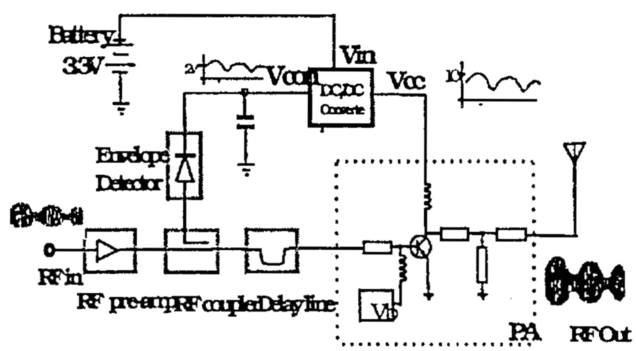

Fig. 6: Block diagram of the power amplifier employing the dc-dc converter

The value of the Vdd voltage was chosen to be somewhat larger than the amplitude of the rf signal swing at the drain of the device. The relationship between the two voltages is shown in fig.7.

It should be noted that the power amplifier remains in Class AB operation, and the overall output amplitude is governed by the input signal amplitude, rather than by the value of Vdd (which would apply for an envelope restoration amplifier). Thus it is not crucial for overall system linearity that the Vdd value exactly replicate the input signal - only that it remain in a regime suitable to avoid clipping, and increase efficiency.

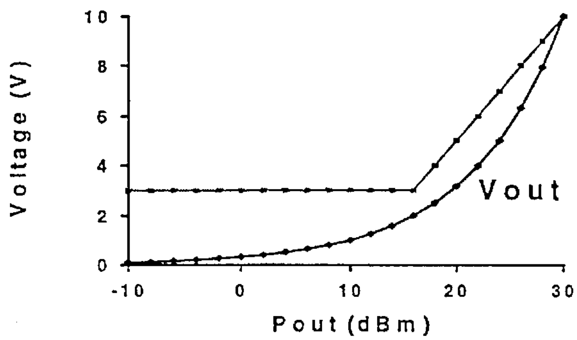

Fig. 7. Dc-dc converter output voltage (Vdd) and calculated rf output voltage amplitude, as a function of output power.

Fig. 8 shows the efficiency of the combined system as a function of output power. The value shown incorporates the inefficiency of the dc-dc converter as well as that of the amplifier. At the highest output power levels, the amplifier alone is more efficient, since there is no loss associated with the voltage converter. At lower power levels, the system with the dc-dc converter is superior, because of the ability to tailor the power supply voltage optimally. By using the dc-dc converter with the power amplifier, a significant improvement of overall efficiency results - because the net energy consumption of the system is dominated by the low power regime, where the amplifier alone is highly

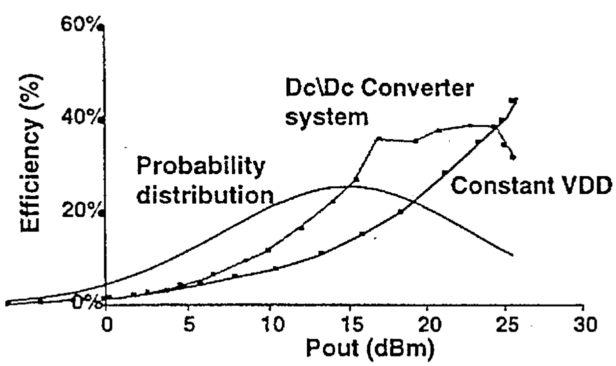

Fig.8: Measured efficiency of the amplifier operated at constant Vdd value and with dc-dc converter (to provide Vdd variable with input power). Also shown is a representative profile of power usage probability.

inefficient. After averaging the energy consumption weighted by probability of usage, the amplifier overall efficiency was increased by 40%. Further increases should be possible, with optimized ICs which integrate dc-dc converter and PA (together with an external inductor).

As the input power is varied and as the drain voltage of the rf output transistor correspondingly changes, in general the rf gain also varies. It is critical to avoid introducing distortion by the power supply time-dependence. To accomplish this, and to optimize the efficiency of the amplifier, we also controlled the gate bias voltage Vgg in accordance with the signal level. The overall gain is shown as a function of output power in fig. 9a, which illustrates a maximum variation of about 2dB. The gain was sufficiently constant to avoid excessive nonlinearity. The corresponding value of Vgg in order to meet this requirement is shown in fig. 9b. The value of Idd is shown in fig. 9c. The large variation of Idd with signal level is conducive to high efficiency.

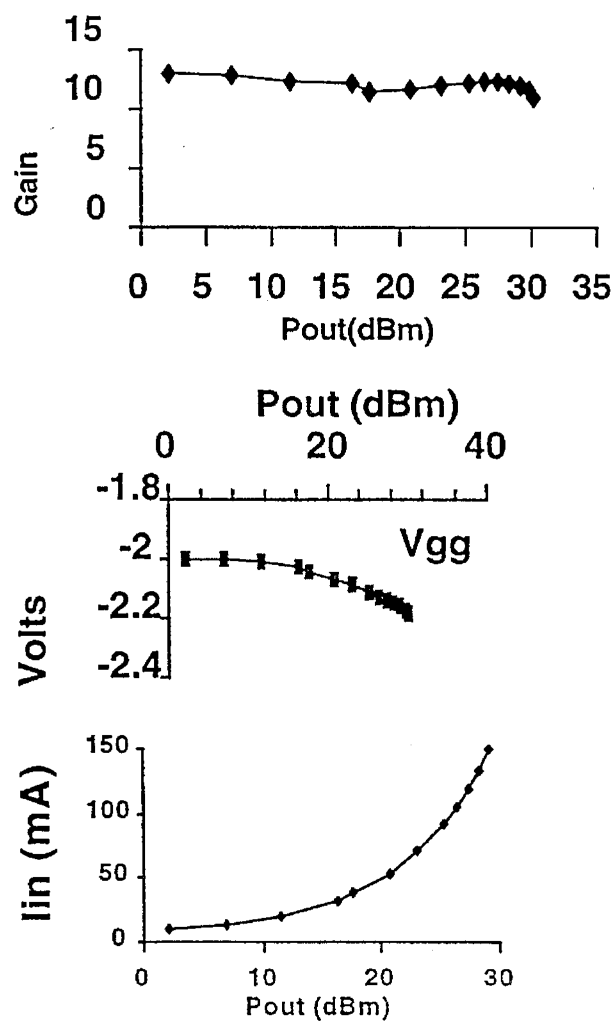

Fig. 9: a) Measured variation of rf gain with output signal level. b) Variation of gate bias voltage Vgg with signal level. c) Variation of dc current with signal level.

Conclusion

Significant improvements in efficiency, while maintaining linearity adequate for the requirements of digital modulation in wireless transmitters, can be realized with the use of a dc-dc converter that optimizes the supply voltage as a function of signal level. High performance dc-dc converters can be realized in GaAs HBT technology and can potentially be incorporated into the same IC as the power amplifier.

Acknowledgments

This work was funded in part by the Army Research Office, as part of the MURI on Low Power, Low Noise Electronics for Wireless Communications. The authors are grateful to J.Sevic, K.Gard, M.F.Chang, T.Itoh, V.Radisic for numerous helpful conversations during the course of this work. HBTs that were used in the dc-dc converter were provided by Hughes Research Laboratories (W.Hooper) and Rockwell Semiconductor Systems (H.Finlay).

References

1) J.Sevic, "Statistical Characterization of RF Power Amplifier Efficiency for IS-95 CDMA Digital Wireless Communication Systems," Proc. 2nd Annual Wireless Comm. Conf, 1997.

2) T.Nojima, S.Nishiki and K.Chiba, "High Efficiency Transmitting Power Amplifiers for Portable Radio Units", IEICE Trans. E74, 1563 (1991).

3) C.Buoli, A.Abbiati and D.Riccardi, "Microwave Power Amplifier with Envelope Controlled drain power supply", 25th European Microwave Conference, 1995.

4) G.Hanington, P.F.Chen, V.Radisic, T.Itoh and P.Asbeck, "A 10MHz HBT DC-DC Converter for Microwave Power Amplifier Efficiency Improvement", 1998 MTT-S.