Low-Power Radio Frequency Circuit Architectures for Portable Wireless Communications

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ABSTRACT

Ultra-low-power implementations of radio-frequency integrated circuits are benefiting from rapid improvements in integrated circuit technology, circuit architecture techniques and wireless system innovations. Some of the key technological developments driving this field are discussed, in addition to new approaches for the realization of next generation wireless circuits and systems that dissipate very little dc power.

1. INTRODUCTION

A wireless radio-frequency receiver typically finds itself immersed in a sea of unwanted and potentially interfering signals - from cellular base stations to television transmitters, airport radars, etc. - and from that environment is able to pick out the unique desired signal, and reproduce and amplify it with near perfect fidelity. This incredible feat of modern engineering is often taken for granted by the user of the device, but represents nearly a century of accumulated engineering expertise and relentless refinement.

The use of these devices for portable applications introduces another dimension of performance requirements - that of *ultra-low-power* . Now, the radio-frequency device must operate from low-voltage batteries of limited energy densities and variable voltage. The ideal radio communicator would dissipate virtually no power, allowing for months or even years between recharges. These devices are composed of a combination of digital, mixed-signal, and radio-frequency circuits, that together perform all of the functionality required to communicate with great fidelity across the hostile wireless environment.

This paper will identify the key circuit architectural and system issues that are driving the development of next-generation ultra-low-power radio frequency wireless communications devices. The optimization of the dc power dissipation of the portable transceiver will require close collaboration between network architecture and transceiver design in order to realize the best performance.

2. BATTERY CONSIDERATIONS FOR PORTABLE WIRELESS DEVICES

Modern day battery technology represents a fundamental constraint on the lifetime of portable wireless communications devices. Whereas digital integrated circuit technology doubles in complexity every three years, and analog and A/D converter technology doubles in performance roughly every 8 years [1], battery technology doubles in energy density only every 35 years [2].

Typical considerations in battery use are the specific energy of the battery (in Wh/Kg), battery cell voltage (in Volts), and lifetime (in number of cycles). The well-known Nickel Cadmium (NiCd) batteries have typical cell voltages of 1.25V and specific energies of 60 WH/kg. Lithium Ion batteries have recently become more popular, and their specific energies are in the 90 Wh/Kg range, with typical cell voltages of 3.6V. Nickel Metal Hydride (NiMH) batteries are also popular, with specific energies slightly greater than those of NiCd batteries, with very similar cell voltages.

A typical portable device has an acceptable weight range of between 4-12 oz. for most handheld applications based on human factors studies [3]. Assuming that battery weight is restricted to less than 50% of the total device weight implies an upper limit on stored energy of approximately 10 WH for the foreseeable future. Early studies of energy usage show that typical personal communicators spend only a short amount of time - one hour per 24 hour day - in the "talk" mode, where the power dissipation is at its highest [4]. Another 2 hours is spent in the "listen" mode, and anther three hours is spent in the "standby" mode. During talk time, the radio-frequency power amplifier is transmitting roughly 600 mW to the antenna, but draws nearly 2.5 W from the battery due to its relatively low efficiency. The power drawn by the rest of the radio-frequency portion of the device is approximately 500 mW during the "standby" mode, so the total power dissipated by the radio-frequency portion of the device is approximately 5 WH - roughly 50% of the total energy available from the battery. As an example, a recently announced fully monolithic DECT receiver dissipated approximately 200 mW, of which 40 mW was consumed by the LNAs, 50 mW by the mixer/downconverter section, and the remaining 100 mW by the analog-to-digital converters and baseband filters [5].

There are several areas for improvement in battery life over the next decade. These include improved power amplifier power-added efficiency, reduced power dissipation for the low-noise amplifier/down-converter/up-converter portions of the transceiver, and migration to "micro-cell" and "pico-cell" architectures to reduce transmitted power requirements. These options will be explored in the next Sections.

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3. CIRCUIT ARCHITECTURES FOR LOW-POWER RADIO COMMUNICATIONS

3.1 Receiver Architectures for Low-Power Implementations

The previous Section illustrated the role that receiver implementation has on dc power dissipation. The classical superheterodyne receiver - despite its manifest advantages - is not well suited to the needs of mobile wireless communications. This is due to its need for multiple image rejection filters through the down-conversion process. By contrast, several alternative architectures are being investigated for lower power implementation in completely monolithic form, including Direct Down-Conversion receivers[6,7], Wide-Band IF Down-Conversion receivers [8], and subsampling receivers. Each has its own unique set of advantages and limitations.

A schematic diagram of a typical direct conversion receiver is shown in Figure 1. In this case, the intermediate frequency (IF) is at dc, and the in-phase and quadrature (I and Q) paths of the mixer contain the positive and negative frequency components of the desired signal. The advantages of this particular architecture are that it is uniquely well suited to monolithic integration, due to its lack of image filtering, and its intrinsically simple architecture. FSK modulated signals are especially well-suited to Direct-Downconversion, due to their low-signal energy at dc [9].

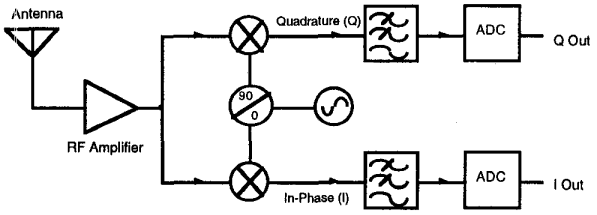

Figure 1. Block diagram of direct down-conversion receiver.

However, the direct conversion receiver has not gained widespread acceptance to date, especially in high performance wireless receivers, due to its intrinsic sensitivity to dc offset problems, even-order harmonics of the input signal that interfere with the desired signal, and local-oscillator leakage problems back to the antenna. These issues are all being actively pursued by a variety of world-wide research groups.

The subsampling receiver, shown in Figure 2, represents the "ultimate" example of simple low-power downconversion - consisting of essentially a sampling switch clocked at much lower frequency than the carrier frequency, and an A/D converter. But the limitations of the approach demonstrate some of the inherent problems in low-power receiver implementations. In a sub-sampling receiver, image frequencies exist at integral multiples of the sampling rate, and can alias into the band of interest. As a result, careful filtering prior to down-conversion is required. For example, downconversion of the 25 MHz bandwidth of a typical cellular frequency band would require a sample rate of at least 50 MHz, assuming a "brick-wall" bandpass filter. In practice, the sample rate will have to be much higher - at least 100 MHz- in order to minimize the finite bandwidth effects of the filter. A typical dynamic range requirement of 80 dB, would result in at least a 14-bit/100 MHz A/D converter - a clear impossibility in today's technology.

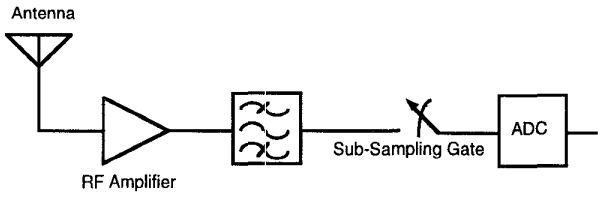

Figure 2: Simplified block diagram of sub-sampling receiver.

In addition, the resulting signal-to-noise ratio of the down-sampled signal will inevitably be poorer than that of an equivalent system employing a mixer for downconversion, due to the noise aliased from the bands between dc and the passband. The resulting signal-to-noise ratio is given by [10]

$$SNR_{sampled} = \frac{Signal}{N_p + (n-1)N_o} \qquad (1)$$

where n is the over-sampling ratio (approximately $f_{signal}/f_{bandwidth}$), S is the spectral power density of the signal, N_p is the in-band noise power density and N_o is the out-of-band noise power density.

If N_p and N_o are roughly comparable, then the degradation in the signal-to-noise ratio is roughly 10log(n) - a significant penalty. In the case of mobile wireless environments, such as digital cellular or PCS, such a degradation would prove to be unacceptable. However, the direct-sampling approach has recently proved popular for GPS receivers, where channel bandwidths are narrower, and out-of-band interference is less likely [11].

3.2 Power Amplifier Architectures for Improved Transmitter Efficiency

Another key aspect of the reduction of dc power in a wireless transceiver is migration towards more efficient linear power amplification techniques at the crucial interface to the antenna. This is especially important because the power amplifier operates at an *effective* power-added efficiency of less than 30% typically, although the *peak* power-added efficiency may be substantially higher. This reduction is due in part to the time varying output power requirements of a typical handset as it moves through the cellular environment [12]. Power amplifier architectures that maintain high power-added efficiency across widely varying output power will exhibit the best performance in this respect.

Another important issue for power amplifiers is the linearity of the amplifier when operated under peak output power conditions. The tradeoff between amplifier linearity and

power-added efficiency is a particularly difficult one, especially for non-constant envelope schemes such as QPSK and QAM. Several approaches are being examined for improved power amplifier linearity and efficiency. These include envelope elimination and restoration [13], Cartesian Feedback [14], and pre-distortion [15]. A block diagram of an envelope elimination and restoration circuit [13] appears in Fig. 3. Envelope elimination and restoration is especially attractive for mobile applications, since it promises simultaneous linearity *and* high efficiency under wide variations in output power.

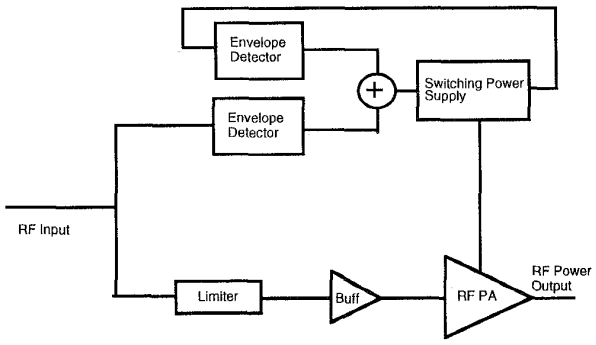

Figure 3. Block diagram of envelope elimination and restoration power amplifier [13].

3.3 Alternative Circuit Approaches for Wireless Communications

The preceding sections illustrate the circuit research directions currently being pursued for low-power implementations of radio transceivers. Are there any new, more speculative, approaches that offer the potential for dramatically lower dc power dissipation?

Chaotic electronic oscillators have been demonstrated to "auto-synchronize" under appropriate conditions, and several researchers have proposed secure, wideband, digital communications systems that take advantage of this effect [16,17]. The potential advantage with this approach is that the oscillators themselves can operate in a highly non-linear, and hence power efficient, mode, potentially eliminating the inherent problems associated with non-linear power amplifier linearity outlined in the previous Section. In addition, carrier synchronization is potentially achieved using a relatively simple and low-power circuit implementation [18]. Some of the important issues to resolve are synchronization across a band-limited, dispersive channel [19] , and synchronization sensitivity to parameter mismatch effects [20].

4. NETWORK DESIGN ISSUES FOR IMPROVED LOW-POWER RF TRANSCEIVERS

One of the key requirements for extended battery life is the extension of the cellular environment to micro-cells and pico-cells in high density areas [21]. Smaller cell sizes inevitably lead to lower transmitted power, and thus lower power dissipation during "talk" times. In addition, the performance requirements on the receiver LNA are also greatly reduced. There appears to be no fundamental lower limit to handset power dissipation as the cell sizes continue to shrink. An example of this approach is the Japanese PHS system where the typical handsets have a six hour talk time and 200 hour standby time - a significant improvement over cellular telephones in the United States. This increase in talk time results from the micro-cellular environment and simplified system architecture, which reduces transmitted power from 600 mW for a typical AMPS telephone to approximately 80 mW.

In the limiting case, personal communications networks could be limited to a distance of a few dozen feet, and transmitted powers could be less than 1 mW. An example of such a system is the BBN BodyLAN™ project, where the portable communication device is intended to be worn, and communicates at rates of up to 90 kB/s over a range of 6-10 feet [22] are expected. The static power dissipation of the device is intended to be approximately 10 μW, with an energy dissipation of 10 nJ per bit.

Other refinements are possible, and are being actively explored for improvements in the power dissipation of the radio portion of the portable communications device. The first, and most obvious, are active power management techniques, whereby the dc power delivered to the device depends on its performance requirements at any given time. All of the critical devices are either turned off when not needed, or powered down to achieve a lower power dissipation when the best performance is not required.

This is done today for power amplifiers, where the transmitted power is updated on a continuous basis to maintain a constant signal-to-noise ratio at the receiver. Further improvements in power management techniques are also possible. Low-noise amplifiers can be powered down under conditions where the absolute lowest noise figure is not required. Voltage controlled oscillators could also be operated at lower powers in cases where reciprocal mixing due to strong interferes is not an issue. These conditions can all be determined in the digital signal processing portion of the transceiver, and the radio circuits can be altered under computer control. Other areas of possible improvement include continuous variation in data rates to minimize dc power dissipation [23], and networking protocol variations to minimize dissipated dc power [24].

For example, Motorola has extended the battery life of their FLEX pagers significantly through the use of improved protocols [25]. In this case, the intermittent receiving ratio - a measure of the percentage of time required in the "listen" mode - dropped from 1:6.4 in the popular POCSAG system to 1:112. This allowed for a dramatic drop in the dc power dissipation of the device. The case of a "receive-only" system like a pager is admittedly a special case, but this does demonstrate how improvements in the network layer can improve overall battery life.

5. SUMMARY

Next generation broadband wireless communication devices will encounter a fundamental limitation imposed by the relatively modest improvements achievable in battery technology. As a result, new circuit and network architectures will be required to achieve increased data rates and battery life. These improvements will involve improved transceiver architectures, and improved network designs that take advantage of the power savings capability of these architectures.

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