Integrated Circuit Technology Options for RFIC's—Present Status and Future Directions

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***Abstract*—This paper will summarize the technology tradeoffs that are involved in the implementation of radio frequency integrated circuits for wireless communications. Radio transceiver circuits have a very broad range of requirements—including noise figure, linearity, gain, phase noise, and power dissipation. The advantages and disadvantages of each of the competing technologies—Si CMOS and bipolar junction transistors (BJT's), Si/SiGe HBT's and GaAs MESFET's, PHEMTS and HBT's will be examined in light of these requirements.**

***Index Terms*—CMOS RF, low-noise amplifiers, monolithic radio architectures, radio receivers, wireless communications.**

I. Introduction

THE explosion of interest in radio frequency integrated circuits (RFIC's) in the last decade has been driven by the expansion of the market for untethered communications in a variety of forms—from pagers and cordless telephones to analog and digital cellular telephones and personal communication systems (PCS's). In addition, the introduction of Ku-band direct-to-home (DTH) satellite television services have created an enormous market for "wireless" transmission of digital video signals using MPEG standards. Together, these developments have created a rapidly expanding market for RFIC's that was previously dominated by the relatively slow-growing military and cable television industries. The technical requirements imposed on these transceiver components are truly challenging.

A wireless radio-frequency receiver typically finds itself immersed in a sea of unwanted and potentially interfering signals—from cellular base stations and television transmitters to airport radars—and from that chaos is able to pick out the unique desired signal and reproduce and amplify it with near perfect fidelity. This incredible feat of modern engineering is often taken for granted by the user of the device, but represents nearly a century of accumulated engineering expertise and relentless refinement.

At the same time, the consumer nature of this market puts a premium on low-cost/low-power/high-volume implementations of radio functions that were formerly implemented using bulky, expensive, and power-hungry hybrid components. Drawing an analogy to digital integrated circuit technology, it would appear that the optimum technology choice for RFIC applications might follow the same path that digital IC implementations followed—toward CMOS—with costs dropping dramatically as the level of integration increases. IDC predicts that the total semiconductor content of a typical cellular handset will actually decrease from an average of $76 today to less than $58 by the year 2000, primarily because of higher levels of CMOS digital integration [1]. It could plausibly be argued that the radio functions of the transceiver should follow a similar technology path, resulting in a highly integrated "single-chip CMOS radio" sometime in the future, in the same spirit that single-chip CMOS digital signal processors exist today.

However, the technical requirements for the transceiver function of a typical wireless device are considerably more multidimensional than that of a digital integrated circuit—where power dissipation, speed, and yield are the major performance metrics, and where performance inevitably improves with increasing lithographic sophistication and higher levels of integration. In addition to those performance requirements of digital circuits, RFIC's have to contend with issues of noise—both broadband and near carrier—linearity, gain, and efficiency. As a result, the optimum integrated circuit technology choices for RF transceivers—in terms of optimum devices and levels of integration—are still evolving. In fact, engineers planning to implement wireless transceivers are confronted with a baffling variety of possibilities: silicon CMOS, BiCMOS, and bipolar technologies, GaAs MESFET, heterojunction bipolar transistor (HBT), and PHEMT, as well as discrete filters. Recent commercial implementations of highly integrated high-performance wireless transceivers typically utilize a mixture of these technologies in order to implement a complete system.

This paper will begin with a review of radio-frequency transceiver architectures for wireless communications, with particular emphasis on existing technology tradeoffs in each of the critical areas of system implementation. It will then follow with a review of each of the critical building-blocks for implementation of a wireless transceiver in the 2-GHz range, where many new system opportunities are emerging, and the technology advantages and disadvantages will be discussed. Finally, there will be some elaboration on "emerging" technologies in the wireless area that may have significant impact on future system design.

II. System Requirements for RFIC's

The radio frequency transceiver for a digital cellular handset (IS-54/IS-136), whose simplified block diagram is shown in Fig. 1 [2], represents a first-generation digital cellular standard, and is a good example of a typical "high-tier PCS" application

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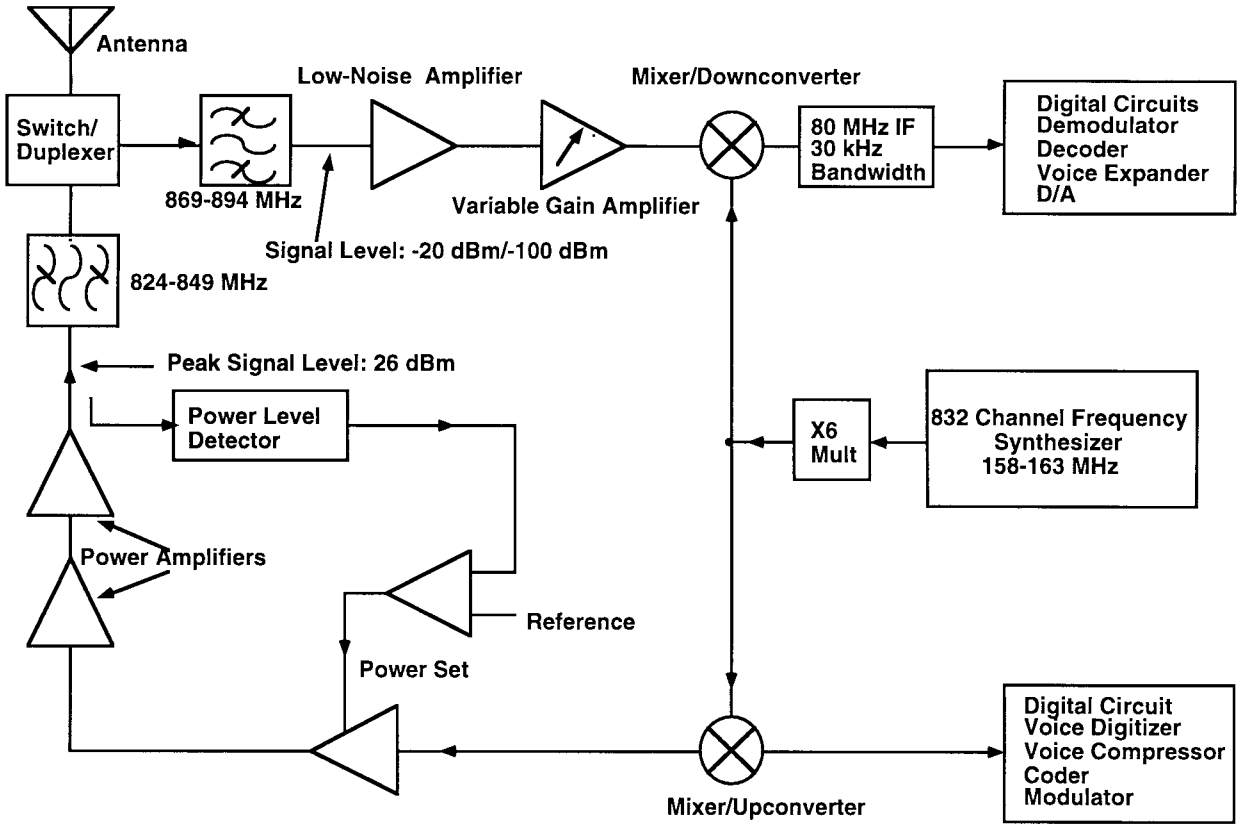


Fig. 1. Simplified block diagram of RF portion of IS-54/136 transceiver [2].

[3]. Other examples of high-tier PCS include IS-95, GSM, and DCS-1800. The transmitter portion of the RF unit operates from 824 to 849 MHz, and the receiver portion operates from 869 to 894 MHz, which are the standard frequencies for operation in the United States.

The receiver in this system has to accommodate a variety of technical challenges. The carrier frequency is roughly 880 MHz, but the signal frequency itself occupies less than 30 kHz of bandwidth. The receiver must therefore select this 30-kHz signal from all of the other cellular signals, which occupy approximately 25 MHz, and all of the other competing signals in the environment, which can occupy considerably greater bandwidth. So the difference in frequency ranges between the desired signal and potentially interfering undesired signals is less than 10^{-3}.

Based on considerations of cell size, transmitter power, expected path loss, and bandwidth, the total receiver noise-figure requirements are typically 3 dB or lower. This level of performance can be achieved by a variety of technologies, from GaAs MESFET to silicon bipolar and even potentially CMOS. The first stage low-noise amplifier (LNA) has the greatest effect on the overall receiver noise figure, and a noise figure of less than 3 dB is typically required. At the same time, the received in-band signal power can vary from less than -100 dBm to greater than -20 dBm, so the dynamic range requirements of the receiver are very challenging. Out-of-band interferers from a variety of potential sources can raise the received power to even higher levels; hence the need for a sharp bandpass filter from 869 to 894 MHz to minimize out-of-band interference.

The transmitted power from the handset power amplifier can rise as high as 23 dBm, although the power amplifier is typically designed for a peak power of 30 dBm or even higher, and then backed-off by 7 dB in order to maintain the required linearity. Another high-Q bandpass filter is provided at the output in order to conform to FCC requirements on out-of-band radiated emission. Spurious performance is typically required to be 60 dB below the carrier in this system. The power amplifier will ideally maintain a high gain, linearity, and power-added efficiency over the entire bandwidth and output power range when operated from a 2.7-V battery power supply. Typical peak power-added efficiencies are in the 50% range for standard handheld telephones. The final power output stage is typically implemented in silicon MOS, GaAs MESFET, or HBT technology.

The frequency synthesizer produces the local oscillator for upconversion/downconversion and is typically produced by a low phase noise voltage controlled oscillator (VCO) that is locked to a lower frequency crystal reference. The phase noise of the VCO is a crucial parameter because channel-channel spacing is only 30 kHz in this system, and reciprocal mixing of adjacent channels can significantly degrade the received carrier/noise (C/N) performance. In addition, the sidebands of the VCO phase noise add directly to the noise floor in the system passband, further degrading the C/N [4]. A typical requirement is that the C/N be at least 7 dB for a bit error rate of 10^{-3}. This in turn requires that the oscillator phase noise be at least -100 dBc/Hz at 100 kHz from the center frequency. These ambitious phase noise requirements will in turn present very stringent requirements on the noise and

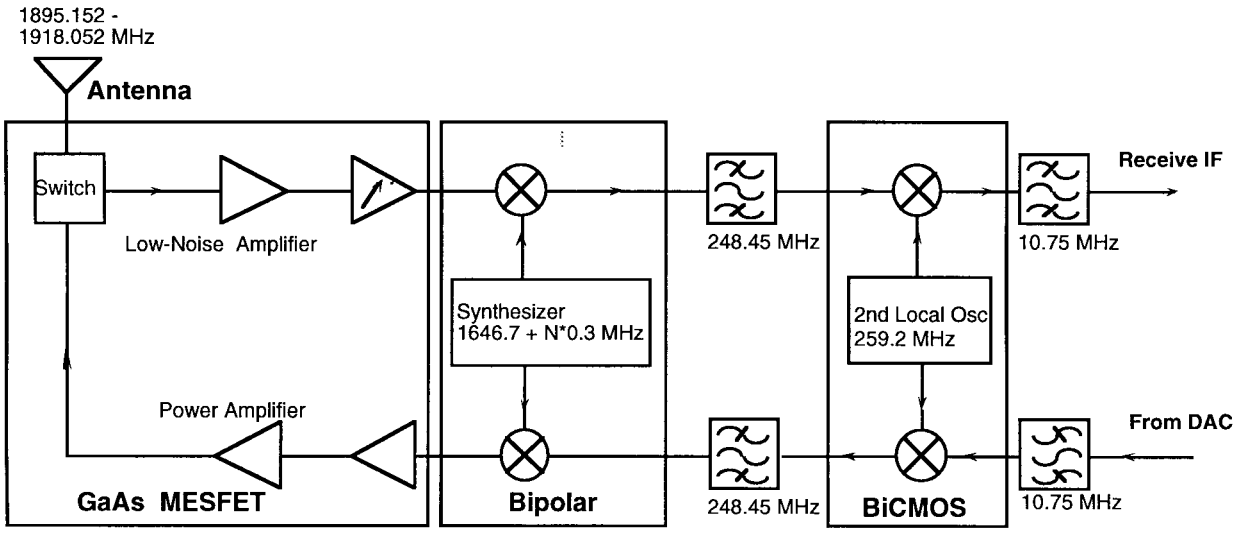


Fig. 2. Simplified block diagram of PHS transceiver [5].

gain of the semiconductor technology used to implement the VCO.

The previous example demonstrated the design tradeoffs involved in the RF section of a "high-tier PCS" application. "Low-tier PCS" applications can benefit from considerable simplification of the RF portion of the handset, although there is a penalty paid in lower range and quality of service. Cordless telephones are an example of a "first generation" low-tier PCS system, but more recent implementations of second generation systems include personal communications services (WACS/PACS), personal handyphone system (PHS/PHP), and digital enhanced cordless telecommunications (DECT). The Japanese personal handyphone system (PHS) is an excellent example of a highly popular low-tier system. It was launched in July of 1995, and by the end of the summer of 1996 there were over three million subscribers. The cost for a three-minute call is roughly ten cents, and the typical handsets have a six-hour talk time and 200-hour standby time. The system was designed for mostly pedestrian use, and so there is very limited hand-off capability as the user moves from one cell to another.

Fig. 2 is an example of a commercially available PHS RF architecture [5]. The PHS system operates over a 23-MHz band from 1895 to 1918 MHz, with carriers spaced 300 kHz apart. Each carrier supports four channels employing time domain duplexing (TDD) and time domain multiple access (TDMA). The use of TDD allows for the same frequency to be used for both transmit and receiver IF, which permits the sharing of certain IF filters and minimizes system complexity. The synthesizer output frequency is an integral multiple of 300 kHz, which allows it to operate directly with a 300-kHz reference signal. This improves the switching time of the phase locked loop (PLL), compared with the high-tier PCS system discussed previously that operated at 30-kHz intervals. One potential problem with this architecture—feedthrough of the transmit carrier to the receiver—is eliminated by disabling the digital transmit samples during the receive periods. In fact, the measured transmitter "off" leakage is approximately -60 dBm, compared to a transmit "on" power of approximately 20 dBm.

The RF portion of the chip-set consists of an analog BiCMOS IF IC, which converts the digital samples to an IF carrier at 248 MHz, a silicon bipolar frequency synthesizer that generates the local oscillator signal for the final upconversion, and two GaAs MESFET ICs—one that upconverts from 248 MHz to 1.9 GHz, and the other that contains the power amplifier, LNA, and switch. Because of the small PHS cell size, the peak output power of the power amplifier is roughly 100 mW—considerably less than a typical cellular system. The smaller cell size also reduces the worst case path loss somewhat, easing the dynamic range requirements on the receiver.

The partitioning of the differing technologies in this system is fairly representative of current techniques, where GaAs MESFET technology is employed for the high-performance areas near the antenna (switch, low-noise, and power amplifiers), silicon bipolar technology is employed for the frequency synthesizer portion because of its low phase noise capabilities, and BiCMOS is used for higher levels of integration in a mixed-signal environment.

These two transceiver architectures are examples of traditional heterodyne and superheterodyne approaches, where off-chip passive filters have been used for "roofing" and image rejection purposes. These filters represent the major impediment to raising the level of integration of wireless radios, since they cannot be easily implemented monolithically. Substantial progress has made recently in the area of *direct downconversion* approaches for wireless receivers, which eliminate the need for image rejection filters and are better suited to fully monolithic integration. However, direct conversion receivers have some unique problems as well, including sensitivity to dc offsets and second-order distortion. An excellent review of recent research in this field is presented in [6] and [7].

III. Technology Considerations for RFIC Implementation

The optimum technology choice for an RF application is complicated by issues of performance, wafer cost, level of

TABLE I
COMPARISON OF FUNDAMENTAL MATERIALS PROPERTIES OF SILICON AND GaAs SEMICONDUCTOR TECHNOLOGY

Properties	Silicon	GaAs
Breakdown Field (V/cm)	≈3x10^5	≈4X10^5
Electron Mobility (cm^2/V-sec)	≈1500	≈8500
Thermal Conductivity at 300°K (watt/cm-°C)	≈1.45	≈0.45
Saturated Electron Drift Velocity (@10^{5}V/cm)	≈10^7	≈10^7
1/f Noise Corner Frequency (Hz)		
BJT/HBT	10-10^3	10^4-10^6
MOSFET/MESFET	10^3-10^5	10^6-10^8
Substrate Resistivity (typical) (Ω-cm)	≈10^3	≈10^8

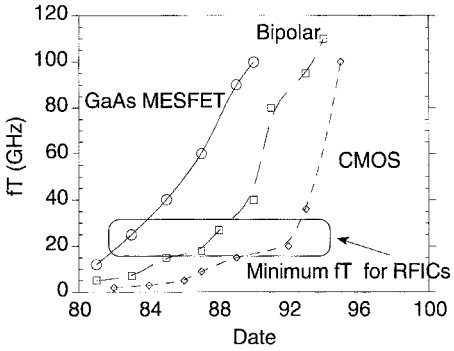


Fig. 3. Reported transistor cutoff frequency versus time [8]. Note that all silicon technologies are now capable of addressing applications in the 1–2 GHz regime.

integration, and time-to market. As mentioned earlier, the performance issue is very multidimensional in the RF area, because of the differing requirements for the various building blocks. These differing requirements often lead to a mix of technologies for the implementation of state-of-the-art radios, as was demonstrated in the previous section.

Until recently, GaAs technology was expected to dominate the RF integrated circuit arena because of its intrinsically higher speed due to its improved electron mobility and saturated drift velocity. Table I summarizes the relative differences of the intrinsic materials properties of silicon and GaAs, with particular attention to differences that are key for radio-frequency applications. Based on the materials properties alone (low-field electron mobility and energy band-gap in particular), GaAs is clearly superior for high-frequency device applications. This is confirmed by the fact that the *highest* performance components of microwave receivers—such as 0.6-dB noise figure Ku-band DBS downconverter LNA's—are inevitably implemented in GaAs MESFET or PHEMT technology [8]. However, as Fig. 3 demonstrates, the transistor unity current-gain frequency (f_T) of silicon technology has recently reached the level where it is comparable with GaAs for applications in the 1–10 GHz frequency range [9]. At very short gate lengths (roughly below 0.2 μm), the saturated drift velocity of the electrons dominates the f_T, and transistors fabricated in silicon and GaAs technologies have comparable cutoff frequencies, albeit at higher voltage levels with the silicon-based devices [10].

Despite their roughly comparable production f_T's, GaAs (or InP)-based technologies will continue to maintain a small but significant *absolute* performance advantage due to the higher low-field mobility, which has a major impact on device noise figure [11]. The ohmic resistances leading to the device, which play a major part in determining noise-figure, are dominated by low-field electron mobility, and the metal-gate structure of a typical GaAs MESFET or PHEMT reduces the series gate resistance compared to that of a silicided MOSFET gate. However, recent results have demonstrated that a "T-gate" aluminum structure in MOS technology can realize gate resistance values comparable to those of GaAs MESFET's or PHEMT's [12]. In many cases, even a few tenths of a decibel difference in noise figure is significant for wireless applications, especially in a base station or satellite receiver, because reductions in noise figure can translate directly into equivalent reductions in the transmit power requirements.

This improvement in performance means that silicon technology has comparable performance capabilities to GaAs technology at wireless communications frequencies. However, as demonstrated above, the peak cutoff frequency of the transistor does not paint a complete picture of performance, since the high-frequency performance of the silicon devices is generally achieved at higher power dissipation levels than GaAs devices. However, the higher levels of integration possible with silicon technology may reduce the need for routing high-frequency signals on- and off-chip, compared with GaAs technology, reducing overall *system* power dissipation.

Parasitic coupling between adjacent sections of a high-frequency RF integrated circuit presents a vexing practical problem for the designer of a highly integrated radio transceiver. It places a practical upper limit on the achievable gain of a circuit—due to the potential for oscillation—and can also result in oscillator "injection locking" in cases where the final high-power output amplifier stage shares a common substrate with the frequency synthesizer/VCO [13]. This coupling can occur through parallel substrate conduction paths [14] or through the mutual inductance and capacitance of the package leads [15].

The former effect is especially a problem in monolithic silicon technology, because of the relatively low substrate resistivity. It has been addressed through a variety of process techniques including guard rings [16], a variety of silicon-on-insulator (SOI) techniques [17], and silicon-on-sapphire (SOS) [18]. Furthermore, careful attention to appropriate circuit design, including the use of fully balanced signal paths, can alleviate the problem significantly. By comparison, GaAs technology exhibits a greater degree of circuit–circuit isolation at high frequencies, due to the semi-insulating nature of the substrate.

The next several sections will illustrate some of the technology considerations involved in the implementation of key wireless system building blocks.

A. Low-Noise Amplifiers

LNA's are one of the key performance bottlenecks in an RF system. They are required to contend with a variety of signals coming from the antenna—often of larger amplitude than the desired signal—and so both low noise and high linearity are simultaneously required. Two measures of these requirements are the amplifier noise figure, which determines the minimum detectable signal (MDS), and the third-order input intercept point (IIP3), which, together with noise figure, determines the spur free dynamic range (SFDR). The SFDR determines the difference between the MDS and the maximum input signal prior to significant distortion [19]. In addition, high gain and low dc power consumption are other requirements of an LNA.

A very simplified expression for transistor minimum noise figure, which is applicable to both bipolar junction transistors (BJT's) and FET's, is given by [20]

$$\text{Noise Figure} \approx 1 + k g_m r_{b/g} \left(\frac{f}{f_T} \right)^2 \tag{1}$$

where g_m is the device transconductance, $r_{b/g}$ is the base or gate resistance, depending on whether the device is a bipolar transistor or FET, and k is a material dependent constant. Clearly, the noise figure of the amplifier will be improved by employing a technology that operates with as high an f_T and as low a base or gate resistance at a given current as possible. As a result, technology scaling will have a significant impact on low-noise amplifier performance, but care must be taken to minimize the access resistances $(r_{b/g})$ to the device at the same time the transistor cutoff frequency is raised. It is this later $r_{b/g}$ factor that provides the performance advantage of GaAs-based devices.

Fig. 4 plots amplifier gain/dc power dissipation (in dB/mW) as a function of noise figure (in dB) for a variety of reported low-noise amplifiers in silicon and GaAs technology at 2 GHz. Care must be exercised in comparing reported circuit performance, since it represents an intermingling of intrinsic device performance, process features, and circuit design. Nevertheless, by comparing the *best* reported results in each technology, the fundamental device performance limits can be assessed. Most of the recently reported LNA results, fabricated in Si CMOS [21], or Si bipolar technologies [22], [23] fall along a gain/(Pdc·NF) line of approximately 0.4 (1/mW). By comparison, a recent SiGe HBT result [24] demonstrated a fully integrated LNA with 0.95 dB noise figure, 2 mW of power dissipation, and 10.5 dB of gain at 2.4 GHz, for a figure of merit of approximately 5.5 (1/mW). The best reported GaAs LNA's have figures of merit of approximately 3.0 (1/mW) [25]–[27]. These results demonstrate the potential performance advantage of advanced GaAs or SiGe technologies at these frequencies, if dc power dissipation is a major consideration.

Because of the extreme dynamic range considerations of the low-noise front end, linearity is an equally important figure-of-merit for LNA's. In this case, a linearity figure-of-merit is the ratio of the input third-order intercept point (IP3) to the dc power dissipation. Field-effect transistors (MOSFET's as well as GaAs MESFET's and PHEMT's) generally exhibit improved third-order intermodulation distortion compared with bipolar devices, due to their near square-law current versus voltage behavior. On the other hand, bipolar transistor amplifiers have recently demonstrated outstanding linearity performance as well, apparently due to the partial cancellation of the resistive and capacitive nonlinearities in the base-emitter junction at certain frequencies [28]. Fig. 5 compares this linearity figure-of-merit for a variety of recently reported monolithic low-noise amplifier circuits, all operating at approximately 2 GHz. As with the case of noise figure, the performance advantages of SiGe and GaAs technologies are significant if dc power dissipation is a critical parameter, although the improvement is less dramatic. Part of the reason for this is the improved intermodulation performance of FET's. The best amplifier results have a ratio of IIP3/dc power of approximately 0.10.

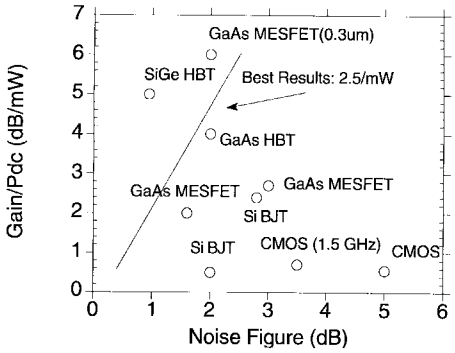


Fig. 4. Gain-to-dc power ratio plotted versus noise figure for state-of-the-art 2-GHz LNA's. The best results have a figure-of-merit of approximately 2.5/mW [21]–[27].

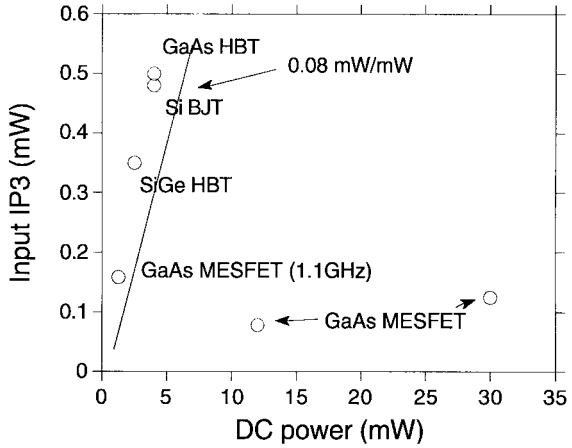
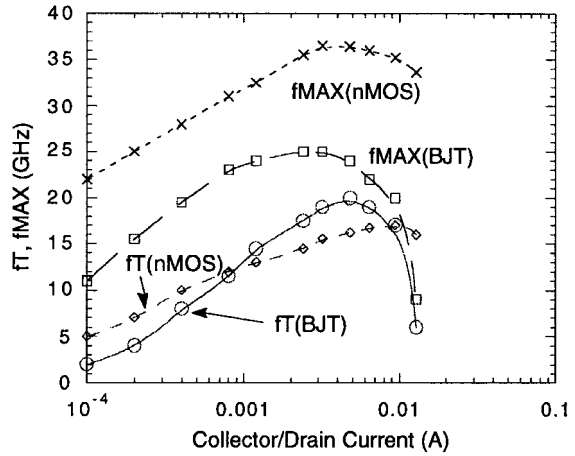
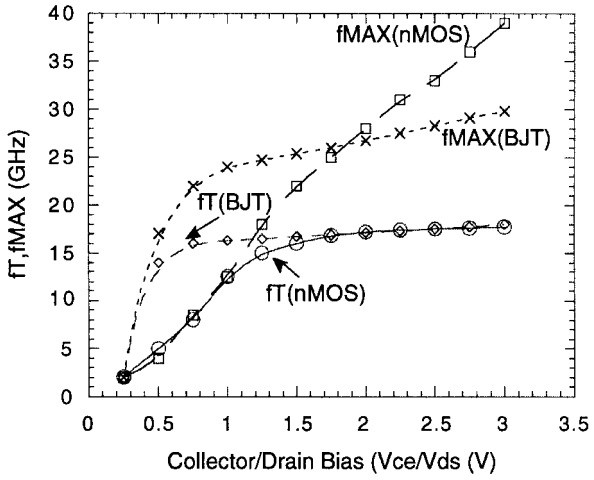


Fig. 5. Amplifier linearity figure-of-merit plotted for the same monolithic 2-GHz amplifiers of Fig. 4. The best results fall on a line of approximately 0.08 mW/mW [21]–[27].

The tradeoff between the use of silicon bipolar and MOS devices for LNA applications is also complicated by a number of factors. As a representative example, a 0.5-μm NMOS device exhibits a peak f_T and f_{MAX} of approximately 20 and 40 GHz, respectively [29]. By comparison, the peak f_T and f_{MAX} of npn bipolar devices fabricated in a comparable process is 20 and 28 GHz, respectively. The improved f_{MAX} of MOS devices, and hence higher microwave gain, is pri-



(a)



(b)

Fig. 6. Measured high-frequency performance of Si BJT and NMOS devices. (a) f_T and f_{MAX} versus collector/drain current. (b) f_T/f_{MAX} versus collector/drain voltage [29].

marily attributed to the lower gate resistance compared to the base resistance of a bipolar device. MOS devices exhibit a substantial speed advantage at low currents compared to bipolar devices, but bipolar transistors exhibit better performance at low voltages. This is illustrated in the f_T and f_{MAX} curves of Fig. 6 [29].

When properly scaled for width and normalized for f_T and power dissipation, MOS devices exhibit a slightly lower minimum noise figure than bipolar devices, but their associated optimum source resistance is much farther from 50 Ω (close to an open- circuit because of the low equivalent input noise current), making optimum low-noise impedance matching difficult. The optimum source impedance can be moved closer to 50 Ω in a MOS device, but only at the expense of increased power dissipation or noise figure.

Circuit design improvements combined with the availability of optimized monolithic components can also yield improved performance in many cases. As an example, the SiGe HBT LNA of [24] (see Fig. 7) utilized a monolithic transformer feedback structure in order to optimize power dissipation, input return loss, and noise figure. The availability of high-quality

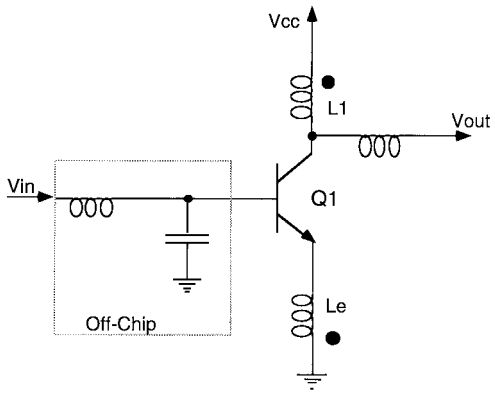


Fig. 7. Schematic of SiGe HBT low-noise amplifier with monolithic transformer coupling [24].

inductor structures combined with the high-performance of the SiGe HBT technology resulted in outstanding performance at extremely low power dissipation.

B. Power Amplifiers

The complications associated with power amplifiers for RF applications are at least as challenging as those associated with low-noise amplifiers. The circuit must simultaneously satisfy requirements of linearity, gain, output power, and power-added efficiency. In addition, the trend toward lowered power supply voltages (from 5 V to 3 V and even lower), has made it difficult to maintain the required output power and efficiency due to impedance matching limitations. Finally, the power amplifier must deliver a wide range of output powers to the antenna, as the user moves throughout the cell site. Ideally, the power-added efficiency of the amplifier should not degrade significantly as the output power varies from near zero to its maximum value.

One of the major dilemmas in wireless systems is that power amplifiers are typically operated in a "backed-off" mode relative to their peak power and power-added efficiency points in order to meet the linearity requirements of the system. The degree of back-off varies depending on the modulation scheme employed—0 dB for Gaussian-filtered minimum shift keying (GMSK) (GSM and DECT), 7 dB for Pi/4DQPSK (IS-54 and PHS), 10 dB for QPSK (IS-95), and 12 dB for 16QAM are typical. In this sense, constant envelope modulation schemes like GMSK have distinct advantages for power amplifier performance—since they can operate at near peak efficiency. However, there is a significant penalty paid with constant envelope modulation in terms of the spectral efficiency (in (b/s)/Hz) compared with the other modulation approaches.

In digital communications systems, the linearity of the output power amplifier—which determines the required back-off—is usually specified as an adjacent channel power ratio (ACPR) in dBc, rather than the more traditional IIP3/IIP5 used in analog communications applications. ACPR is a measure of the spectral "spill-over" due to amplifier nonlinearities into an adjacent frequency band by a digitally modulated waveform. Fortunately, the two measures are closely related, and a useful expression for the required IP3 in terms of specified ACPR for

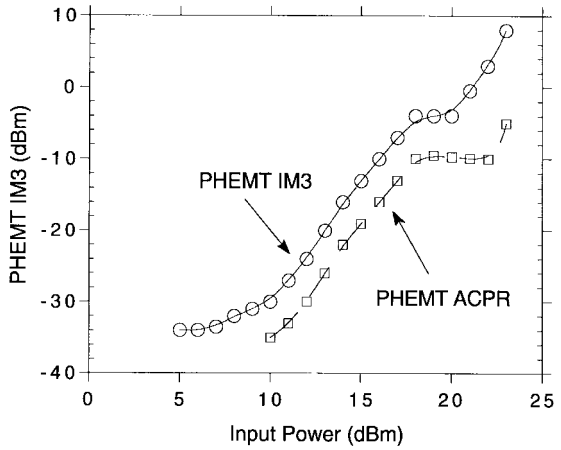


Fig. 8. Comparison of third-order IM power and adjacent-channel power for GaAs PHEMT [31]. Note that IM3 and ACPR track each other over a broad range of input power levels.

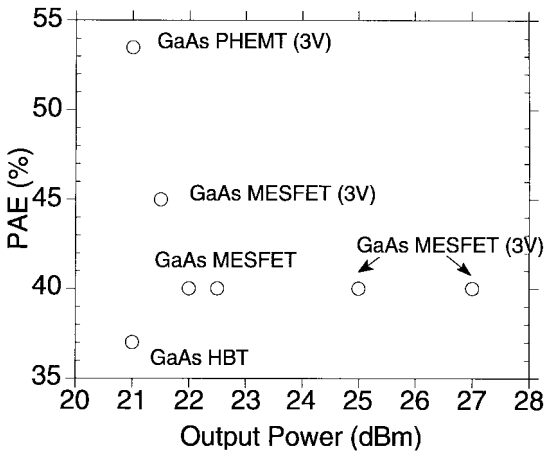


Fig. 9. PHS/PACS power amplifier performance for ACP <-55 dBc at 600 kHz offset [75]–[80]. The best performance is obtained with a GaAs PHEMT.

a CDMA system was recently derived [30] and is given by

$$\mathrm{IP3} = -5\log\left[\frac{P_{\mathrm{IM3}}(f_1,f_2)B^3}{P_o\left[(3B-f_1)^3-(3B-f_2)^3\right]}\right]+22.2 \quad (2)$$

where IP3 is the required output third-order intercept point in dBm, B is one-half of the signal bandwidth, f_1 and f_2 are the out-of-band frequency limits, P_o is the output power of the amplifier, and $P_{\mathrm{IM3}}(f_1,f_2)$ is the out-of-band specified power. This expression assumes that only third-order nonlinearities determine out-of-band power, although it can be used with some modifications for examining the effects of higher order nonlinearities as well. Experimentally, it has been demonstrated that the IM3 and ACPR track each other closely as predicted by (2), and as the data in [31] demonstrates (see Fig. 8).

Power amplifiers are typically operated in the Class-AB mode for most RFIC applications in an attempt to achieve a compromise between linearity and power-added efficiency. In this case, the factors of key importance for amplifier performance are transistor f_{MAX} (for high power gain), linearity (for lowest possible adjacent channel interference), and breakdown voltage (BVCEO for bipolar devices or BVGDS for FET's). As it turns out, the breakdown voltage has become less critical for handsets in recent years, due to the reduction of operating voltages in most handheld units. The power-added efficiency of a power amplifier is given by the well-known expression

$$\mathrm{PAE} = \frac{\eta}{1-1/G} \quad (3)$$

where η is the collector/drain efficiency—which typically varies from 40 to 75%—and G is the amplifier power gain. Since gain is so critical to achieving the best performance, most high-performance power amplifiers in the 2-GHz frequency range have been implemented in GaAs technology to achieve the highest possible power-added efficiency. At lower frequencies, silicon MOS devices are often employed for power amplifiers because of their low-cost and robust operation, despite their poorer performance compared to GaAs technology. Fig. 9 summarizes a recent comparison of monolithic power amplifier performance for PHS applications at 1900 MHz, where the adjacent channel leakage specification of -55 dBc is specified at 600 kHz from the carrier center [32]. The best results are achieved with 0.25-μm GaAs PHEMT technology, probably due to its higher f_T and f_{MAX} (50 and 90 GHz, respectively) compared with GaAs MESFET technology. The resulting differences are not dramatic however, and the higher current and power gain of the PHEMT device at these frequencies may only translate into modest improvements in power-added efficiency at a given output power.

Experimental results from several other promising candidate power amplifier technologies are not presented in Fig. 9, due to an incomplete specification of adjacent channel power performance. An SiGe HBT recently demonstrated an output power of 23 dBm at 1.9 GHz and power-added efficiency of 37% under two-tone operation, with a resulting third-order intermodulation product of -30 dBc [33]. A completely integrated RF MOS power amplifier achieved 56% power-added efficiency and 1.5 W output power, with a power supply voltage of 5.8 V at 850 MHz [34].

As with low-noise amplifiers, despite their high f_T, the peak performance of silicon-based devices will lag that of GaAs devices for the foreseeable future, even at lower power supply voltages. The well-known Johnson limit [35] for speed versus breakdown voltage in semiconductor devices results in significantly higher gain for the GaAs devices, even at the lower operating voltage, due to the higher electron mobility. The higher gain translates into improved power-added efficiency, and potentially linearity, at higher-frequencies of operation. Therefore, the *best* performance is usually obtained with GaAs power devices, and this will remain true for the foreseeable future. Care must be taken in the design of power amplifiers in low-voltage technologies, since the peak drain/collector voltage can approach four times the supply voltage under extreme voltage standing wave ratio (VSWR) conditions [36].

Power amplifier designs require that extraordinary attention be paid to issues of package parasitics, thermal impedances, and harmonic terminations [37]. Losses in interstage matching networks must be absolutely minimized, and

tradeoffs between linearity and power-added efficiency are usually achieved through optimum biasing and impedance matching. The high ratio of impedance matching with these devices usually requires an off-chip hybrid for maximum power-added efficiency. Monolithic GaAs technology has a distinct performance advantage compared to monolithic silicon implementations of power amplifiers, because of the ability to easily realize low-loss impedance matching structures on the semi-insulating substrate.

C. Voltage Controlled Oscillators and Frequency Synthesizers

The VCO represents one of the most difficult challenges for a design engineer. The ideal VCO output exhibits no phase noise, tunes over a fixed frequency range, and is insensitive to temperature, process drift, output loading, or power supply variations. Hybrid VCO's are available today that closely approximate this ideal and sell for fractions of a dollar in high volume [38]. They typically employ discrete silicon bipolar transistors, high-quality surface mount inductors and varactor diodes, and are temperature compensated and laser-trimmed to the proper center frequency. By contrast, a completely monolithic integrated VCO suffers from low-quality monolithic inductors (typical Q-factors are less than 20), relatively poor quality varactor-diodes [39], [40], and a difficulty in trimming the center frequency to accommodate its inevitable drift due to process variations.

The quality factor of the VCO resonator, which is mostly determined by the inductor in the resonator, is especially important due to its effect on the phase noise of the resulting oscillator. A simplified expression for oscillator phase noise, which gives good agreement with experimental data over a broad range of oscillator circuits, was derived by Leeson [41] and later extended by Scherer [42] to account for flicker noise

$$S_\phi(\omega_m) = S_{\Delta\theta}\left[1+\left(\frac{\omega_0}{2Q\omega_m}\right)^2\right]\left(1+\frac{\omega_c}{\omega_m}\right) \qquad (4)$$

where $S_\phi(\omega_m)$ is the output power spectral density at frequency ω_m offset from the oscillator center frequency, $S_{\Delta\theta}$ is the power spectral density of the oscillator input phase error (roughly $2FKT/P_s$, where F is the noise figure and P_s is the signal power), Q is the resonator loaded quality factor, ω_o is the center frequency of the oscillator output, and ω_c is the flicker noise corner frequency.

This result illustrates the importance of the resonator circuit for an oscillator, since the power spectral density drops as the square of the quality factor. Low-noise oscillators also require a large output amplitude and a low-noise amplifier in order to achieve the best performance. As a result, it is not expected that *technological* improvements will dramatically improve monolithic VCO phase noise at a given power dissipation for the foreseeable future, since inductor Q is relatively difficult to improve dramatically (see Section IV), and the transistor noise figure is already quite low. The only other control variable is signal power, which is directly related to dc power dissipation.

The difference between the performance of 2-GHz VCO's with internal and external resonators is illustrated in Fig. 10. Generally, the best performance is obtained from circuits employing external resonators, and phase noise tends to rise as dc power is reduced. However, it is expected that the performance of fully monolithic oscillators will continue to improve as various groups continue to develop improved circuit design techniques for this class of problem.

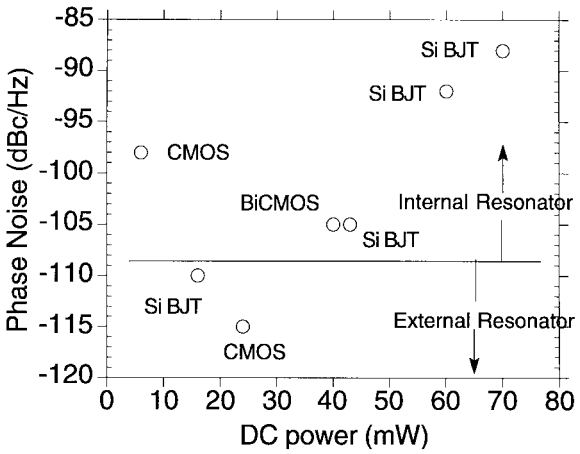


Fig. 10. Measured phase noise as a function of dc power for a variety of monolithic VCO circuits in the 2 GHz frequency range at an offset frequency of 100 kHz from the carrier [81]–[87]. The use of an external resonator provides the best noise performance.

Fig. 10 does not demonstrate any obvious trend in terms of optimum semiconductor technology for the realization of VCO's. Historically, silicon BJT's have been preferred for microwave oscillator applications because of their low levels of $1/f$ noise, which is especially important for narrow bandwidth applications and adequate gain at microwave frequencies. GaAs MESFET's have been used at higher microwave frequencies for *dielectric resonator oscillators* (DRO's), since the extraordinarily high Q of the dielectric resonator results in acceptable phase noise for many applications [43]. Si/SiGe HBT's exhibit equally good $1/f$ noise performance as Si BJT's [44], but with considerably more gain. A 7.5-GHz Si/SiGe monolithic microwave integrated circuit (MMIC) VCO demonstrated less than 100 dBc/Hz phase noise at an offset frequency of 100 kHz [45]. However, GaAs and even CMOS devices have demonstrated excellent performance as well. This may be due in part to their improved linearity, which tends to minimize the up-conversion of low-frequency noise components [46].

The output of the VCO is typically phase-locked to an external reference by means of frequency dividers embedded within a PLL [47]. In these cases, it is also important that the phase noise of the frequency dividers be minimized in order to insure that the overall noise performance is not compromised. Phase noise levels at the input to an *ideal noiseless* digital divider of ratio N are reduced by $20\log_{10}N$ at the divider output [48]. In these cases, the phase noise requirements at the divider *output* can be more important than those at the divider *input*, in contrast to more typical cascaded noise calculations.

In order to make accurate technology comparisons for divider phase noise, the divider circuits should be normalized to the same frequency. Furthermore, there will be a significant difference in performance between synchronous and ripple counters in terms of their phase noise performance [49],

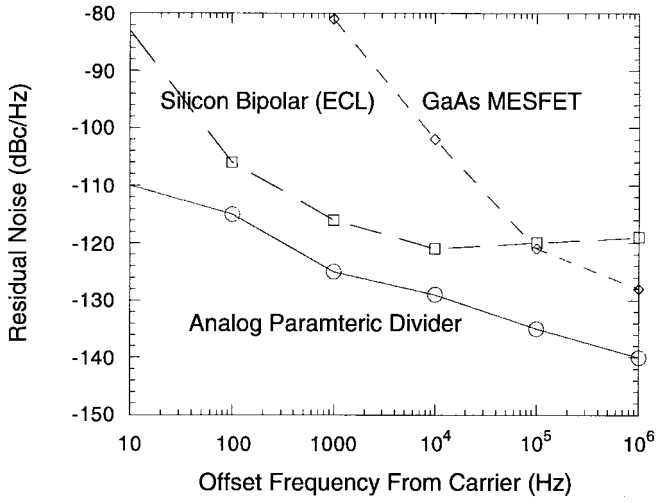


Fig. 11. Reported frequency divider residual phase noise normalized to 10 GHz [50]. Note that the lower phase noise of the silicon bipolar transistor results in lower residual divider phase noise.

since all of the noise sources add independently in the case of a ripple counter. Fig. 11 plots the relative phase noise performance of frequency dividers implemented in a variety of technologies, normalized to 10 GHz [50]. It is clear from these results that, all else being equal, technologies that exhibit low flicker noise will exhibit the best frequency divider phase noise performance.

D. RF Switches

High quality microwave switches are a key building block at the input of most TDD systems since they perform the crucial task of switching between the transmit and receive mode. Historically, microwave switches were realized with high-quality p-i-n diodes. However, the large control currents required by these devices have necessitated the use of GaAs FET-based switches for most handheld applications (due to their low dc power consumption).

A major conflict arises when transmit power levels in excess of +30 dBm are passed through a switch operated from a 3-V or lower supply. The two problems are maintaining linearity in the "on" state and maintaining isolation in the "off" state. Junction isolated silicon technologies have great difficulty in meeting these performance targets, due to the possibility of forward biasing the substrate junction diodes during large power excursions at the input to the switch. A typical value for a GaAs MESFET switch achieves a 1-dB compression point of +30 dBm, with 1 dB insertion loss and 25 dB isolation at 1 GHz [51]. A GaAs MESFET single-pole double-throw (SPDT) switch for PHS (1.9 GHz) applications was recently demonstrated using a novel resonance structure for improved isolation in the "off" state [52]. It exhibited an insertion loss of 0.5 dB and an isolation of 35.8 dB.

At higher frequencies, a CMOS/SOS switch recently demonstrated an input-referred third-order intercept point of 18 dBm at 2.4 GHz, with a 1.8 dB insertion loss and 30 dB isolation in the "off" state [53]. In this particular application, switches built in semiconductor IC technologies with insulating substrates (such as GaAs and CMOS/SOS) have some significant advantages compared to bulk CMOS technology. However, an Si/SiGe HBT SPDT switch was recently demonstrated for DECT and DCS1800 applications [54]. The insertion loss was $<$1.5 dB and the isolation was $>$25 dB, although linearity was not reported.

IV. Technology Research Directions for RFIC Applications

The major development in RFIC technology for the foreseeable future will be the relentless progress of CMOS, and to a lesser extent silicon bipolar and GaAs technologies, toward smaller geometries, higher performance, and higher levels of integration. As a result, RFIC applications can "ride the wave" of digital integrated circuit technology advances for some time to come.

However, a variety of new technologies—specifically designed for RFIC's but complementary to existing approaches—are beginning to emerge from various laboratories. These technologies may allow for dramatic improvements in RFIC performance in the future. This section will summarize some innovative approaches that have recently been taken toward fundamental improvements in RFIC technology.

A. Monolithic Inductors

Although planar monolithic inductors have a long history, there has been renewed interest recently in their development, with application to RFIC VCO's in particular. The realization of high performance inductors—with performance comparable to hybrid implementations—is *fundamentally* limited by the fact that inductor Q is roughly proportional to the *area* of the inductor [55]; the inevitable area limitations of a monolithic integrated circuit render dramatic improvements in Q nearly impossible. Most current efforts at Q enhancement involve modest reductions in series resistance, or elimination of substrate loss effects. These efforts include the use of thick gold metallization [56], multiple metal layers in parallel [57], bulk micromachining techniques for the removal of resistive material underneath the inductor [58], and spun-on thick dielectrics [59] to physically separate the inductor from the lossy silicon substrate. Peak values of monolithic inductor Q in the 5–20 range have been achieved to date, but this is still well below what is achievable using off-chip hybrid components, which have typical peak Q's in the 50–500 range.

A summary of reported *peak-Q* (prior to self resonance) as a function of inductance is shown in Fig. 12. Clearly, the best results are obtained on a semi-insulating substrate, such as GaAs or sapphire, and with an extremely thick high-conductivity metal layer—such as gold. This will be difficult to achieve in a standard silicon process environment. Recent results employing copper metallization point to improvements in Q using standard very large scale integration (VLSI) metallization [60]. A further improvement in the Q of monolithic inductors was recently demonstrated by researchers, who employed "porous silicon" processing techniques to increase the resistivity of the bulk substrate underneath a spiral inductor [61].

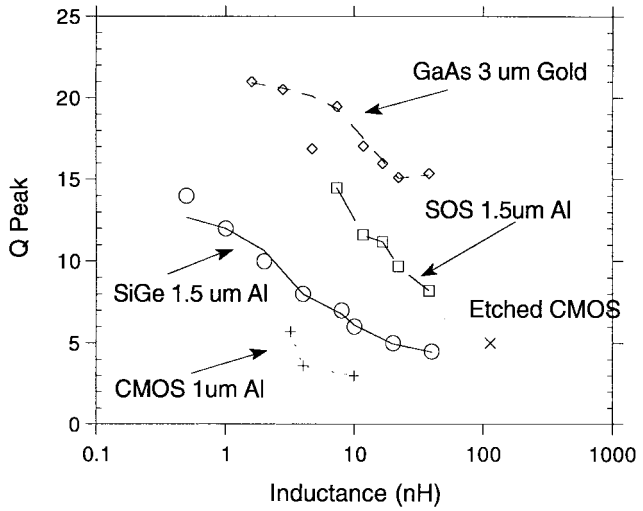


Fig. 12. Reported peak-Q values of monolithic inductors as a function of inductance [56]–[59]. The highest values of peak inductor Q are obtained with semi-insulating substrates and relatively thick metallizations.

B. Micromachining Technology for RFIC Applications

Bulk and surface micromachining techniques have recently been applied to RF and microwave integrated circuits in order to address a variety of limitations of traditional semiconductor approaches to high-frequency transceivers [62]. These devices include microwave switches for front-end TDD applications [63]–[65] and a high-Q micromachined capacitor for VCO applications [66]. The switches have the potential for superior isolation, insertion loss, and linearity compared with semiconductor-based switches, since the only conductor in the switch is metal, and the only dielectrics are air, Si_3N_4, and SiO_2. There is virtually no dc power consumption during operation, and input intercept points in excess of +66 dBm have been demonstrated [65]. Both "bending-beam" [62] and capacitively coupled switch [65] geometries have been demonstrated. The bending beam approach promises lower insertion loss and improved isolation, at the expense of uncertain reliability performance. The switching time with either approach appears to be adequate for most handheld mobile applications.

A micromachined voltage variable capacitor [66], where the plates of a parallel plate capacitor are suspended in air, demonstrated a 16% tuning range with a quality factor of 60 at 1 GHz. This element would be an attractive alternative to a lower Q monolithic varactor diode for a VCO application. One potential drawback of this approach is that vibration-induced phase noise, due to mechanical resonances within the structure, can be substantial. A reduced pressure environment can reduce the effect.

At higher frequencies, there has recently been substantial progress in the area of bulk-micromachining techniques for the realization of monolithic suspended stripline filters, from 20–100 GHz [67], [68]. At these frequencies, the free-space wavelength is compatible with monolithic integrated circuit fabrication techniques, and the Q's that are achievable are substantially higher than those of planar integrated circuit approaches because the transmission lines are essentially "floating in air." These structures exhibit negligible dielectric losses and very little dispersion or radiative losses. A 95-GHz bandpass filter was realized in this technology and achieved a 3.4-dB insertion loss with a 6% bandwidth [68]. However, scaling this technology to lower frequencies presents some daunting challenges, because the dimensions required for the matching elements grow as the frequency drops.

C. CMOS/SOS Technology for RFIC's

One approach to circumvent some of the drawbacks of silicon technology for RFIC applications (lossy substrate, poor high-frequency isolation) is the use of a sapphire substrate in a CMOS/SOS configuration [69], [70]. It was recognized that this technology could have potential applications for microwave and RF circuits, beyond its traditional applications to radiation hardened environments, if the cost could made comparable to that of traditional CMOS technology.

Substantial progress has been made recently in the development of this technology for wireless transceiver applications.[1] N-channel MOSFET's with 0.5-μm T-gate structures exhibit f_T values in excess of 22 GHz and f_{MAX} values in excess of 60 GHz [71]. Comparable P-channel devices exhibit f_T values in excess of 10 GHz and f_{MAX} values in excess of 50 GHz. A 2.4-GHz monolithic LNA fabricated in this technology exhibited 10 dB of gain with a 2.8 dB noise figure and input referred intercept point of 4 dBm while dissipating 14 mW of dc power [28]. Fig. 13 shows the excellent inductor performance recently achieved with the technology.

CMOS/SOS technology has also been used by Peregrine Semiconductor to demonstrate a fractional-N PLL frequency synthesizer operating at 1.1 GHz, whose power dissipation is only 24 mW [72] in a 0.7-μm technology. The phase noise at the output circuit was 75 dBC/Hz at 31.25 kHz away from the carrier frequency at approximately 650 MHz. The phase noise performance was aided by the high-isolation of the substrate, which minimized the noise contribution from the digital portions of the circuit from intermodulation with the high-frequency VCO and PLL.

V. Cost and Time-to-Market

Other important issues for the implementation of RFIC's in the commercial marketplace are final production cost and time-to-market. Final production costs are mostly determined by manufacturing scales of efficiency and cumulative production volumes. Both the high-speed silicon bipolar and GaAs RF markets are expected to grow to over a billion dollars in the next four years, but they are both dwarfed by the greater than 100 billion dollar per year CMOS market. As a result, CMOS technology is expected to possess a significant edge in final wafer production costs—measured in a dollars per square millimeter—for the foreseeable future, and this presents an attractive opportunity to leverage CMOS technology into the RF regime. For example, Micron Technology has demonstrated a set of RFID products based on CMOS technology.[2] Each

[1] These research results were obtained under the direction of Prof. P. Asbeck, of the University of California, San Diego, and Dr. I. Lagnado of the Naval Command Control and Ocean Surveillance Center.

[2] An interesting overview of the technology can be found at http://www.micronccommunications.com.

integrated circuit combines a direct sequence spread spectrum (DSSS) microwave frequency radio, a microcontroller, and a low-power static random access memory (SRAM). The IC, when coupled with an antenna and a battery, forms the complete RFID product.

However, time-to-market and performance issues are also important for RF applications, and it is in these areas that traditional Si bipolar and GaAs technologies possess an edge at this time. In addition, the cost and performance of *discrete* hybrid RF system building blocks continues to improve rapidly, and the ease with which these components can be prototyped and placed quickly into production has doomed many highly integrated monolithic RFIC implementations [73].

Nevertheless, in the long run, CMOS technology will acquire many of these desirable qualities, and Si Bipolar and GaAs technologies will find themselves increasingly pressed by competition with CMOS in the 1–2.5 GHz frequency range. RF CMOS is one of the most actively researched areas in the integrated circuits community, as evidenced by a variety of recent publications [74].

VI. Conclusion

The implementation of highly integrated radio transceivers is one of the great challenges in the area of integrated circuit technology today. The ideal goal of a low-cost "single-chip radio" is becoming increasingly plausible, as research and development groups around the world develop improved techniques for minimizing the limitations of integrated circuit technology for the wide variety of functions required of a radio unit. The choice of technology to implement these radios is complicated by a variety of factors, including performance in each of the critical functional areas, as well as final production price and time to market. CMOS technology is clearly the most attractive technology in the long run. However, at this time, the critical functional blocks for radio transceivers exhibit the best performance in GaAs or Si bipolar technologies, especially when dc power dissipation is a major consideration.

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