Improved Design Technique of a Microwave Class-E Power Amplifier with Finite Switching-on Resistance

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Abstract: The class-E amplifier is a highly efficient amplifier for microwave power applications. Due to the complexity involved, previous analytical efforts assumed either zero switch resistance and/or infinite drain (collector) inductance, which resulted in less than optimum designs. In this paper, we take the effect of both the finite switching-on resistance and finite drain inductance into account, and present an improved and optimized design technique. A 1.9GHz CMOS class-E power amplifier, which can deliver 0.25W of output power, was analyzed as an example of this new design technique. Excellent agreement between the theoretical analysis and simulation results is reported, pointing the way towards the optimized design of the class-E stage for microwave applications.

I. Introduction

The class-E amplifier is a switching-mode amplifier, which has the intrinsic ability to realize very high drain(or collector) efficiency due to the fact that the drain voltage is minimized when the device is "on". This is very attractive for implementation of power amplifiers in portable wireless communications applications, where the dc power consumption needs to be absolutely minimized [1]. The class-E amplifier was first introduced by Ewing [2], and then was further elaborated by Sokal [3] and other researchers [4] [5]. To alleviate the analytical complexity, all their theoretical analysis assumed either zero switch resistance and/or infinite drain inductance, resulting in less than optimum designs. Recently published class-E papers [6]-[8] also relied on the previously reported analysis and concentrated on the implementation details.

To obtain an optimized class-E operation, an analytical method accounting for both finite choke inductance and finite switching-on resistance is necessary. In this paper, this optimum is established for the first time under the constraint of a given $R_{switch}C_{switch}$ product, which is a more realistic estimate of the operation in a typical MOS technology. This new technique expresses the optimum circuit parameters in terms of the amplifier specifications, such as output power, device output capacitance, and operating frequency. The agreement obtained between this new design approach and circuit simulation results is outstanding, verifying the utility of the technique.

The disadvantage of this technique is its analytical complexity due to the inclusion of both the finite choke inductance and the finite switching-on resistance. Although the analysis leads to more accurate and optimized designs, it does not provide naturally intuitive results.

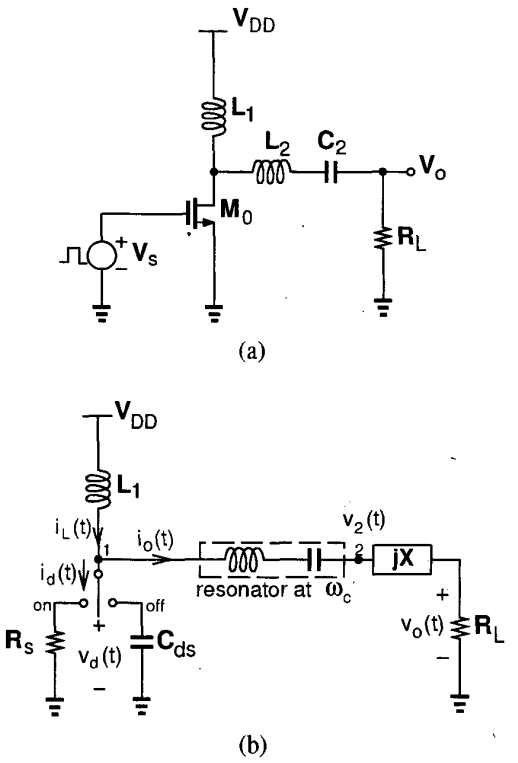


Fig. 1. Class-E power amplifier. Part (a) shows the simplified schematic, and part (b) shows the model accounting for both finite "on" resistance and finite drain inductance.

II. Analysis

The simplified CMOS class-E amplifier circuit and the corresponding improved model is shown in Fig. 1. To sim-

plify our analysis, the model assumes that the switching-on resistance R_s is constant, the output capacitance C_{ds} is independent of the switch voltage and the Q factor of the output circuit is large enough to only allow a sinusoidal output current, which is expressed as:

$$i_o(t) = I_o sin(\omega_c t + \phi_o) \tag{1}$$

where I_o is the amplitude of the output current, and ϕ_o is a phase shift constant.

At the drain node of M_0, we have

$$i_L(t) = i_d(t) + I_o sin(\omega_c t + \phi_o) \tag{2}$$

$$V_{DD} - v_d(t) = L_1 \frac{di_L(t)}{dt}. \tag{3}$$

The operation of the amplifier is divided into two parts:

- *Off state*: when the transistor is off,

$$L_1 C_{ds} \frac{d^2 i_{Loff}(t)}{dt^2} + i_{Loff}(t) = I_o \sin(\omega_c t + \phi_o) \tag{4}$$

- *On state*: when the transistor is "on", it is resistive and

$$V_{DD} - i_{Lon}(t)R_s + I_o R_s \sin(\omega_c t + \phi_o) = L_1 \frac{di_{Lon}(t)}{dt}. \tag{5}$$

Solving [4] and [5] results in

$$\begin{aligned} i_{Loff}(t) &= A\cos(\omega_o t) + B\sin(\omega_o t) \\ &\quad + \frac{I_o}{1-\beta^2}\sin(\omega_c t + \phi_o) \end{aligned} \tag{6a}$$

$$\begin{aligned} i_{Lon}(t) &= \frac{I_o \gamma}{\gamma^2 + {\omega_c}^2}[\gamma \sin(\omega_c t + \phi_o) \\ &\quad - \omega_c \cos(\omega_c t + \phi_o)] \\ &\quad + \frac{V_{DD}}{R_s} + Ce^{-\gamma t}, \end{aligned} \tag{6b}$$

where

$$\omega_o = \frac{1}{\sqrt{L_1 C_{ds}}} \tag{7a}$$

$$\beta = \omega_c/\omega_o \tag{7b}$$

$$\gamma = \frac{R_s}{L_1} \tag{7c}$$

and A, B and C are constants to be determined. The amplifier specifications are V_{DD}, ω_c and P_{out}, which are fixed by the design requirements. Assuming the device size is chosen, i.e., R_s and C_{ds} is known, the only variables to be evaluated are A, B, C, Io, ϕ_o and L_1. Thus, six equations are required to solve these six variables. Note that we have

- *Periodic condition:*

$$i_{Lon}(t)\Big|_{t=(n+1)T} = i_{Loff}(t)\,|_{t=nT} \tag{8a}$$

$$v_{don}(t)\Big|_{t=(n+1)T} = v_{doff}(t)\,|_{t=nT} \tag{8b}$$

- *Boundary condition:*

$$i_{Lon}(t)\Big|_{t=(n+1/2)T} = i_{Loff}(t)\Big|_{t=(n+1/2)T} \tag{9}$$

- *Class-E conditions:*

$$v_{doff}(t)\Big|_{t=(n+1/2)T} = 0 \tag{10a}$$

$$\frac{dv_{doff}(t)}{dt}\Big|_{t=(n+1/2)T} = 0 \tag{10b}$$

- *Power conservation condition:*

$$\frac{V_{dd}}{T}\int_0^T i_L(t)dt = P_{out} + \frac{1}{T}\int_{\frac{T}{2}}^T i_{don}^2(t)R_s dt. \tag{11}$$

Solving [8]-[11], we get L_1, I_o, ϕ_o and the expressions of all the currents and voltages as functions of time. Once this is accomplished, the rest of the circuit parameters can be derived easily.

First, R_L and L_2 can be evaluated from

$$P_{out} = \frac{I_o^2}{2}R_L \tag{12}$$

$$L_2 = \frac{Q_L R_L}{\omega_c} \tag{13}$$

since ω_c and P_{out} are design specifications and I_o has been evaluated from previous calculations. There is no specific requirements for Q_L except that it must be large enough to only allow a sinusoidal output. In our design, a Q_L of 5 is chosen.

Second, as shown in Fig. 1, C_2 is the series combination of the capacitor in the output resonator and the excessive reactance X. Thus, we have

$$C_2 = \frac{1}{\omega_c(\omega_c L_2 - X)}. \tag{14}$$

X can be evaluated by the fact that the amplitude of the voltage at node 2 (V) is also the fundamental component of the drain voltage of M_0, i.e.,

$$\begin{aligned} V &= \frac{2}{T}\int_{nT}^{(n+1)T} v_d(t)\sin(\omega_c t + \phi_1)dt \\ &= I_o R_L \sqrt{\left(1 + \frac{X^2}{R_L^2}\right)} \end{aligned} \tag{15}$$

where

$$\phi_1 = \phi_o + tan^{-1}\left(\frac{X}{R_L}\right). \tag{16}$$

Thus C_2 can be solved.

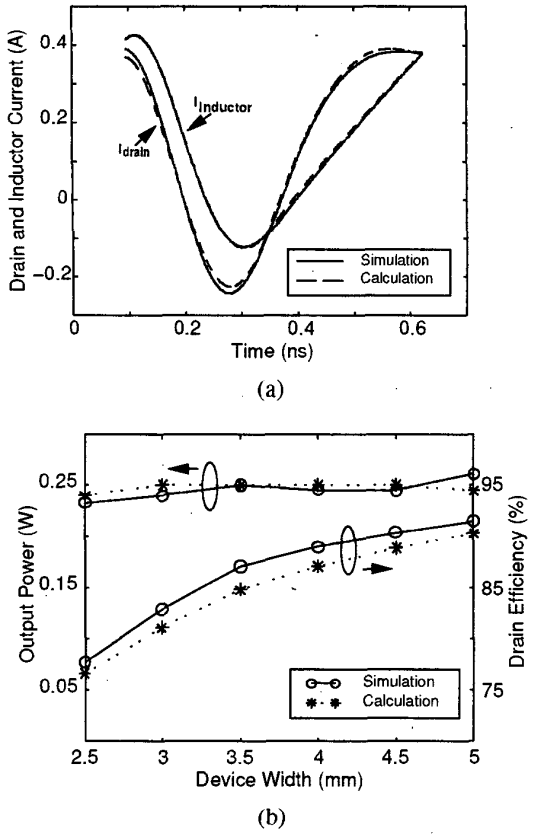


Fig. 2. Comparison between simulation and calculation. Part (a) shows the current waveforms, and part (b) shows the output power and the drain efficiency versus device size.

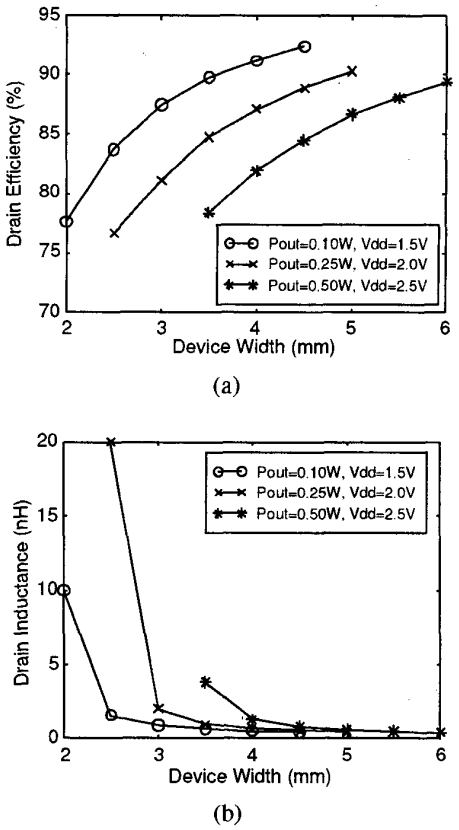


Fig. 3. Simulated (a) drain efficiency and (b) optimum drain inductance versus the device size at three different output power levels.

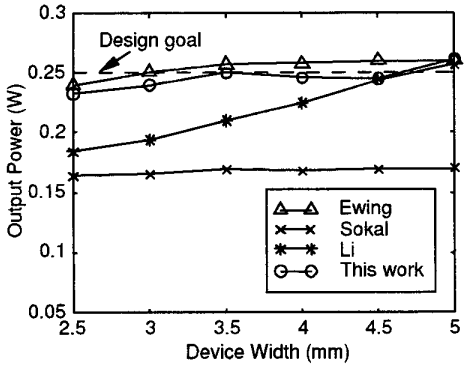
III. Results

As an example of this new design procedure, a 0.25W class-E power amplifier, operating at $V_{DD} = 2V$ and $f_c = 1.9GHz$, was analyzed. The device parameters are those of a $0.6\mu m$ digital CMOS technology. We achieve a peak of 87% drain efficiency from SPICE simulations, and the theoretically calculated results are in excellent agreement with the simulated one, as shown in Fig. 2. In order to explore how the switching-on resistance may influence the drain efficiency and peak drain voltage, different sizes of MOS devices are used in calculating the corresponding class-E operation under the constraint of $R_sC_{ds} = 0.88\Omega * 3.5pF$. As shown in Fig. 3, with the device size getting wider, the drain efficiency improves because the switching on-resistance becomes smaller. However, as the device size is increased to maximize the amplifier drain efficiency, designing the driving stage becomes more difficult due to the increased gate capacitance. At the same time, the optimum drain inductance becomes less than 1nH, resulting in implementation difficulties. Therefore, a tradeoff has to be made in choosing the optimum device size.

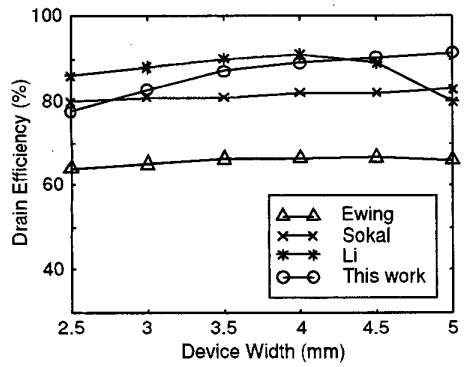
To show this technique leads to improved designs, simulations were performed based on the different design approaches developed by Ewing [2], Sokal [3], Li [5] and us, respectively. Ewing assumed an infinite drain choke inductance but a finite switching-on resistance. Sokal assumed an infinite drain choke inductance with an ideal switching condition, i.e., zero switching-on resistance. Li took the finite drain inductance into account and assumed an ideal switching condition. To make the comparison fair, we employed the same devices and set the same design specifications of $P_{out} = 0.25W$ and $f_c = 1.9GHz$. Since both Ewing and Sokal assumed an infinite choke inductance, their designs have one less freedom than Li's and ours. To achieve the design specifications and make the comparison

possible, V_{DD} was varied for Ewing's and Sokal's designs and was fixed as $2V$ for Li's and our designs. Fig. 4 shows the simulated output power and drain efficiency versus the device size by the four design approaches.

The simulation results show that Ewing's approach has good output power performance, but with poor drain efficiency, while both Sokal and Li's works achieve good efficiency but with poor output power performance. Our design technique, however, not only achieves the specified output powers, but also optimize the drain efficiency.



(a)



(b)

Fig. 4. Simulated (a) output power and (b) drain efficiency versus device size based on the design approaches developed by Ewing, Sokal, Li and this work.

IV. Conclusions

An analytical method was described to determine the optimum performance of class-E amplifiers with both finite drain inductance and switching-on resistance. Direct expressions for the circuit parameters, component values in terms of certain initial settings, amplifier specifications, and time function of circuit parameters can be obtained. The most valuable aspect of this result is that it considers the effect of both the switching-on resistance of the device and the finite shunting inductance, which is very close to the real world transistor as the output stage. For a low-power device, which is widely used in mobile and portable communication equipments, the resistance is the major source that consumes the input power and makes the real power efficiency drop. According to the simulation results, there is excellent agreement with the theoretical results. The technique is especially useful for bulk MOS devices characterized by high drain-bulk capacitance.

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