Design Options for High Efficiency Linear Handset Power Amplifiers

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***Abstract* — Design techniques for handset power amplifiers are discussed, with emphasis on high efficiency architectures and CMOS technology. Experimental results with prototype circuits including Doherty, envelope tracking, outphasing and digital polar modulation are presented. Future design challenges are also highlighted.**

***Index Terms* — Power amplifiers, RF transmitters, wireless integrated circuit technology.**

I. Introduction

With the emergence of WiMAX and 3GPP Long Term Evolution applications, future handset power amplifiers must accommodate broader bandwidth and higher peak-to-average ratio than present circuits. Multiband and multimode operation should also be provided. A premium is placed on amplifier efficiency in order to preserve battery life even as the data throughput is increased. This paper discusses options for power amplifier design, with emphasis on high efficiency techniques.

II. Device Technology

In handset applications, GaAs HBT is currently an established technology, with costs that have successfully been decreased over time. Most research efforts focus on Si, to exploit the high levels of integration available. LDMOS technology can achieve the high breakdown levels needed for cell phones, and is being actively pursued, along with BiCMOS approaches. Entirely CMOS solutions remain an elusive goal. Excellent demonstrations have been made of CMOS-based saturated PAs, such as with distributed active transformers [1]. Comparable results have not yet been realized with linear amplifiers. A critical problem is the limited voltage swing available to the CMOS devices. Traditional strategies to deal with this are to use differential structure and cascode device combinations. Current research strategies pursue similar paths, with added technology: 1) transformers with multiple inputs, to partition the power requirements among many individual amplifier units [1,2]; and 2) stacking more than two transistors in series. Transformer implementation on the circuit board results in highest efficiency, and on the chip gives lowest cost. Representative on-chip transformers achieve coupling factor k of order 0.7 at 1.9GHz and as a result have sizeable leakage inductances that require careful tuning to resonate them at the desired frequency.

The approach of stacking transistors can in principle lead to arbitrary values of voltage handling capability. The series resistance increases with stacking, so that increasing device width is needed at the same time. The stacking principle has been applied with success for RF switches, such as needed next to the antenna for TX/RX and band selection, where voltage levels can be very high (handling 15V is required). One of the penalties of device stacking, the body effect reduction of gm and the source/drain to body capacitance, is avoided with silicon on insulator. The same strategy can be applied in power amplifiers. Fig.1a shows the schematic design of a 3 stack amplifier. For best operation, the gate-source and drain-source swings should be identical for each device. This can be achieved if the gate for different devices is made to swing over increasing voltage ranges with properly sized capacitive terminations on the gates [3,4] (unlike the cascode case, for which the ac signal on gates is zero for the higher transistors). Fig. 1b shows the simulated voltage swings for the three transistors. Fig.2 shows the measured characteristics of output power , gain and efficiency for a prototype 3 stacked power amplifier implemented in SOS technology. The device achieved a voltage swing of 7V, into a load resistance of 50 ohms (and as a result, no output impedance matching was needed on chip).

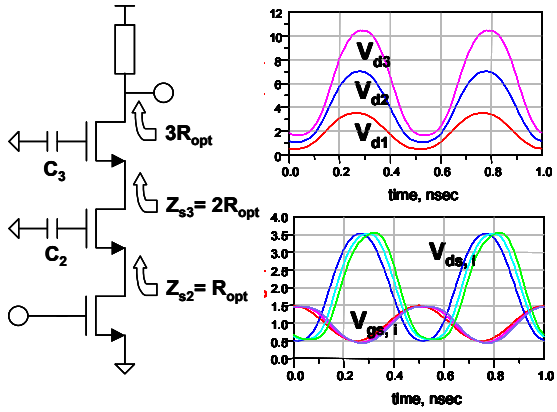

Fig.1: a) Schematic stacked nMOS design; b) simulated drain voltage, Vds and Vgs waveforms for the stacked devices.

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III. High Efficiency Architectures

A well-know problem is the rapid fall-off of efficiency as the power is backed off from its maximum value. To cope with this problem on the time-scale of power control (of order msec), the strategies of by-passing stages using RF

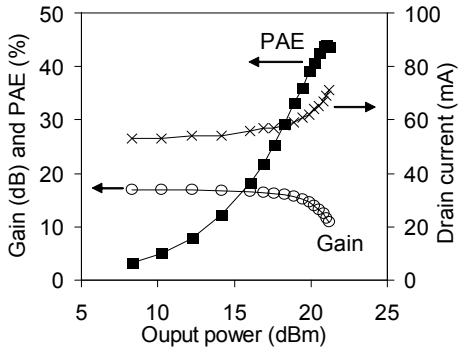

Fig.2: Experimental results for 3 stacked nMOS amplifier using SOS technology.

switches or by slowly varying the power supply voltage using efficient dc-dc converters have been established. An increasingly burdensome problem is the variation of power on a faster time scale associated with the

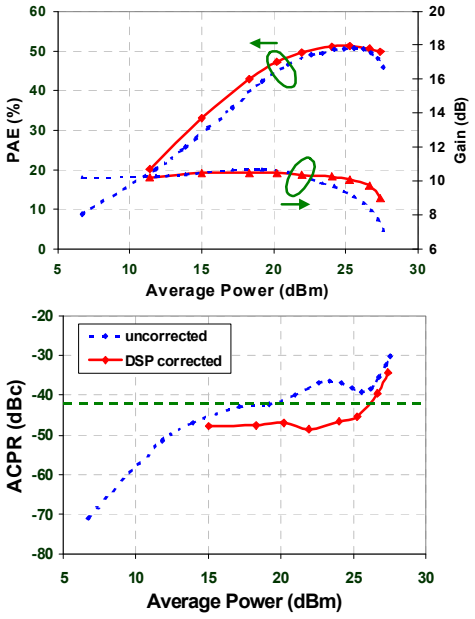

Fig.3: Experimental results for Doherty handset PA using CDMA inputs. Results before and after digital predistortion are shown.

modulation. Peak-to-average power ratio for the WiMAX and 3GPP Long Term Evolution standards is increasing (to nominally over 10dB, although it is likely that with the use of "decresting" the PAR will end up at 7-9dB). Architectures that can achieve high efficiency on a rapid modulation basis include the Doherty, the Outphasing and the EER or Envelope Tracking amplifier.

Doherty amplifiers have become widespread for basestation implementations since they typically provide very good efficiency improvement over a 6dB backoff range. Improvements over a range of 10-12 dB can also be obtained with three stage Doherty structures or asymmetric Doherty structures which provide an impedance variation for the main amplifier by a factor of 4 instead of the more conventional factor of 2. The opportunities for handsets are considerable - but there are also problems. In basestations it is customary to apply

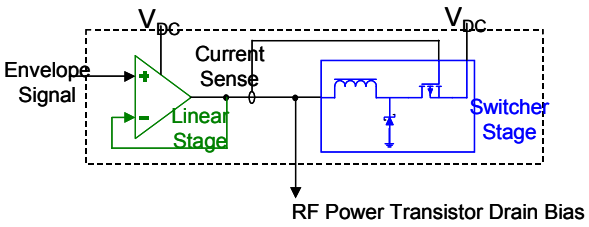

Fig. 4: Architecture of dynamic drain voltage supply for ET and EER amplifiers.

linearization through digital predistortion (DPD) or related techniques, while in handsets the luxury of predistortion is not generally allowed. Fig. 3 illustrates experimental results for a handset Doherty PA implemented with GaAs FETs, with and without DPD [5]. Dramatic improvement in efficiency is obtained over a wide power range. The classical Doherty employs transmission line impedance converters, which must be shrunk in size with L-C networks for implementation in mobile units. The handset application also must consider an output impedance mismatch from the antenna, not present in the base-station. The Doherty is in general more sensitive than a single PA, or a balanced PA. Adaptive techniques may be needed to sense various non-standard conditions and optimize the amplifier configuration to cope with them.

Envelope tracking (ET) and Envelope Elimination and Restoration (EER) systems operate by rapidly varying the power supply voltage in accordance with the modulation, keeping the RF transistor near saturation almost all the time. ET and EET have been shown to provide exceptionally high efficiencies in base station applications. A significant issue is to provide a high efficiency dynamic power supply voltage. It is generally accepted that a dc stage based on a switching converter is to be used, together with a linear stage that typically has lower efficiency, as shown in fig. 4. Both the Vdd amplifier and the RF stage can be made in integrated form, with powers appropriate to handsets, and initial demonstrations with good efficiency (28%) for WiFi signals with bandwidths

up to 20MHz have been carried out [6]. One issue of general concern is linearity; most systems operate with the assistance of digital predistortion. Another concern is the accuracy of time alignment between the envelope signal and the RF signal. For EER systems, power control also becomes an issue, as described below. In ET, operation smoothly merges into linear Class AB at low power levels.

Outphasing amplifiers exploit two RF amplifier stages operating in compression at high efficiency, and provide output amplitude modulation by virtue of the constructive or destructive interference between the two outputs. In base-station applications, promising efficiency has been demonstrated [7]. In handset applications, improvements

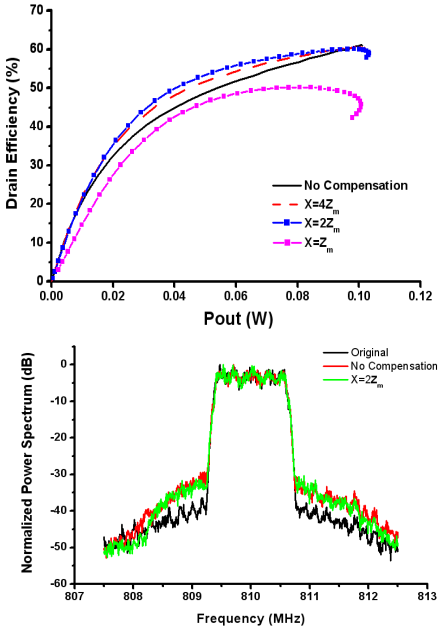

Fig. 5: Experimental results for CMOS amplifier with Chireix combiner: a) efficiency for CW signals; b) spectrum with CDMA signal.

in efficiency are also possible. One key problem is that often the RF output stages have output power that varies with the load impedance modulation associated with the outphasing angle. Good linearity and efficiency has been observed, however, with CMOS-based output stages operating as voltage-mode Class D amplifiers which are very immune from load changes, as shown in fig. 5 (although the VMCD amplifiers can suffer from increasing C_{ds} discharge loss at higher frequency). Another issue with outphasing amplifiers is that to accurately reproduce low output powers, the gain and phase through the two amplifier chains must be accurately matched. Efficiency tends to degrade for low output power. A useful strategy is likely to convert from Chireix modulation to conventional modulation (symmetrically provided to the two amplifiers) as the power level decreases, and the efficiency becomes less critical.

IV. Polar Amplifiers and Digitally Controlled Amplifiers

The polar modulation approach to power amplifiers is a generalization of the EER technique, and is attractive for providing a simplified structure for the overall transmitter, one that can be easily adapted to different signaling formats and frequency bands. While use of a dynamic power supply is the highest efficiency technique for polar modulation, a variety of other approaches are interesting. Direct use of digital inputs for amplitude control at the modulation rates is a convenient technique that leverages the capabilities of modern CMOS. One of the strategies that have been advanced for amplitude control is to vary the number of transistors turned on [9]. As shown in fig.6, the output amplifier is made up of a number of identical cells, and in response to the amplitude control word, a suitable number of them is turned on to provide the output signal. The circuit functions as a digital-to-analog converter and power amplifier. Depending on the load line that is employed with this circuit, the individual elements can act as current sources (and thus achieve a

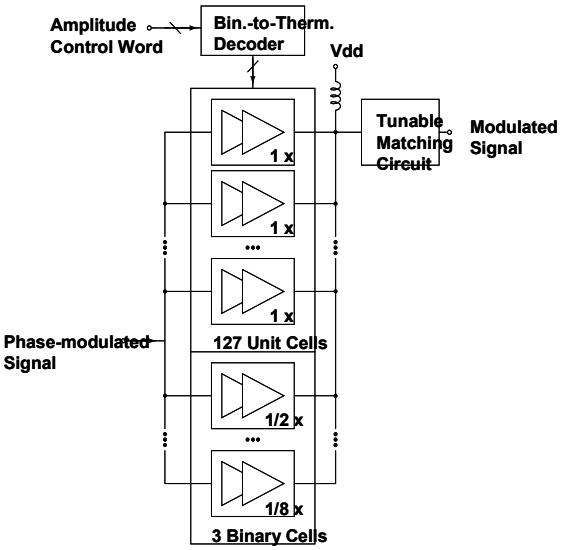

Fig. 6: Architecture of digital power amplifier based on control of number of unit cells.

relatively linear output power vs. transistor count) or the elements can be placed in compression at high power (thereby increasing efficiency, at the cost of linearity). Fig. 7 shows the dynamic load line simulated for unit cells under different conditions. As for EER and ET, it is critical that timing adjustment be correct between envelope and RF phase signal inputs. In order to correct

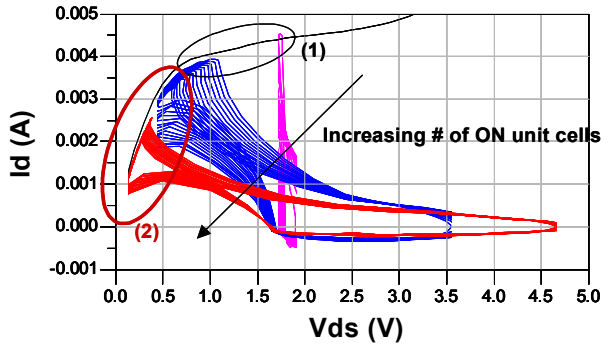

Fig.7: Simulated variation of load lines in digitally controlled PA as output power changes.

for the nonlinearity of the signal, digital predistortion is required.

V. Challenges

The wide dynamic range of power control required for several signal standards (up to 90 dB for WCDMA) represents a significant challenge for high efficiency operation. For several of the architectures discussed, attenuation of the *input signal* with a variable gain amplifier is not an option. Output power control can be exercised by techniques similar to the signal modulation (e.g. variation of power supply or transistor count, interference between signals). However, this can generally only be maintained over a limited range (of order 20dB). An additional strategy is to implement a variable attenuator, so that very low values of output power can be achieved as needed. The inefficiency associated with the attenuator can be insignificant for the overall power budget. Another major problem is receive band noise. For frequency division duplex systems such as CDMA and WCDMA, the spurious emissions of the transmitter in the frequency band reserved for the receiver (typically 60-80 MHz away from the transmit frequency) must be very low, of order -80 dBm/100KHz from the PA, according to present specifications (which already assume attenuation of 45dB from the duplexer employed). Attainment of this low level of RX band noise is a major challenge for EER, ET, and polar amplifiers. One direction in which to seek solutions is to employ active noise cancellation circuits. For example, simple techniques of this type can enhance the noise rejection of the duplexer by 20dB over a narrow band (limited by the requirement of group delay matching), as shown in fig. 8.

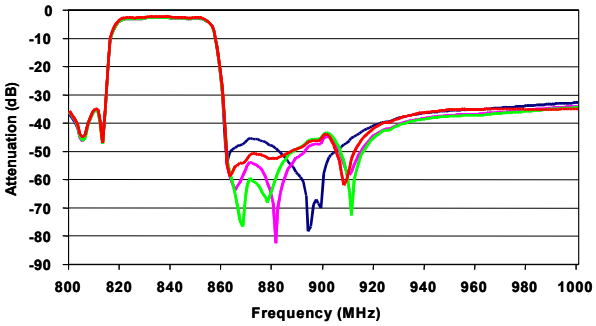

Fig.8: Experimental transfer curves for duplexer enhanced with active feedforward noise cancellation [10]

V. Conclusions and Outlook

Research results are promising for the implementation of power amplifiers that can maintain high efficiency over a wide dynamic range of modulation and power control. To achieve robust operation over antenna mismatch, power supply voltage and temperature conditions, as well as multimode and multiband operation, strategies for tunability and adaptability will likely be required. It remains to be determined if digital control and signal processing should be done within the PA or transmitter module, or if the resources of the baseband DSP within a handset should be used.

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