# A Low-Distortion, Low-Loss Varactor Phase-Shifter Based on a Silicon-on-Glass Technology

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***Abstract*—A varactor-tuned continuously variable phase shifter based on an all-pass network is presented. Design equations for this phase shifter network are derived and presented. The phase shifter achieves an IIP3 of 52dBm with 10MHz tone-spacing at 2GHz and loss of 2.3-3.7dB with continuous 180° phase shift at 2GHz. The total chip size including pads is 2900$\mu$m X 2200$\mu$m.**

***Index Terms*—Phase shifters, phased arrays, varactors, All-pass networks, variable inductors, silicon on insulator technology**

## I. Introduction

Phase-shifters are valuable components in the transmit and receive paths of phased-array radar and communication systems. The performance requirements in these systems are stringent; the phase shifters should be highly linear to prevent signal distortion and they should be compact for a small form factor. They are also required to have low dc power consumption and low insertion loss. MEMS phase shifters are excellent candidates for phased array antenna systems, since they demonstrate outstanding performance in many applications in terms of low insertion loss and high linearity [1], [2].

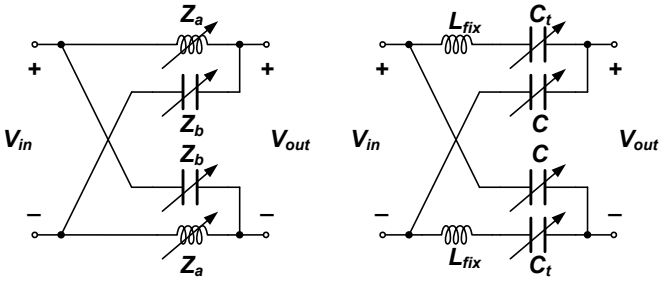
However, phase shifters based on MEMS varactor loaded transmission lines suffer from relatively high cost due to non-standard processing and hermetic packaging. An alternative to MEMS varactors would be varactor diodes, and the linearity and loss of varactor diodes were recently improved by using uniformly doped Schottky diodes in anti-series configuration associated with a dedicated silicon-on-glass technology. A varactor diode transmission line-based phase-shifter was presented in [3]. For further reduction of chip size, an all-pass-based phase shifter is presented in this work.

## II. Design Theory

Lossless all-pass networks are ideal candidates for phase shifters, since they vary the phase of a signal without affecting its magnitude. One simple implementation is shown in Fig. 1(a) [4], [5]. If the reactance components are designed such that $Z_a \cdot Z_b = R_L^2$, where $R_L$ is load resistance, then the input impedance and voltage transfer function of the circuit can be expressed as

$$Z_{in} = R_L \tag{1}$$

$$\frac{V_o}{V_{in}} = \left(\frac{1 - Z_a/R_L}{1 + Z_a/R_L}\right) \tag{2}$$




(a) (b)

Fig. 1. (a) Schematic of an all-pass network with LC reactance component and (b) schematic of a proposed all-pass network phase shifter.

From (2), the phase shift of this network is given by

$$\angle\left(\frac{V_o}{V_{in}}\right) = \Delta\phi = -2\arctan\left(\omega R_S C\right), \tag{3}$$

where $L/C = R_S^2$. From (3), a variable phase shift can be achieved by tuning the capacitance and inductance. Over a small frequency bandwidth, a variable inductance can be approximated by a fixed inductor in series with a variable capacitance $C_t$. The proposed circuit is introduced in Fig. 1(b).

In order to find appropriate values of capacitors, we set the capacitance $C_t$ to be $s$ times larger than $C$. The capacitance tuning ratio $r$, given by $C_{max}/C_{min}$, is limited by the process technology. The reactance of the series combination of $L_{fix}$ and $C_t$ can be expressed as

$$X_L = \omega L_{fix} - \frac{1}{\omega C_t} \tag{4}$$

and for a given $C_{min}$ and capacitance tuning range,

$$s = r^{-1}\left(\omega R_S C_{min}\right)^{-2} \tag{5}$$

$$L_{fix} = (1 + r) R_S^2 C_{min} \tag{6}$$

For a $50\Omega$ source and load impedance, and a varactor tuning ratio $r$ of 4:1 given by the process technology, the ratio of $C_t$ to $C$, and the necessary inductance $L$, can be obtained as a function of the minimum capacitance $C_{min}$ as shown in Fig. 2. As $C_{min}$ decreases, the achievable phase shift increases (by (3)) and the lower inductance shrinks the entire chip size. However, it also increases the size of $C_t$. An optimum value of $C_{min}$ of $260fF$ is chosen in this case. The corresponding

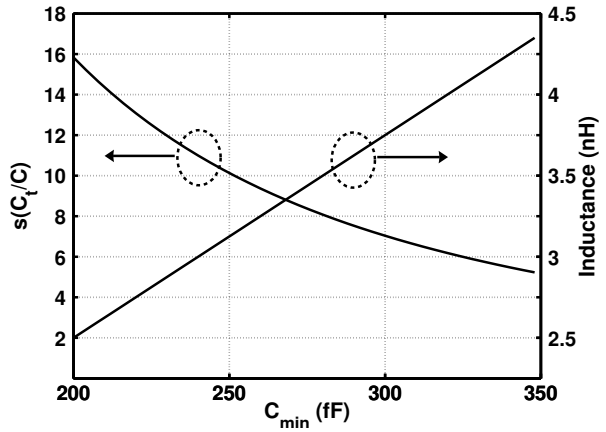



Fig. 2. Simulated value of s (=$C_t/C$) and required inductance as a function of minimum capacitance $C_{min}$ at 2GHz (capacitor tuning ratio $r$ is four).

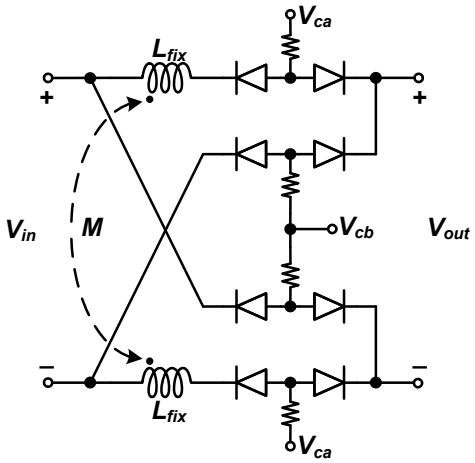



Fig. 3. Schematic of the phase shifter with distortion-free diode varactors and magnetically coupled inductors.

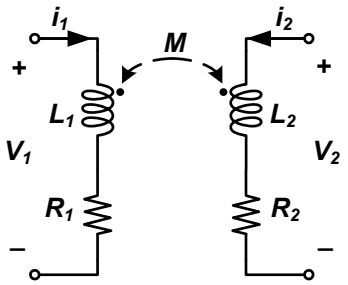



Fig. 4. Magnetically coupled inductors.

maximum achievable change in phase shift per section can be calculated from (3), which is approximately 48°.

## III. Phase Shifter Circuit Design

### A. Process Technology

In order to design a phase shifter based on the all-pass network, high-performance variable capacitors are necessary. In this study, a dedicated silicon-on-glass technology, which was developed at the Delft University of Technology is employed [6]. This technology provides a low-loss substrate and patterning of both the front and back sides of the wafer, so the intrinsic varactor can be directly contacted by thick metal on both sides. This removes the need for a buried layer or finger structures, as would be the case in conventional integrated varactor implementations [7]. Moreover, this technology presents a very high performance Schottky varactor diode; quality (Q) factor ranges typically from 50 to 300 at 2GHz and the effective capacitance tuning range of the uniformly doped diodes is approximately 4:1.

### B. Variable Capacitor Design

A schematic of a single phase shifter stage based on anti-series varactors is shown in Fig. 3. As was explained in [3], [7]–[9], for uniformly doped anti-series diodes with a sufficiently high center-tap impedance, the varactor is "distortion-free". The impedance of the dc biasing network should be significantly larger than the reactance of the varactor diodes. 120kΩ center-tap resistors are used. Anti-parallel diode pairs can be used to further increase the center-tap impedance. 120kΩ resistors are also connected at the input and output of each stage to provide DC ground for the varactor diodes. Varactor diode pairs $a$ and $b$ have zero bias capacitance of 10pF and 1pF, respectively.

### C. Inductor Design and Layout

The two separated fixed inductors are substituted with magnetically coupled inductors in order to increase the *effective* inductance. The V-I relationship for two magnetically coupled inductors (Fig. 4) can be written as

$$\begin{bmatrix} V_1(s) \\ V_2(s) \end{bmatrix} = \begin{bmatrix} sL_1 + R_1 & sM \\ sM & sL_2 + R_2 \end{bmatrix} \begin{bmatrix} I_1(s) \\ I_2(s) \end{bmatrix}, \quad (7)$$

where $M$=$k\sqrt{L_1 L_2}$, $k$ is the coupling coefficient, and $R_1$ and $R_2$ are parasitic resistances. For 1:1 coupled inductors in the phase shifter, we can assume $L_1 = L_2 = L_{fix}$ and $R_1 = R_2 = R$. If $i_2/i_1 = Ae^{j\theta}$, then the V-I relationship at the primary and secondary ports can be expressed as

$$V_1 = [j\omega L_{fix}(1 + kA\cos\theta) + (R - \omega kAL_{fix}\sin\theta)]\, I_1 \quad (8)$$
$$V_2 = \left[j\omega L_{fix}(1 + kA^{-1}\cos\theta) + (R + \omega kA^{-1}L_{fix}\sin\theta)\right] I_2$$

For a balanced differential signal applied at the input of the phase shifter, $A = 1$, $\theta = 180°$. Consequently, (8) becomes

$$V_1 = [j\omega L_{fix}(1 - k) + R]\, I_1 \quad (9)$$
$$V_2 = [j\omega L_{fix}(1 - k) + R]\, I_2$$

Therefore, the effective inductance is given by

$$L_{eff} = L_{fix}(1 - k) \quad (10)$$

By substituting $L_{fix}$ in (6) with $L_{eff}$ in (10),

$$L_{fix} = \left(\frac{1 + r}{1 - k}\right) R_S^2 C_{min} \quad (11)$$

For $k < 0$, the required inductance $L_{fix}$ decreases as $|k|$ increases, which also contributes to make the entire chip smaller.

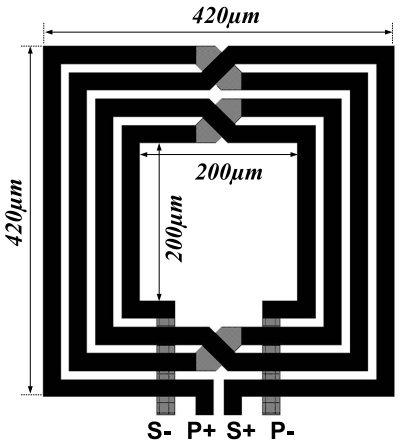



Fig. 5. Layout of the magnetically coupled inductors in the phase shifter.

As shown in Fig. 5, the 1:1 interleaved transformer is designed on the top-level metal layer of the process. This type of transformer is best suited for four-port applications that demand symmetry, since the electrical characteristics of the primary and secondary are identical when they have the same number of turns [10], [11]. The outer diameter of the transformer is 420$\mu$m and the inner diameter is 200$\mu$m. A full EM-simulation was performed, and a coupling coefficient of -0.6, with self-inductance of 2.1nH, were obtained.

### *D. Cascaded Phase Shifter Architecture*

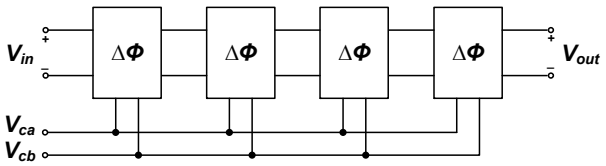
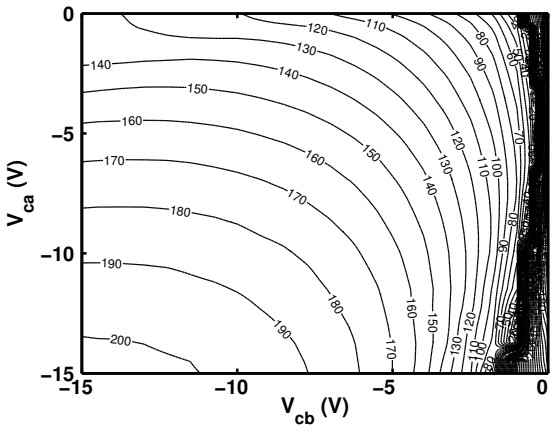



Fig. 6. Four stages phase shifter architecture.

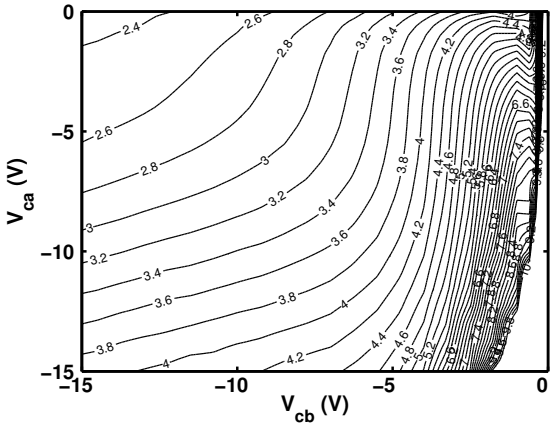
As discussed earlier, the proposed all-pass network phase shifters have a limited phase variation of approximately 48°. The phase shift requirement for this project is 180°. Four identical phase shifters, which are connected in sequence as shown in Fig. 6, can overcome the limited phase shift of each stage. Tuning voltage nodes $V_{ca}$ and $V_{cb}$ are connected separately so that only two tuning voltages are required.

## IV. Experimental Results

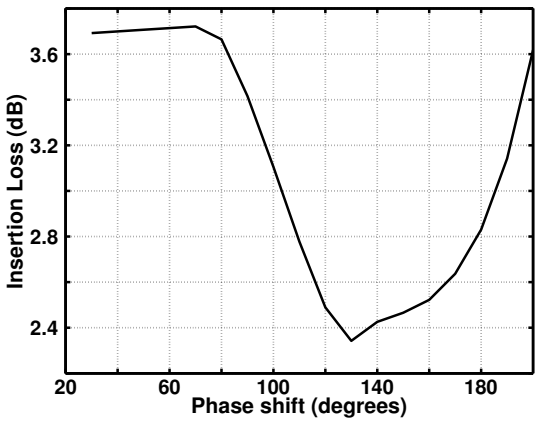
Differential two-port S-parameter measurements were performed after LRM calibration. The two dc control voltages were swept to find optimum pairs of $V_{ca}$,$V_{cb}$. The measured phase shift (=∠S21) and insertion loss at 2GHz are shown in Fig. 7(a) and (b) in the form of contour lines. It must be noted that although the dc control voltages are quite high, very little dc current (on the order of 10$\mu$A), which is the total leakage current of the realized varactor diodes, is required. This phase shifter can achieve continuous phase shift up to 180° with insertion loss less than 3.7dB as shown in Fig. 7(c). The variation of the insertion loss with phase shift is due to




(a) Phase shift contour




(b) Loss contour




(c) Minimum Loss

Fig. 7. (a) Measured phase shift contour lines and (b) measured loss contour lines as a function of control voltages $V_{ca}$ and $V_{cb}$ at 2GHz (c) minimum loss vs. phase shift at 2GHz.

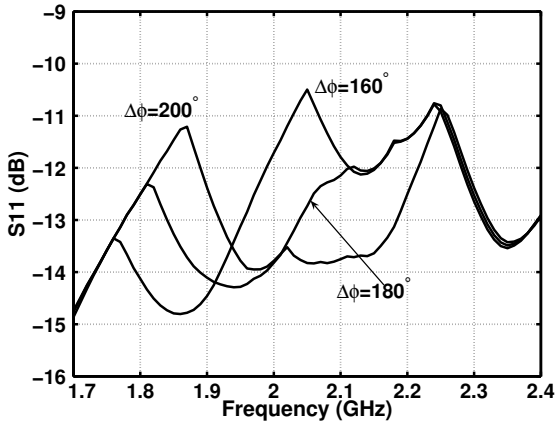



Fig. 8. Measured $|S11|$ of the phase shifter at optimum tuning voltage pairs.

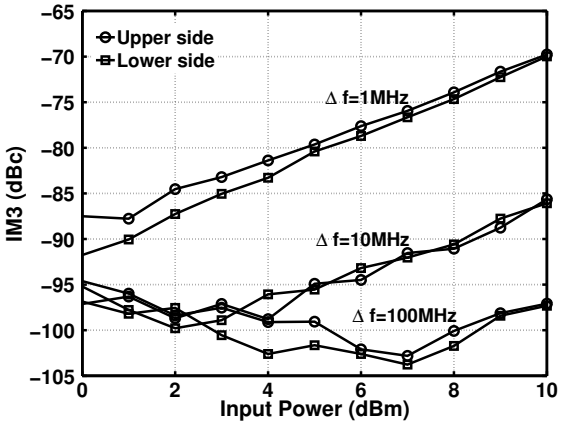



Fig. 9. Measured IM3(dBc) versus frequencies at three different tone-spacings($\Delta f$=1MHz, 10MHz and 100MHz).

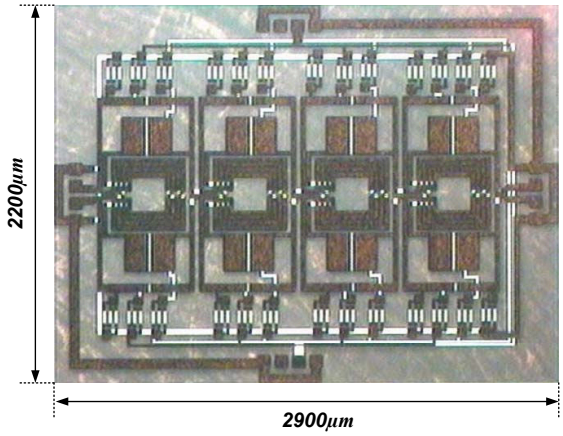



Fig. 10. Microphotograph of the phase shifter realized in silicon-on-glass technology.

the Q factor variation of the varactors with bias. The higher than expected insertion loss is due to the Q factor of the varactor diodes being slightly lower than the desired value for this wafer. The measured phase shifter return losses for three different phase shifts ($\Delta\phi$=160°, 180° and 200°) are shown in Fig. 8 and are better than -10dB. A two-tone test was performed on the phase shifter at 2GHz using a 50Ω differential two-port measurement fixture. For the calibrated power measurement of all frequency components of interest, the linearity of the phase shifter was measured with the load pull system of [12]. Fig. 9 gives the measured IM3 components as function of input power for three different tone-spacings ($\Delta f$=1MHz, 10MHz and 100MHz) for a target phase shift of 80°. IM3 components are less than -70dBm and -85dBm for 1MHz and 10MHz tone-spacing at $P_{in}$=10dBm, respectively. This corresponds to an IIP3 better than +45dBm for 1MHz tone-spacing and +52dBm for 10MHz tone-spacing. The phase shifter circuit has been fabricated in the high performance silicon-on-glass technology. A microphotograph is shown in Fig. 10.

## V. Conclusions

This paper presented a low-distortion phase shifter design based on transformers and low-loss varactor diodes. A very compact, low-power, differential phase shifter has been implemented, which shows very high linearity of IIP3 $\geq$ 52dBm. This makes it possible for this phase shifter to be applied to various demanding applications such as phased array transmitter systems.

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