A Resistively Degenerated Wide-Band Passive Mixer with Low Noise Figure and +60dBm IIP2 in 0.18μm CMOS

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***Abstract* — This paper presents a wide-band CMOS passive Mixer with 8dB Double Side Band (DSB) Noise Figure (NF) and 24dB voltage gain with +60dBm of un-calibrated IIP2 and +9dBm of IIP3 at 2GHz. The linearity is maintained for a wide frequency offset range to ensure interferer performance for in-band jammers. A source degeneration method to improve NF and linearity is introduced and analyzed. G_m boosting methods, such as input cross-coupling, current reuse, complementary input, and back gate connection, are used. The Mixer consumes only 10mW from a 2V power supply for I and Q both channels including trans-impedance amplifier stages (TIA).**

***Index Terms* — Degeneration, Passive Mixer, G_m boosting, IIP2, Noise Figure.**

I. Introduction

CMOS processes have been scaled down to shorter gate lengths to improve overall area and power consumption, while achieving higher unity current gain frequency (f_t). Even though a shorter gate length is helpful for better radio frequency (RF) performance, it introduces more flicker noise (1/f noise) [1]. Especially for narrowband wireless cellular systems, this 1/f noise seriously degrades NF performance.

There have been some efforts to improve the 1/f noise performance of active Mixers [2]-[3]. A PMOS switching pair is reported in [2] and a method of 1/f noise cancellation is introduced in [3]. Another way to mitigate 1/f noise is to use longer channel length devices, since 1/f noise is inversely proportional to the square of the channel length. But using non-minimum channel length FETs will introduce other problems. The parasitic capacitance associated with the gate will be increased, degrading RF performance.

The best way to alleviate 1/f noise is to eliminate DC current in the switching core. This leads to a passive Mixer application. There are several drawbacks to the use of a passive Mixer, but poor NF performance is the main concern.

This paper describes wideband operation of a passive Mixer with low NF and highly linear performance, while consuming 10mW of power from a 2V supply. Section II explains the conventional passive Mixer architecture and related issues. Section III introduces and analyzes a new resistively degenerated passive Mixer topology. Section IV describes individual block design. Section V shows measured results. Section VI concludes the paper.

II. Conventional CMOS passive Mixer

There have been many publications using a passive Mixer architecture to avoid 1/f noise issues [4]-[5]. The most common passive Mixer architecture is "current input and current output", with a TIA stage to provide the low impedance node at the Mixer output, as shown in Fig. 1. The conventional passive Mixer has a high NF due to conversion loss and well known TIA noise amplification [5],

$$\overline{v_{no\_TIA}^{\,2}} = \left(1 + \frac{2 \cdot R_{TIA}}{R_{Mix}}\right)^2 \cdot \overline{v_{ni\_TIA}^{\,2}} \qquad (1)$$

where, v_{no_TIA} is the output noise voltage of the TIA, v_{ni_TIA} is the input referred TIA noise, R_{TIA} is feedback resistance from TIA stage, the factor of two is for doubly balanced operation, and R_{Mix} is the equivalent Mixer output resistance. As can be seen from (1), R_{Mix} needs to be as high as possible to reduce noise amplification of the TIA input referred noise. But the operation frequency is the limiting factor to obtain a high resistance, since R_{Mix} can be expressed by

$$R_{Mix} = \left(f_{LO} \cdot \alpha \cdot \left(C_{p1} + C_{p2}\right) \cdot \left(1 - e^{\frac{-T_{LO}}{\alpha \cdot (C_{p1}+C_{p2}) \beta \cdot R_{on}}}\right)\right)^{-1} \qquad (2)$$

where, C_{p1} is the parasitic capacitance from the output of the preceding stage, C_{p2} is parasitic capacitance from the Mixer cores, R_{on} is the turn-on resistance of the Mixer core, α is the capacitance multiplication factor, which is 2 for single channel and 4 for dual channel (I and Q), and β is the resistance multiplication factor, which is 2 for doubly-balanced Mixer.

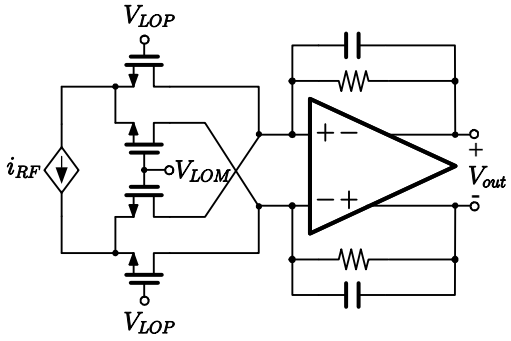

Fig. 1. Conventional Passive Mixer with TIA.

With 500fF of total parasitic capacitance and 2GHz operation, R_{Mix} would be 250Ω for a doubly-balanced Mixer in a dual channel application. Since the usual and very common value for R_{TIA} is about 2~5kΩ, the TIA noise will be amplified by 81~441 times. Therefore, designing a very low noise TIA stage would be challenging while maintaining low power consumption.

III. Resistively Degenerated Passive Mixer

The proposed Mixer Architecture is shown in Fig. 2. R_{deg} is the degeneration resistance and C_c is a high-frequency compensation capacitor.

R_{deg} serves several purposes. First, it provides a higher equivalent resistance, since the equivalent resistance can be modified from (2) to be

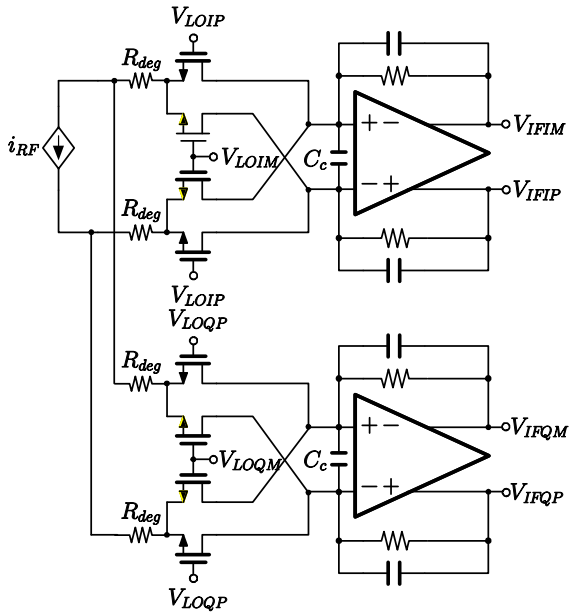

Fig. 2. Proposed Resistively Degenerated Passive Mixer

$$R'_{Mix} = \left(f_{LO} \cdot \left[\alpha \cdot C_{p1} \cdot \left(1 - e^{\frac{-T_{LO}}{[\alpha \cdot C_{p1}][\beta \cdot (R_{on} + R_{deg})]}} \right) + \alpha \cdot C_{p2} \cdot \left(1 - e^{\frac{-T_{LO}}{[\alpha \cdot C_{p2}][\beta \cdot R_{on}]}} \right) \right] \right)^{-1} \quad (3)$$

As can be seen from (3), the equivalent Mixer output resistance is increased since C_{p1} is the dominant parasitic capacitance. The difference between the conventional and proposed passive Mixer is illustrated in Fig. 3. Another issue is that the RF current from preceding stage can not be perfectly separated, due to mismatches in the Mixer cores. All mismatch factors can be modeled and referred to a gate voltage difference, so that the turn-on resistance will be different. This could cause strong second-order distortion in passive Mixers. By adding R_{deg}, the current split can be more balanced, since a poly resistor can be made with a large aspect ratio, which will reduce the resistance mismatch. Therefore, the total resistance seen by the RF current would be R_{deg}+ R_{on}, and variation of this total resistance will be smaller than a conventional passive Mixer if R_{deg}> R_{on}.

Simulated and calculated results for the Mixer output impedance and the noise amplification factor ratio (NA_{ratio}) are shown in Fig. 4. The noise amplification factor ratio is the ratio of conventional vs. proposed passive Mixer for the first term of right side of (1).

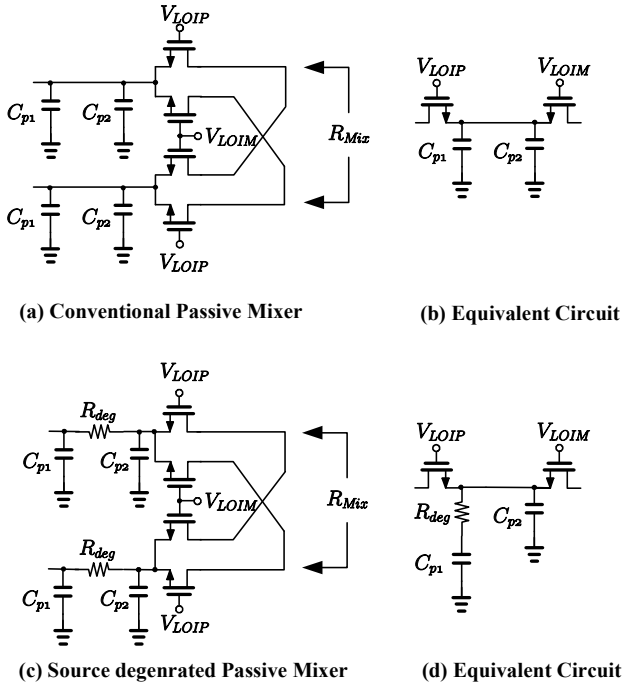

Fig. 3. Difference between Conventional and Proposed Mixer

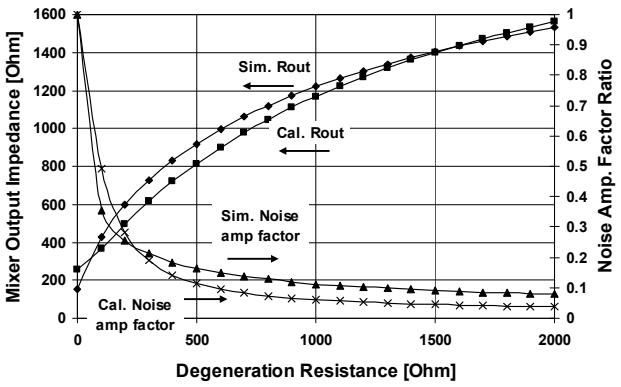

Fig. 4. Simulated and calculated R_{out} and Noise amplification factor.

As is shown in Fig. 4 and (3), the equivalent output resistance saturates when the degeneration resistance is increased further. The gain will decrease, since the RF current from the preceding stage will be decreased compared to the conventional Mixer. This implies that there will be an optimum degeneration resistance value, where NF is minimal but the gain is acceptable. This will be discussed in the next Section.

IV. Mixer Design

The simplified Mixer schematic is shown in Fig. 5. It consists of an input transconductance stage, resistively degenerated passive Mixer core, and TIA.

A. Trans-conductance Stage

The transconductance (G_m) stage converts the RF voltage input to current. Due to the wideband operation requirement, the input stage is designed with a Common Gate (CG). The CG input stage can provide wideband operation but it has a NF penalty. To improve the NF performance of the CG, the cross-coupled method is introduced [6]. But the cross-coupled method can boost the G_m by only a factor of two at best. The G_m can be boosted further with a current reuse complementary input stage, and back gate connection, as shown in Fig. 5. With this additional boosting method, the G_m can be boosted up to three times. The input impedance will be the same as in [6] but the noise factor will be increased to

$$F = 1 + \frac{\gamma}{\delta} \cdot \frac{5}{4 \cdot A + \frac{1}{1+A}}, \quad A = \frac{1}{1 + C_{gs}/C_{cp}} \tag{4}$$

where, δ and γ are the bias dependant constant and C_{cp} is the input cross coupling capacitance [6].

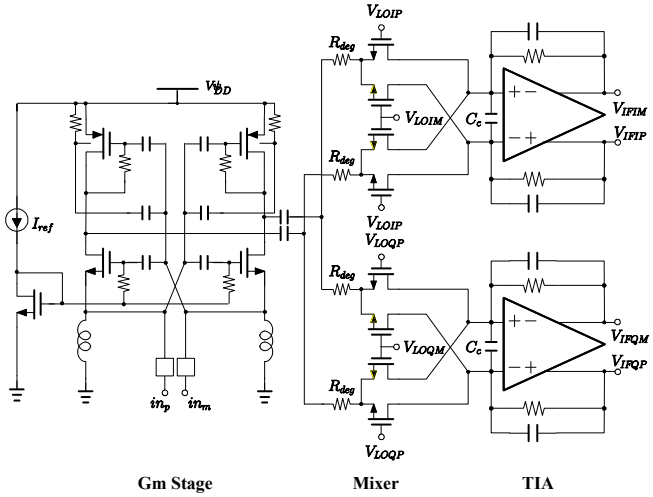

Fig. 5. Simplified schematic of Mixer.

B. Mixer Core Stage

The degeneration resistance value needs to be optimized based on the overall NF and gain performance. The overall gain of the Mixer (G) and the noise factor ratio (F_{ratio}), relative to the conventional case, can be described

$$G \approx \frac{2}{\pi} \cdot G_{m,eff} \cdot R_{TIA}, \quad F_{ratio} = 1 + \frac{NA_{ratio} + \overline{i_n^2}}{G_{m,ratio}^2}$$

$$G_{m,eff} = g_m \cdot (2A+1) \cdot \frac{Z_{out}}{\frac{R_{\deg} + R_{on}}{2} + Z_{out}}, \quad G_{m,ratio} = \frac{1}{1 + \frac{R_{\deg}}{R_{on} + 2 \cdot Z_{out}}} \tag{5}$$

where, Z_{out} is output impedance of the transconductance stage with parasitic capacitance (C_{p1}) and i_n is the Mixer core itself noise contribution. The simulated and calculated value of G and F_{ratio} is shown in Fig. 6. A degeneration resistance of 600Ω was chosen.

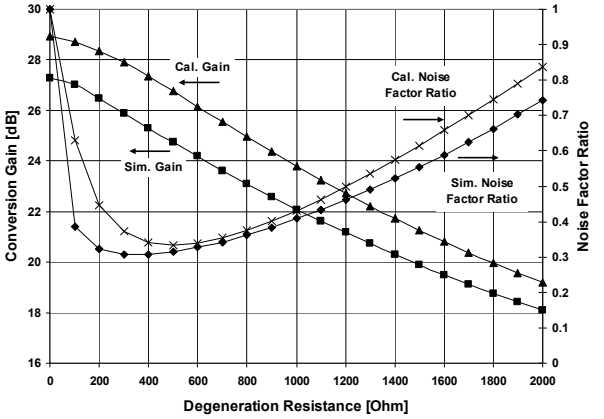

Fig. 6. Simulated and calculated Gain and Noise Factor Ratio.

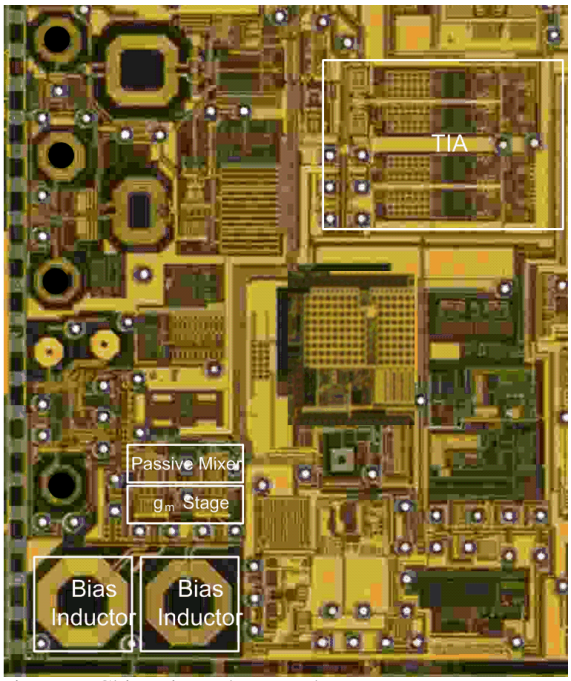

Fig. 7. Chip Micro-photograph

V. Measured Results

The designed Mixer is fabricated in a 0.18μm Si CMOS 5M1P process. The chip micro-photograph is shown in Fig. 7. The measured matching and IIP2 performance are shown in Fig. 8 and Fig. 9, respectively. As can be seen, the 10dB input matching bandwidth is from 1.35GHz to 2.3GHz. The IIP2, without calibration, is more than +60dBm for wide frequency offset range relative to the RF frequency. The IIP2 performance between I and Q channel has almost 10dB of difference, due to stronger coupling to I channel from TIA output.

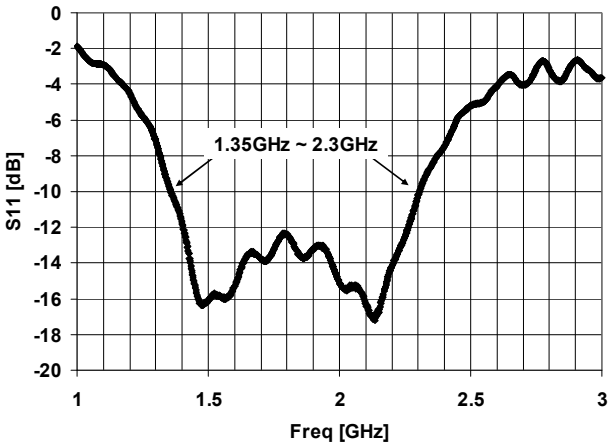

Fig. 8. Measured input matching condition.

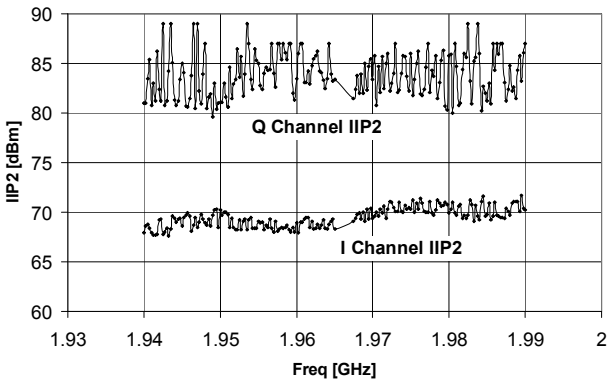

Fig. 9. Measured un-calibrated IIP2 performance.

The IIP3 performance is +9dBm. The DSB NF is 8dB and gain is 24dB. The total current consumption from a 2V supply is 5mA. The G_m stage consumes 1.5mA from each leg and the TIA consumes 1mA for each channel.

VI. Conclusion

A new resistively degenerated wide-band passive Mixer is introduced and analyzed. The analytical results show good agreement with simulated results. Thanks to the proposed architecture, the fabricated passive Mixer shows a low noise figure with more than +60dBm of IIP2 performance.

Acknowledgement

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