

A Low Insertion Loss, High Linearity, T/R Switch in 65 nm Bulk CMOS for WLAN 802.11g Applications

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Abstract – A transmit-receiver (T/R) switch is fabricated in a 65 nm CMOS process for WLAN 802.11g applications. By floating the triple well device, the switch achieves low insertion loss, high power handling capability and good linearity simultaneously. In the transmit mode, the switch features 0.8 dB insertion loss, 29 dBm output P1dB and less than 0.2dB EVM degradation at 24 dBm output power level. In the receive mode, it exhibits 1.6 dB insertion loss and 28dB isolation at 2.45GHz.

Index Terms — WLAN, 802.11, CMOS, T/R switches, triple-well device, EVM

I. INTRODUCTION

Due to the increased popularity of WLAN applications, the demand for lower power and fewer off-chip components has increased. The upcoming 802.11n MIMO standard will require integration of multiple transmitter/receiver chains on the same die [1], which further increases the demand for highly integrated and area efficient designs.

Since there are already solutions for integrating the balun and high power PA on a single chip, the T/R switch becomes the last external component (excluding the crystal) that needs to be integrated on chip to provide the most cost-efficient solution. The major requirements for a T/R switch are low insertion loss, high power handling capability, high linearity, good isolation and reliability.

In today's deep sub-micrometer CMOS process, the low resistivity substrate causes a significant signal loss at high frequency, while at the same time the thin oxide device limits the signal swing and introduces a reliability issue. To meet the switch requirements in a standard CMOS process, several efforts have been deployed. The substrate impedance was raised in [2] by using an inductor to provide a narrowband resonance, but with an area penalty. A transformer based T/R switch was introduced in [3], which was limited to low power applications with complex matching requirements.

Bonding wire inductors were employed in [4], which may cause a yield issue especially in the 5GHz band.

The CMOS T/R switch presented here can withstand more than 29 dBm PA output power with the normal thin oxide 65nm device, by employing a novel floating device scheme. Over the 802.11g operation frequency band, the loss due to the switch is less than 1dB in transmit mode and 1.6 dB in receive mode. Measurement results show that there is almost no EVM degradation caused by the switch, which demonstrates its high linearity.

II. T/R SWITCH CIRCUIT DESIGN

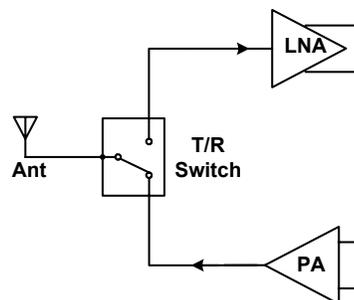


Fig. 1 General T/R switch in 802.11 application.

As shown in Fig. 1, the on-chip T/R switch is located at the input of the LNA and the output of the PA to enable sharing of the antenna between transmitter and receiver. It is required to have low insertion loss, high power handling capability and high linearity, which must be implemented in a standard CMOS process. Furthermore, there are also demands on impedance matching, device reliability and die area efficiency, which make the design even more challenging.

Fig. 2 shows the proposed active T/R switch architecture. It is a three-port network consisting of two regular

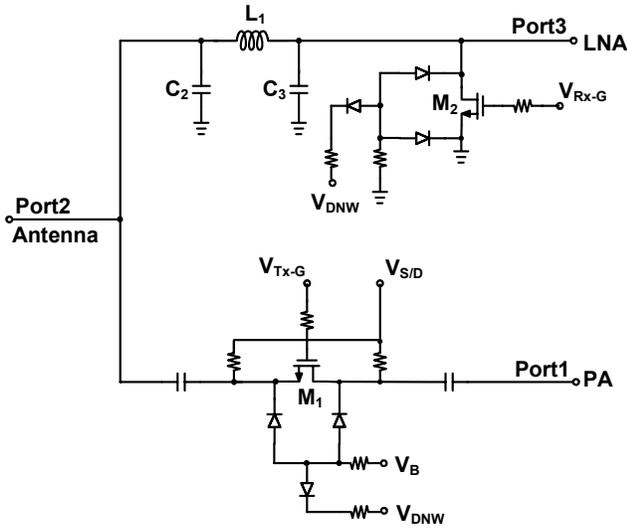


Fig. 2 Proposed T/R switch architecture.

NMOS devices and one π match network. Port 1 and port 3 are connected to the PA output and the LNA input, respectively. Port 2 is the common node to the antenna. Each port of the switch is designed to match to 50Ω , which is generated by the internal matching networks from the LNA input and the PA output. In contrast to the previous passive approach [3], the current switch proposal enables optimizing the matching network design of the LNA and PA separately, eliminating the complex and conflicting impedance matching requirements of the PA and the LNA. In addition, L_1 is part of the LNA matching circuit, further reducing the overall switch area.

A. Transmit Mode

In transmit operating mode, the PA is on and the LNA is off. Both NMOS switches are turned on, with M_1 connecting the PA output to the antenna and M_2 to short the LNA input to ground. With 24 dBm output power from the on-chip PA, M_1 must be able to withstand more than 27 dBm power. The extra 3 dB margin is added by considering the potential impedance variation at the antenna port. The loss introduced by the switch device needs to be minimized as well.

All device terminals are floated in order to handle such a high voltage swing with a regular NMOS device[5]. However, in today's CMOS process, it is impractical to float the substrate and the performance degradation due to the low resistivity substrate would dominate [6][7]. To address this issue, a triple-well NMOS device is selected due to its additional P-well and deep N-well(DNW) structure, which separates the body from the substrate and provides

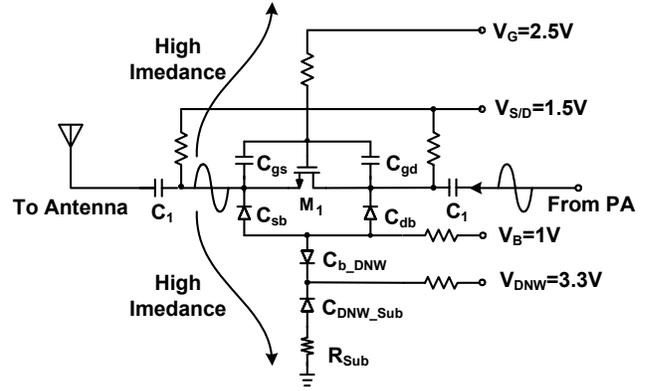


Fig. 3 The triple-well structure and associated NMOS pass gate biasing.

freedom to bias the device body and deep N-well separately.

From the detailed triple-well device structure shown in Fig. 3, selecting the appropriate bias voltages on the source/drain, the DNW and the body can guarantee reverse bias for all diodes. It also provides a high impedance path from the floated device to the lossy substrate. Due to the un-conventional bias condition on the body (1V in this case), the other terminal voltages of the device need to be adjusted as well.

It is observed from both simulations and measurements that M_1 works at higher than 24 dBm power, with less than 1dB loss. Furthermore, floating the bulk connection also improves the linearity. With the high linearity of the small ON-resistor of the transistor, the major nonlinearity mechanism is the signal passing through the nonlinear elements, which, in this case, are the diodes. Strongly reverse-biased diodes prevent the signal current flowing through them to produce the nonlinear voltage at the antenna output, which results in the improved linearity performance.

For this level of power handling and linearity, to keep the diodes reverse biased at all the times during the large output swing, the diodes need to be biased at voltages higher than V_{DD} . However, since the diodes are always reverse biased, no current will be drawn from the high bias voltage source, which makes the approach feasible and the required bias is easily generated on-chip without the need for any external components.

In summary, a triple-well NMOS device, where all terminals have a high impedance with respect to ground, realizes high power handling capability, high linearity and low loss simultaneously in the transmit mode.

In transmit mode, there is a leakage signal from transmitter output into the gate of the LNA input device. Due to the large voltage swings at the antenna, the protection of the LNA thin oxide input device from breakdown needs to be addressed. M_2 is used to short the LNA input to ground in this mode. Furthermore, to minimize the loading effect from the transmitter [2], an L -type impedance transfer network, consisting of inductor L_1 and capacitor C_2 , is formed as shown in Fig. 2. By shorting port 3 to ground with M_2 , the impedance looking toward the receiver is raised, which reduces the transmitter loss through this path. The simulated impedance value is approximate 500Ω , which is determined by the Q of inductor L_1 and the ON-resistance of M_2 .

B. Receive Mode

When the T/R switch operates in the receive mode, both of the switch transistors are turned off. There is high impedance looking toward the transmitter due to the off-status of M_1 , which eliminates the large loading effect from the PA output on the LNA input. On the other hand, due to the off-status of M_2 , the capacitor C_3 forms a π match network with inductor L_1 and capacitor C_2 . Furthermore, by employing M_2 with the triple well device, the received signal loss through this device to the substrate is minimized as well. The measured insertion loss in the receive mode is less than 1.6dB, which is determined by the limited Q of the corresponding π match network.

III. MEASUREMENT RESULTS

The circuit is fabricated in a 65nm RF CMOS process and bonded in a QFN package. Fig. 4 shows the measurement setup for characterizing the key parameters of the T/R switch, where an external PA with 35.5dB gain and 32 dBm OP1dB was used to boost the test signal at the T/R switch input.

In the transmitter mode, by sweeping the power of the network analyzer, the measured S_{21} magnitude at 2.45GHz is shown in Fig. 5. By subtracting the loss from attenuator and cable, the measured output P1dB (OP1dB) of the T/R switch is 29 dBm. The measured phase variation within OP1dB is less than three degrees. In order to test the switch reliability, the measurement was left on for 24 hours with absolutely no performance degradation observed. The measurement demonstrates the extremely high power handling capability and reliability of the floating switch.

The T/R switch insertion loss in the transmitter mode was measured with all the external components bypassed,

as shown as dashed lines in Fig. 4. The measured insertion loss over the 802.11g frequency band is less than 0.8 dB as shown in Fig. 6. Furthermore, to evaluate the system degradation due to the designed T/R switch, an EVM test was performed with a 64 QAM OFDM signal in 54-Mb/s mode. As shown in Fig. 7, with 24 dBm output power at the T/R switch output, there is less than 0.2 dB EVM degradation from the T/R switch, which demonstrates the high linearity as expected.

In receive mode, the measured insertion loss over the 802.11g frequency band is less than 1.6 dB, which is limited by the Q of the π match network. The chip micro-photograph is shown in Fig. 8, with an area of 0.2 mm^2 . Table I gives a summary of the measured T/R switch performance.

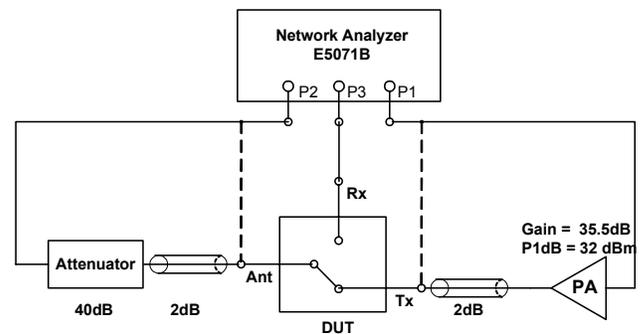


Fig. 4 T/R switch measurement setup.

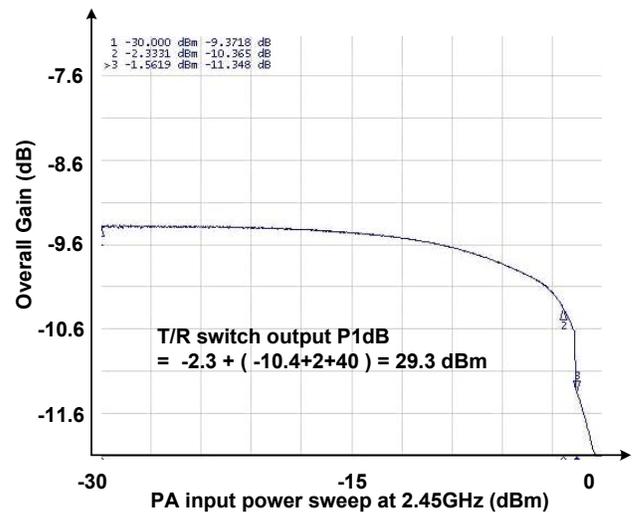


Fig. 5 T/R switch output P1dB.

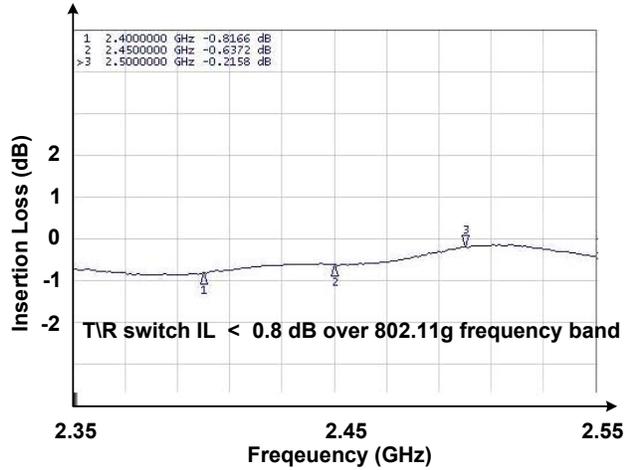


Fig. 6 T/R switch insertion loss in the transmit mode.

Transmitter EVM	Without T/R switch			With T/R switch		
	Result Summary			Result Summary		
No. of Bursts	13			13		
	Min	Mean	Limit	Min	Mean	Limit
EVM All Carriers	5.25	5.27	5.62	5.35	5.38	5.62
	-25.60	-25.57	-25.00	-25.43	-25.41	-25.00
EVM Data Carriers	5.30	5.32	5.62	5.40	5.41	5.62
	-25.52	-25.49	-25.00	-25.35	-25.33	-25.00
EVM Pilot Carriers	4.63	4.65	39.81	4.73	4.76	39.81
	-26.68	-26.65	-0.00	-26.49	-26.46	-0.00
IQ Offset	-53.56	-53.17	-15.00	-53.73	-53.26	-15.00
Gain Imbalance	-0.42	-0.40		-0.47	-0.45	
	-0.04	-0.03		-0.04	-0.04	
Quadrature Error	-0.02	-0.00		-0.02	0.01	
Center Frequency Error	16.73	20.80	+48840	16.35	19.50	+48840
Symbol Clock Error	-0.65	-0.89	+20	-0.75	-1.03	+20
Burst Power	26.55	26.55		21.88	21.88	

Fig. 7 Transmitter EVM with and without T/R switch (Including 4dB cable loss when measured with T/R switch).

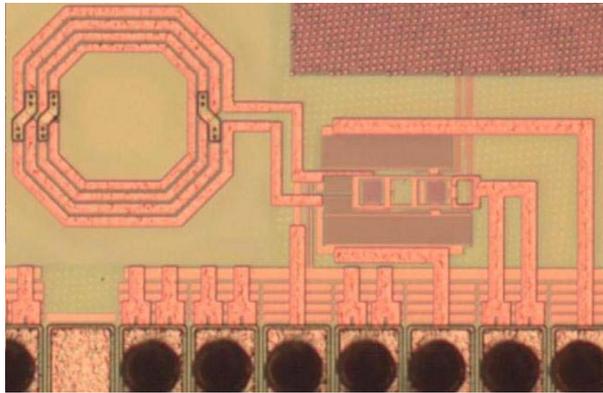


Fig. 8 T/R switch microphotograph.

TABLE I. T/R Switch Performance Summary

	Measured	Units
Operation Frequency	2.35 – 2.55	GHz
Insertion Loss in Tx mode	< 0.8	dB
Insertion Loss in Rx mode	< 1.6	dB
Output P1dB	29	dBm
EVM degradation at 24 dBm	< 0.2	dB
S11, S22, S33	< -10	dB
Port to Port Isolation	28	dB
Current Consumption	0	mA
Technology	65 nm CMOS	
Active Area	0.2	mm ²

IV. CONCLUSION

A 2.45GHz 65 nm CMOS T/R switch is presented. The switch features 0.8 dB insertion loss, 29 dBm output P1dB and less than 0.2dB EVM degradation at 24 dBm output power level in transmit mode. In the receiver mode, it exhibits 1.6 dB insertion loss and 28dB isolation. These results demonstrate that a high performance, highly integrated T/R switch is achievable in a deep sub-micrometer CMOS process.

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