

A 24-GHz CMOS Passive Subharmonic Mixer/Downconverter for Zero-IF Applications

Rahul M. Kodkani, *Member, IEEE*, and Lawrence E. Larson, *Fellow, IEEE*

Abstract—The design and implementation of a 24-GHz subharmonic-mixer-based downconverter based on a multiphase local oscillator (LO) is presented. Fabricated in a 0.13- μm CMOS process, the downconverter includes a pre-amplifier and an IF buffer and consumes 14.4 mW from a 1.6-V supply. The quadrature LO buffer consumes 15 mA at 1.2 V. The circuit includes a single-ended to differential phase splitter for the LO. The downconverter has a conversion gain of 3.2 dB and double-sideband noise figure of 10 dB. The measured input referred 1-dB compression point is -12.7 dBm. DC offsets were less than 2 mV.

Index Terms—CMOS, direct-conversion receiver, millimeter-wave integrated circuits, passive mixer, subharmonic mixer (SHM), 24 GHz.

I. INTRODUCTION

GIGABIT-PER-SECOND wireless data is now possible in high-frequency millimeter-wave and near-millimeter-wave bands, and the use of silicon technology provides an opportunity for deployment of these systems at low cost [1]–[3]. Unlicensed bands around 24 and 60 GHz provide high bandwidth enabling high-speed wireless networks. Current CMOS and SiGe technologies offer high f_T and f_{MAX} well over 100 GHz. In addition to the evolving silicon technologies, phased-array and multiple-input multiple-output (MIMO) systems can lead to exciting applications such as automotive radar and wireless HDTV. This paper presents a 24-GHz CMOS subharmonic mixer (SHM) for low-power phased-array applications.

Several design issues such as $1/f$ noise in mixers and dc offsets make the design of a direct-conversion receiver extremely challenging. The $1/f$ noise of the mixers is critical since it falls within the baseband bandwidth. Another design issue in direct-conversion receivers is dc offsets due to local oscillator (LO)-RF feedthrough [4]. A passive subharmonic downconverter can overcome both of these issues [5], [8]. In an SHM, the LO is a subharmonic of the RF frequency. As shown in Fig. 1, any LO leakage into the RF port and subsequent self-mixing will not cause a dc offset due to the subharmonic mixing action. Another advantage of using an SHM for these high-frequency applications is the potential LO phase-noise improvement. The LO can now be generated at a fraction of the RF frequency, which can lead to lower phase noise. For the same technology,

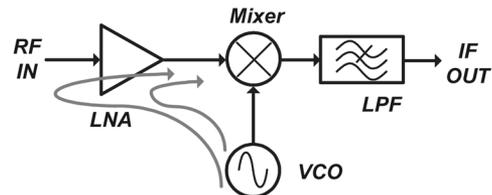


Fig. 1. LO-RF feedthrough in direct-conversion receivers.

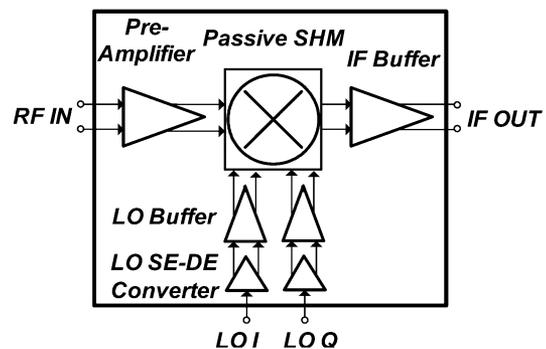


Fig. 2. Block diagram of complete passive SHM-based downconverter.

the phase-noise performance of a voltage-controlled oscillator (VCO) at a lower LO frequency is better than that of a higher LO frequency [6]. If the LO is obtained by dividing a signal generated at twice the LO frequency, a 6-dB improvement in phase noise can also be achieved.

An integrated downconverter for use in zero-IF receivers using a passive SHM is shown in Fig. 2. It includes a pre-amplifier, a passive SHM, an IF buffer, and LO buffers. The design and measurement results of this downconverter, implemented in a 0.13- μm CMOS technology, are discussed [7]. In a complete direct-conversion in-phase/quadrature (I-Q) receiver, two such downconverters are needed. In Section II, the design and analysis of the double-balanced passive SHM based on multiphase switching is described.

This mixer topology does not consume any dc power and, hence, is ideally devoid of $1/f$ noise. In addition, it does not have any dc offset under ideal conditions owing to its subharmonic mixing function. The pre-amplifier used to compensate for the loss in the passive SHM is described in Section III, while the LO and IF circuits are described in Section IV.

An integrated mixer/downconverter, which includes the passive SHM, a low-noise pre-amplifier, and the associated LO and IF buffers, is fabricated in the IBM CMOS 8RF process [7]. The measurement results are presented in Section V.

Manuscript received September 1, 2007; revised February 12, 2008. This work was supported by the University of California under a Discovery Grant.

The authors are with the Department of Electrical and Computer Engineering, University of California at San Diego, La Jolla, CA 92093 USA (e-mail: rkodkani@ucsd.edu; larson@ece.ucsd.edu).

Digital Object Identifier 10.1109/TMTT.2008.920177

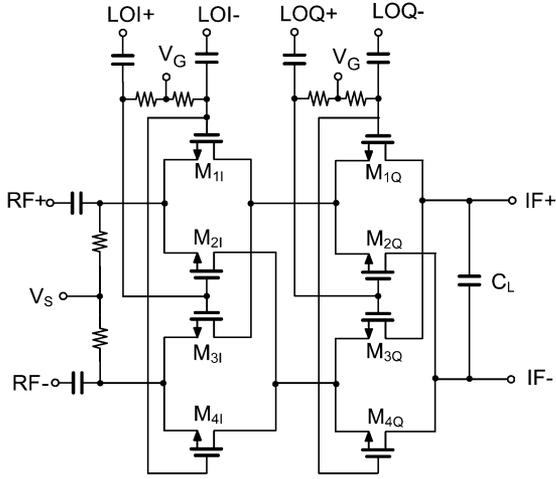


Fig. 3. Schematic of the SHM.

II. CMOS PASSIVE SHM

A. Passive SHM Topology

The core of the downconverter is the passive SHM. The 24-GHz RF is mixed with an LO at half the RF frequency i.e., 12 GHz to downconvert to baseband. Fig. 3 shows the schematic of the SHM. By successive mixing with quadrature LO signals, one can obtain subharmonic mixing [5], [8]. This topology is balanced for RF, LO, 2LO, and IF signals. Transistors M_{1I} – M_{4I} form a regular double-balanced passive mixer. M_{1Q} – M_{4Q} form the second stage of the passive SHM.

To understand the operation of the mixer, consider the switching behavior in one complete cycle of the LO, as shown in Fig. 4. In the first quarter-cycle, transistors M_{1I} , M_{4I} and M_{2Q} , M_{3Q} are on, modulating the current to the IF port. In the second quarter cycle, the current is modulated through M_{1I} , M_{4I} and M_{1Q} , M_{4Q} , thus reversing the polarity. It can be observed that in one complete cycle of the LO, the RF current is modulated four times, and hence, at twice the LO frequency. Subharmonic square-wave mixing is thus obtained. The circuit can, therefore, be viewed as a passive mixer with square-wave switching at twice the LO frequency.

B. SHM Conversion Gain

As explained in Section II-A, the RF current is modulated four times in one complete LO cycle. In each reversal, four transistors are on, as compared to two being on in a regular passive fundamental order mixer. Although each transistor is on for 50% of the LO duration, the RF current is effectively modulated by a square wave at twice the LO frequency.

The mixer switches can be represented by time-varying conductances and the mixer can be represented by a model consisting of these conductances, as shown in Fig. 5. Here, C_L is the load capacitance.

For large LO drives, the time-varying conductance of the individual switches can be assumed to be a square wave. For transistor M_{1I} , it is given by [9]

$$g(t) \approx \begin{cases} g_{\max}, & \text{when switch is ON} \\ 0, & \text{when switch is OFF} \end{cases} \quad (1)$$

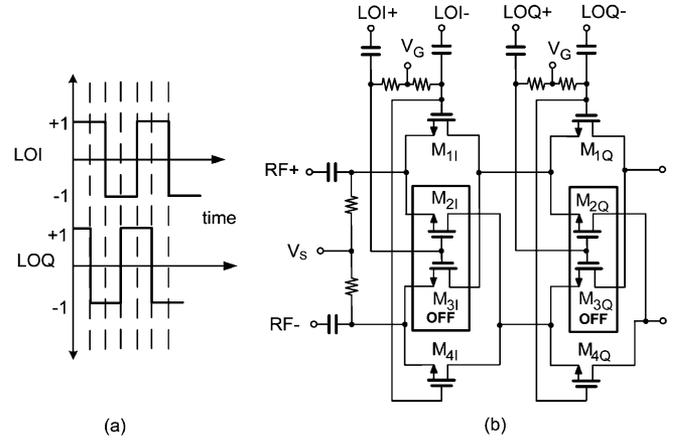


Fig. 4. Subharmonic switching in the mixer. (a) LO waveforms. (b) Mixer operating in noninverting configuration. (c) Mixer operating in inverting configuration.

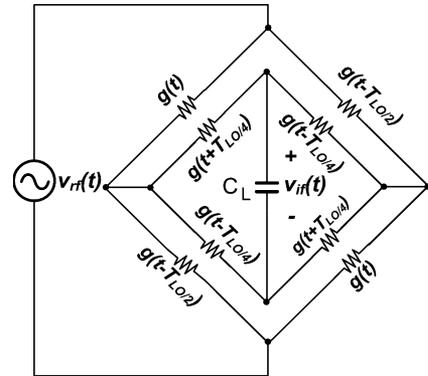


Fig. 5. Equivalent time-varying conductance model of the SHM.

where g_{\max} is the maximum value of the time-varying conductance and is given by

$$g_{\max} = \mu_n C_{\text{ox}} \frac{W}{L} (V_{\text{LO}} - V_{\text{CM}}) \quad (2)$$

where $V_{\text{CM}} = V_S + V_{\text{TH}} - V_G$. Here, μ_n is the electron mobility of the nMOS switches, C_{ox} is the oxide capacitance per unit area, V_{LO} is the LO amplitude, V_S is the dc voltage at the drain and the source of the switches, V_{TH} is the threshold voltage, and V_G is the common mode voltage at the gate of the switches.

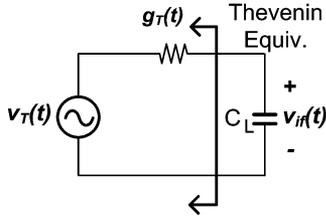


Fig. 6. Thevenin equivalent of the mixer.

The time-varying conductance of transistors M_{1Q} , M_{2I} , etc. are just phase-shifted versions of the above expression.

To understand the mixing operation, consider the Thevenin equivalent across C_L , as explained in [10]. The mixer can be represented by the Thevenin equivalent, as shown Fig. 6. The open circuit Thevenin voltage across the load capacitor is given by

$$v_T(t) = m(t)v_{rf}(t). \quad (3)$$

The mixing function $m(t)$ is defined as the time domain transfer function from the input RF voltage to the open-circuit voltage across the load. In the absence of the load capacitance,

$$v_{if}(t)|_{C_L=0} = v_T(t) = m(t)v_{rf}(t). \quad (4)$$

The Thevenin's equivalent conductance seen from the load capacitor is given by (6). For a square-wave LO drive, the two terms in the numerator of the mixing function $m(t)$, given by (5), are square waves switching between $+g_{\max}$ and $-g_{\max}$, but with 90° phase shift. The two denominators both take a constant value of g_{\max} . Hence, the mixing function is a product of two square waves switching from $+1$ to -1 and quadrature in-phase, resulting in another square wave switching between $+1$ or -1 at twice the LO frequency, as shown in Fig. 7. Subharmonic mixing with twice the LO frequency is thus obtained

$$m(t) = \frac{\left\{ \frac{g(t) - g(t - T_{LO/2})}{g(t) + g(t - T_{LO/2})} \right\} \left\{ \frac{g(t - T_{LO/4}) - g(t - T_{LO/4})}{g(t - T_{LO/4}) + g(t + T_{LO/4})} \right\}}{1} \quad (5)$$

$$g_{eq}(t) = \frac{\{g(t) + g(t - T_{LO/2})\} \{g(t - T_{LO/4}) + g(t - T_{LO/4})\}}{4\{g(t) + g(t - T_{LO/2}) + g(t - T_{LO/4}) + g(t - T_{LO/4})\}}. \quad (6)$$

In the frequency domain, the mixing function is represented by odd harmonics of $2LO$,

$$m(t) \approx \frac{4}{\pi} \sum_{\substack{n=1 \\ n \text{ odd}}}^{\infty} \left(\frac{1}{n} \right) \cos(2n\omega_{LO}t). \quad (7)$$

Thus, the conversion loss of the mixer, defined as the ratio of the IF current to the input RF, under ideal conditions is calculated

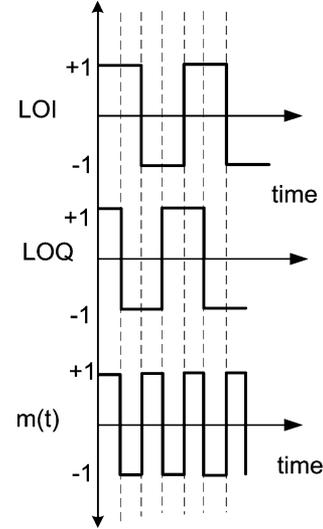


Fig. 7. Mixing function of the passive SHM.

from the product of the mixing function fundamental with the RF frequency and is given by

$$CL = \frac{\pi}{2} = 3.9 \text{ dB}. \quad (8)$$

In general, the conversion loss for each odd harmonic mixing product is given by

$$CL(n, f_{RF} \pm 2nf_{LO}) = \frac{\pi \cdot n}{2} \quad (9)$$

where n is the n th odd harmonic of LO.

The preceding analysis assumes a $C_L = 0$. With a finite load capacitance, C_L , however, the analysis is more complicated. It has been shown using the superposition integral, that for this case, the mixing function of a passive fundamental order mixer is modified by a factor as derived in [10]

$$m'(t) = \frac{g_{eq}(t)}{g_{eq\max}} m(t) \quad (10)$$

where $g_{eq\max}$ represents the peak value of the equivalent conductance g_{meq} . The modified mixing function is also a square wave with a period of $(1/f_{2LO})$ if a square-wave approximation for the LO signal is assumed.

It is noteworthy that the conversion loss under ideal conditions of the passive SHM is the same as that of a fundamental mixer. Subharmonic mixing is obtained only when a direct path from RF to IF ports is obtained, when two series switches are on. Thus, the cascaded stages are correlated [8]. The mixer is not equivalent to multiplying by two quadrature signals, which would lead to a conversion loss of $(\pi/2)^2$ or 7.8 dB. This is also explained by the mixer multiplying function m , which is a square wave at twice the LO frequency.

The conversion gain of the mixer is robust to phase errors in the quadrature LO signals. As shown in Fig. 8, a phase error of $\Delta\theta$ leads to a duty cycle error in the mixing function m' . The time delay due to the phase error is given by

$$\Delta t = \Delta\theta \left(\frac{T}{\pi} \right). \quad (11)$$

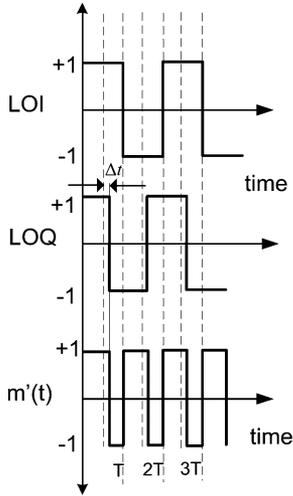


Fig. 8. Effect of phase error on mixing function.

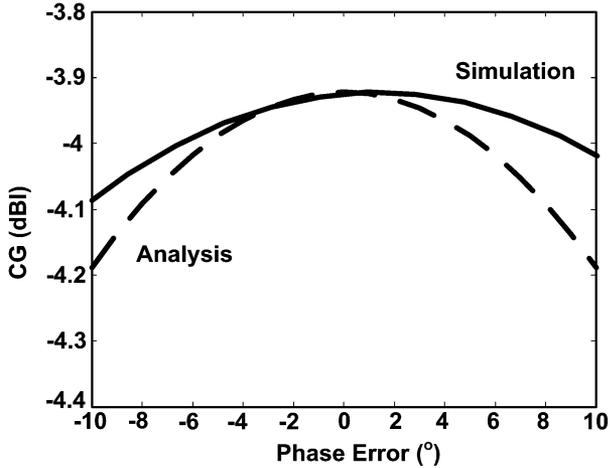


Fig. 9. Effect of quadrature phase errors on conversion gain.

The fundamental term in the Fourier series expansion of the mixer function, which is at twice the LO frequency, is given by

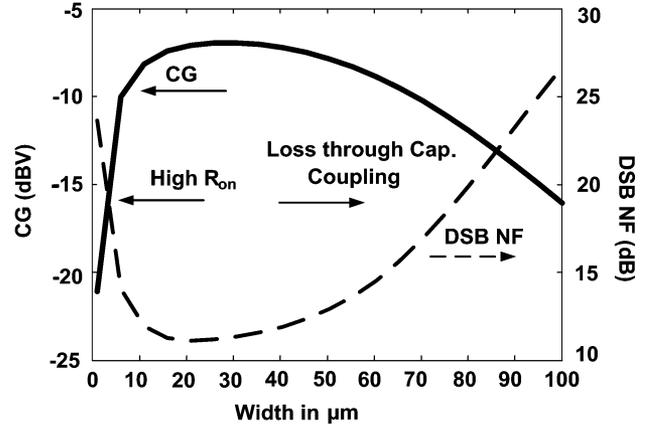
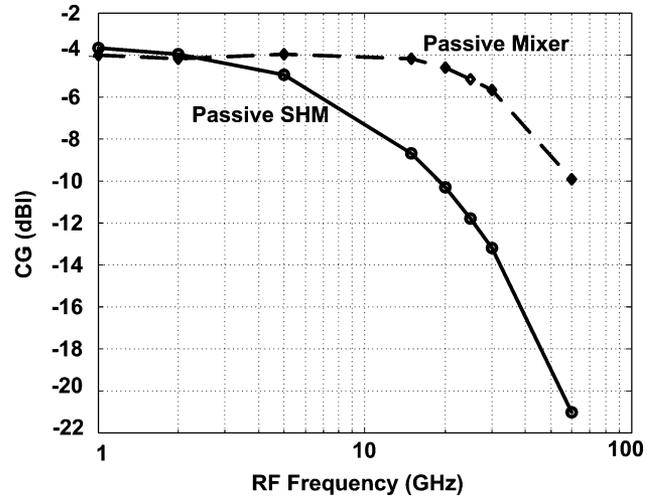
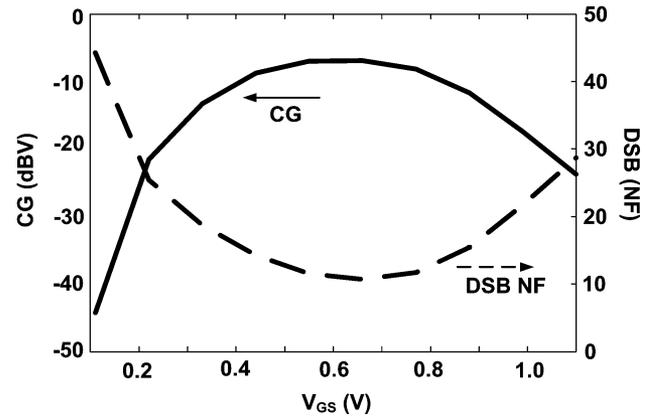
$$m'(2f_{LO}) = \frac{4}{\pi} \cos^2(\theta). \quad (12)$$

Hence, the conversion gain modifies to

$$CG_{\Delta\theta} = \frac{2}{\pi} \cos^2(\theta). \quad (13)$$

The simulated and analytical conversion gain based on (13) is shown in Fig. 9. It is observed that for a phase error of $\pm 10^\circ$, there is less than ± 0.3 -dB reduction in the current conversion gain of the mixer.

In the case of a direct conversion receiver, it should be noted that four differential phases of the LO i.e., 0° – 180° , 45° – 135° , 90° – 270° , and 225° – 315° will be needed for quadrature operation. These can be readily generated using techniques such as multiple-phase VCOs [2] or I/Q summing techniques [11].

Fig. 10. Simulated performance dependence on width of the nMOS switches with $f_{RF} = 24$ GHz, $f_{IF} = 10$ MHz, resistive load of 1 k Ω .Fig. 11. Simulated short-circuit current loss RF frequency response for $f_{IF} = 10$ MHz, $W_g = 30$ μm , $L_g = 0.13$ μm .Fig. 12. Simulated dependence of conversion gain and noise figure on dc bias with $f_{RF} = 24$ GHz, $f_{IF} = 10$ MHz, $W_g = 30$ μm , $L_g = 0.13$ μm , $R_L = 1$ k Ω .

C. Mixer Design

Three important design parameters for the mixer are the size of the switching transistors, the LO drive, and the switching duty

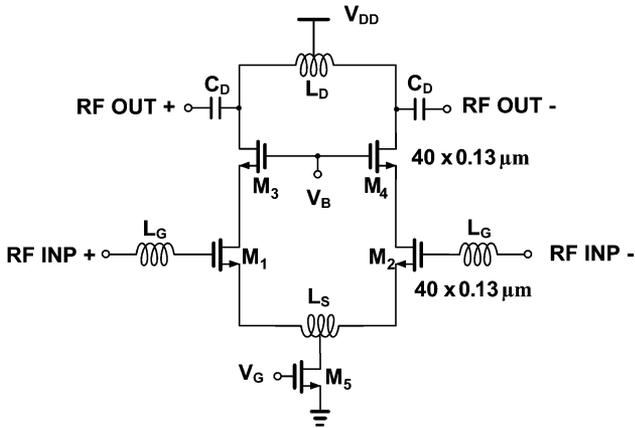


Fig. 13. Schematic of the low-noise pre-amplifier.

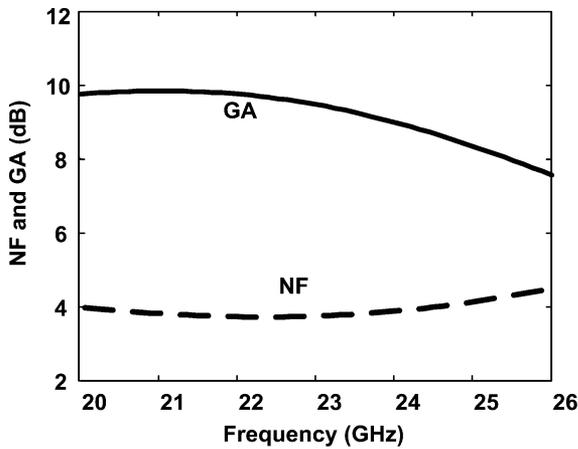


Fig. 14. Simulated available gain and noise figure of the pre-amplifier.

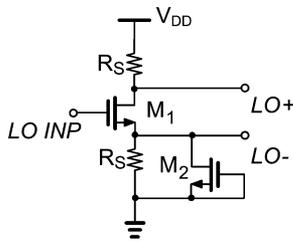


Fig. 15. Schematic of the single-ended-to-differential phase splitter.

cycle. In this section, the optimization of these parameters is discussed.

As explained in [9], the noise figure and conversion loss depend on the mixing function and conductance of the switches under nonideal conditions, which include imperfections in the square-wave switching. High switch conductance is essential for good noise and gain performance. The width of the transistors is a key parameter in determining the conductance. Larger devices have a lower on resistance and, hence, should result in lower loss and noise figure. From (1), it would seem that making the transistors as wide as possible would give the best performance. However, at high frequencies, there is high capacitive coupling to the substrate through parasitic capacitances such as the drain–bulk capacitance C_{db} , and the source–bulk capacitance C_{sb} , leading to losses due to the substrate resistance.

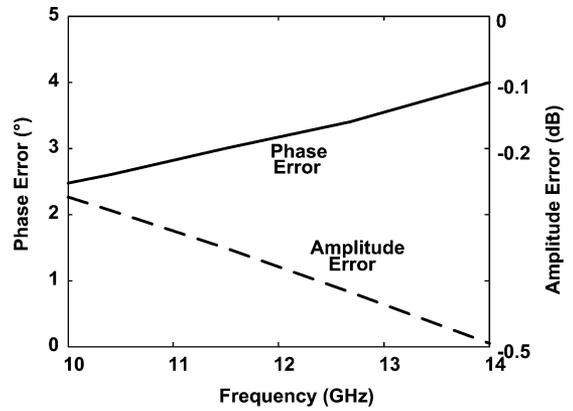


Fig. 16. Simulated gain and phase mismatch in the phase splitter.

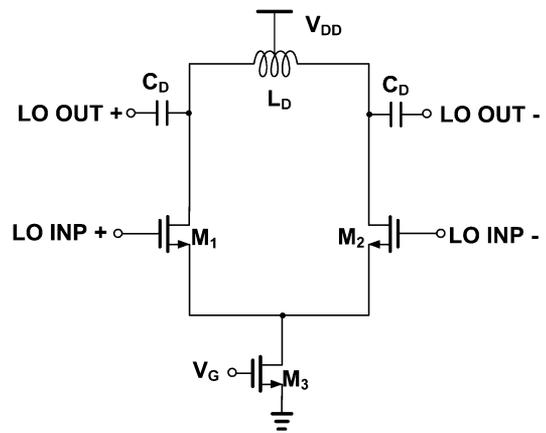


Fig. 17. Schematic of the LO buffer.

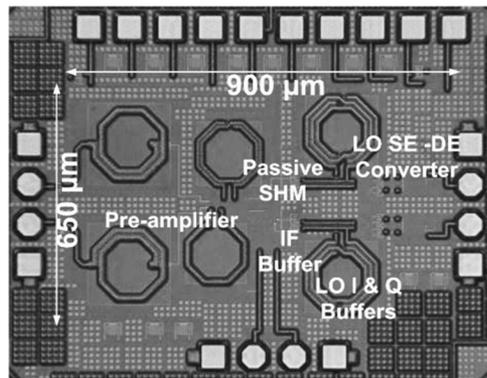


Fig. 18. Chip microphotograph.

This loss mechanism has been examined in [12] in T/R switches used for time-division duplexing communication systems. The capacitive coupling to the substrate increases with the width of the transistors. Increasing the width increases the capacitive coupling and, hence, the losses through the substrate. The dependence on the transistor width of the conductance and capacitive-coupled losses lead to an optimum width for the transistor, similar to T/R switches, as explained in [12]. Fig. 10 shows the simulated conversion voltage loss and double-sideband (DSB) noise figure as a function of device width for RF of 24 GHz, and IF of 10 MHz with a resistive load of 1 kΩ.

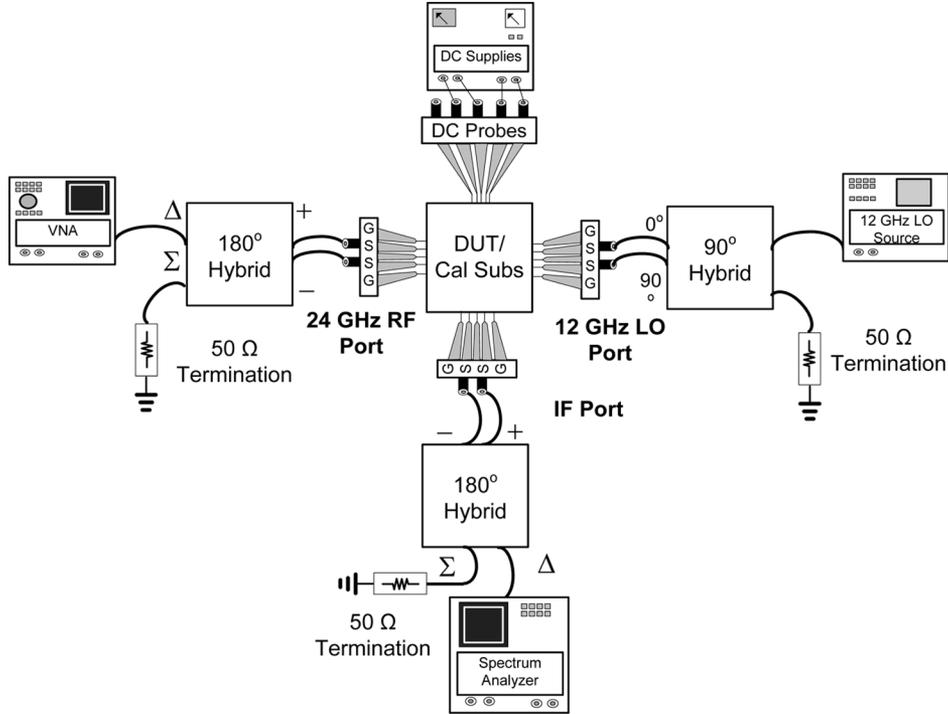


Fig. 19. Measurement setup.

An optimum size of $30 \mu\text{m} \times 0.13 \mu\text{m}$ was chosen where the conversion loss and the noise figure were minimized.

The effect is even more pronounced in the passive SHM due to the cascading of two switches during each modulation. To simulate the current conversion loss, the IF port is shorted and the RF port is driven by an ideal current source. Fig. 11 shows a plot of simulated short-circuit RF-IF current conversion loss. A comparison with the fundamental passive mixer is also shown. At low frequencies, the current loss is approximately 4 dB, as expected from (8). However, at higher frequencies, the modulating currents find a path to ground through the substrate resistance and the parasitic source-bulk and drain-bulk capacitances. This results in a reduction of the current gain at the IF port. The passive SHM has four switches turned ON at any given time. In comparison, a traditional passive mixer has only two switches ON at any given time. As a result, the current loss in the SHM is larger at higher frequencies. It is important to note that despite the higher current loss in the SHM at these frequencies, there are several advantages. As explained in Section I, SHMs have reduced dc offsets and can operate with better phase noise. At high frequencies, the LO path routing and buffering needed for multiple element phase array systems can be complicated [2]. The use of SHMs can ease this requirement since the LO is now at half the RF frequency, giving an additional benefit over the fundamental order mixer.

The gates of these transistors are driven by 12-GHz quadrature signals. The transistors should switch 50% duty cycle for best noise and conversion loss performance. This is achieved by a biasing the gate at a voltage that is above the source by the threshold voltage of the transistor. Fig. 12 shows the simulated conversion loss and noise figure as a function of the dc

gate-source voltage for an RF of 24 GHz, IF of 10 MHz, and a resistive load of 1 k Ω .

Another important parameter is the LO switching amplitude. As in most switching mixers, a larger LO amplitude leads to a smaller time-window where the two opposite switches are on. This reduces the losses and, hence, the noise contributions of the switches as well. As explained by (2), with a large LO amplitude, the switch conductance is also increased, reducing the resistive losses through the mixer. A 1.8-V differential peak-to-peak swing was chosen to reduce the losses due to the ON resistance.

In use as a direct-conversion mixer, the second-order intermodulation intercept point (IIP2) plays an important role. Ideally, in a completely balanced mixer, the second-order nonlinearities are common mode and cancel out when measured differentially. However, mismatches in the component values can cause common-mode to differential conversion leading to finite IIP2 [13]. To compare the IIP2 of the passive SHM and the passive fundamental-order mixer, Monte Carlo simulations with process and mismatch errors in the devices were carried out. Since there are twice the number of devices in the passive SHM, the effect of mismatch and symmetry is more pronounced than as compared to the passive fundamental order mixer. The simulated mean of the IIP2 of the passive SHM was 44.7 dBm, as compared to 50.6 dBm for the passive fundamental order mixer.

III. LOW-NOISE PRE-AMPLIFIER

To compensate for the conversion loss in the passive mixer, a low-noise pre-amplifier is used. A standard differential cascode amplifier, designed using the power-constrained noise op-

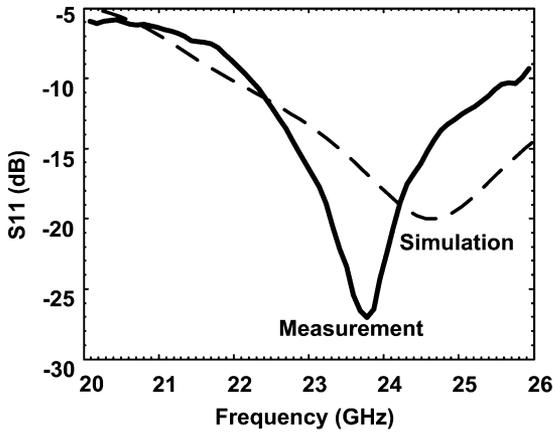


Fig. 20. Measured input return loss.

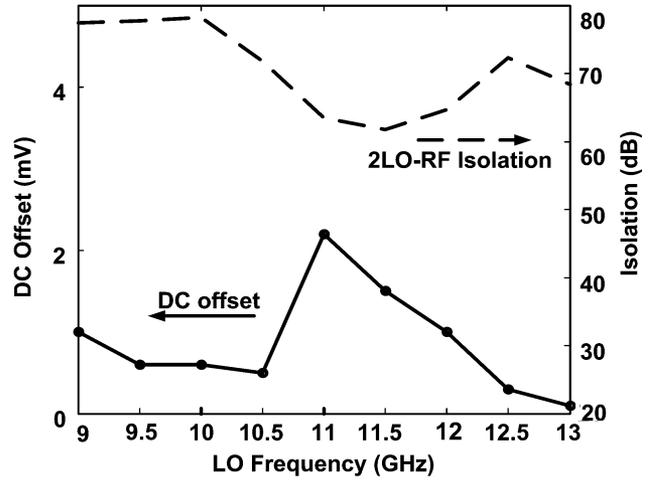


Fig. 23. Measured 2LO-RF isolation and dc offset.

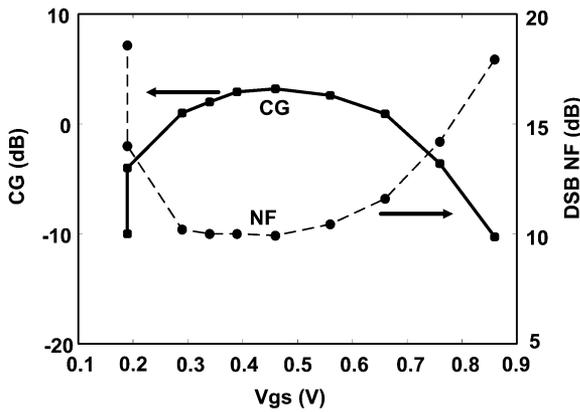


Fig. 21. Measured conversion gain and noise figure with varying V_{GS} .

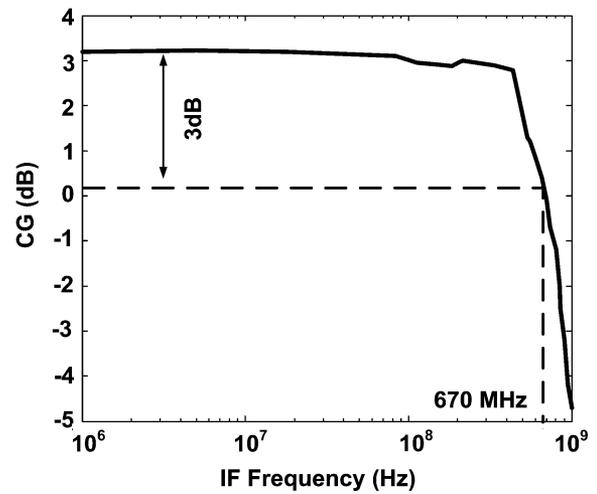


Fig. 24. Measured IF 3-dB bandwidth.

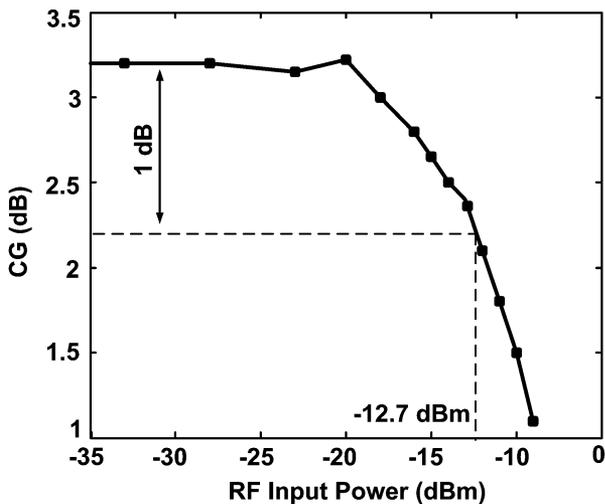


Fig. 22. Measured input-referred 1-dB compression point.

timization method, is used for this purpose [14]. Fig. 13 shows the schematic of the pre-amplifier. Multiple fingers are used to reduce the gate resistance noise contribution.

TABLE I
MEASURED PERFORMANCE PARAMETERS OF THE DOWNCONVERTER

Parameter	Performance
RF Frequency	24 GHz
LO Frequency	12 GHz
Supply Voltage	1.6 V
Current Consumption	13.6 mA
RF pre-amp and IF buffer	15 mA
Conversion Gain	3.2 dB
Noise Figure (DSB)	10 dB
RF Input Return Loss S11	< -15 dB
IF 3 - dB Bandwidth	670 MHz
Input 1 dB Compression Point	-12.7 dBm
IIP2	18 dBm
2LO-RF Isolation	> 60 dB
DC Offset	< 2 mV

A differential source inductor and gate inductor are used at the drain and source to provide input matching to a 100-Ω differential source. The pre-amplifier draws 5 mA at 1.6 V. Simulations show a gain and noise figure of 9.4 and 3.8 dB, respectively, as shown in Fig. 14.

TABLE II
PERFORMANCE COMPARISON WITH RECENT MIXERS

Reference	Frequency (GHz)	CG (dB)	DSB NF (dB)	IP1dBm (dBm)	Core Power (mW)	Topology	Technology
[3]	24	13	14.5	-	40.5 includes IF Amp.	Gilbert Cell	0.18 μm CMOS
[8]	2.2	4.5	11	-10	7.2 includes pre-amp.	Passive Double Bal. SHM	0.13 μm CMOS
[18]	24	2	-	10	-	PMOS Folded Gilbert Cell	0.18 μm CMOS
[19]	10	13	24	-15	6.6	Leveled-LO SHM	2 μm GaInP/GaAs HBT
[20]	28	-11	8.6	-2.7	0.64	Passive Unbal. with LO Doubler	0.18 μm CMOS
[21]	30	-2.6	10.5	-10.5	20	Single Bal. Gilbert Cell	90 nm CMOS
[22]	19	1	6	-12	6.9	Gilbert Cell	0.13 μm CMOS
This Work	24	3.2	10	-12.7	13.6 includes pre-amp. and IF amp.	Passive Double Bal. SHM	0.13 μm CMOS

IV. LO AND IF CIRCUIT DESIGN

A. LO Single-Ended to Differential Phase Splitter

To convert an external 12-GHz single-ended LO to the differential LO needed for the mixer, a simple resistor loaded common-source stage with resistive degeneration is used, as shown in Fig. 15.

The capacitance of a dummy transistor M_2 connected at the source of M_1 helps in balancing the phase and amplitude inaccuracies due to the imbalance in the impedance seen at the drain and the source at high frequencies [15]. The imbalance in the capacitance at the drain and source is mainly due to the Miller effect on the capacitance C_{gd} of M_1 . Due to the unity gain of the phase splitter, the capacitance on the drain of M_1 is approximately twice the value of C_{gd} . The transistor M_1 is sized $20 \mu\text{m} \times 0.12 \mu\text{m}$. The dummy transistor M_2 has a width of approximately twice that of M_1 to balance these capacitances. As shown by Fig. 16, simulations indicated less than 0.5-dB amplitude mismatch and less than 4° phase error in a 10–14-GHz bandwidth. The phase-splitter consumes 2.5 mA with a 1.2-V supply.

B. LO Buffer Design

As explained earlier, for low conversion loss and noise figure, a high LO swing is needed. To obtain a high LO differential peak-to-peak swing of 1.8 V, an inductive loaded differential pair is used as the LO buffer. To obtain the same swing with a resistive loaded differential pair, the power consumption is Q^2 times higher than that using an inductive loaded differential pair with a differential inductor with a quality factor of Q . The differential inductor resonates with the capacitance seen at the gate of the switches of the passive SHM. The schematic of the LO buffer is shown in Fig. 17. The transistors M_1 and M_2 are sized $40 \mu\text{m} \times 0.12 \mu\text{m}$. Each LO buffer consumes 5 mA at 1.2 V.

C. IF Buffer

The IF buffer is a simple nMOS differential pair with 100- Ω resistive loading. A tradeoff between $1/f$ noise and bandwidth limits the size of transistors to $350 \mu\text{m} \times 0.8 \mu\text{m}$. The simulated

$1/f$ corner is approximately 2 MHz. The buffer is designed for 1.5-dB gain and a bandwidth of 700 MHz.

V. MEASUREMENT RESULTS

The circuit is fabricated in a seven-metal-layer IBM 8RF 0.13- μm CMOS process [16]. The chip microphotograph is shown in Fig. 18. The active die area including the pre-amplifier, mixer, LO, and IF circuits is $0.9 \text{ mm} \times 0.65 \text{ mm}$.

A. Measurement Setup

The measurement setup is shown in Fig. 19. A coaxial 180° hybrid was used for generating the 24-GHz differential signal. The quadrature 12-GHz LO was generated using a 90° hybrid. An off-chip balun, as well as a 180° coaxial hybrid was used to obtain single-ended IF to drive the 50- Ω load of the spectrum analyzer. Noise figure was measured using the direct method [17]. An external low-noise amplifier (LNA) was used to increase the noise floor to above that of the spectrum analyzer. The results were comparable to that obtained using a noise source.

B. Measurement Results

The measured input return loss is shown in Fig. 20. Fig. 21 shows the measured conversion gain and the DSB noise figure of the downconverter, as the dc V_{GS} is varied, for an RF frequency of 23.1 GHz and an IF frequency of 30 MHz. It shows the sensitivity of the performance of the mixer with changing bias or duty cycle of the LO switching waveform. As expected, the gain and noise performance is best optimized close to the threshold voltage of the individual switches.

The 1-dB compression point was measured to be -12.7 dBm , as shown in Fig. 22. The pre-amplifier stage, as well as the IF buffer, play an important role in the overall linearity of the downconverter. The linearity of the downconverter is not as high as in most current-driven passive mixers. However, most millimeter-wave applications are not constrained by high linearity requirements, due to the severe path losses associated with atmospheric absorption. The measured IIP2 was $+18 \text{ dBm}$ and is limited by the inaccuracies in the differential test setup at these frequencies.

The measured 2LO-RF isolation and dc offset with varying LO frequency is shown in Fig. 23. This was carried out by measuring the 2LO power at the RF port with respect to the LO power driven at the LO port. The 2LO-RF isolation was better than 62 dB from 9- to 13-GHz LO (or from 18- to 26-GHz 2LO). The resulting dc offsets were measured by terminating the RF port and exciting the LO port. They were less than 2.1 mV from 9 to 13 GHz.

Fig. 24. shows the measured IF 3-dB bandwidth for varying LO. The 3-dB bandwidth was 670 MHz making it suitable for gigabit/s applications.

Table I shows a summary of the measured performance of the downconverter.

A comparison of the performance with recently published mixers is given in Table II.

VI. CONCLUSION

This paper has presented a balanced passive SHM in 0.13- μm CMOS for 24-GHz direct-conversion applications. Design and optimization methods for gain and noise performance have been presented. The downconverter has a conversion gain of 3.2 dB and a DSB noise figure of 10 dB. The input-referred 1-dB compression point is -12.7 dBm. The mixer core including the pre-amplifier and the IF buffer consumes 8.5 mA at 1.6 V. The LO circuitry consumes 15 mA at 1.2 V. The dc offsets are less than 2 mV, making it highly suitable for zero-IF applications due to its high 2LO-RF isolation and $1/f$ noise performance. The downconverter can be preceded by an LNA in silicon or III-V technologies to set the overall system noise figure. Being completely balanced, it is very suitable for millimeter-wave frequency-band operation.

ACKNOWLEDGMENT

The authors wish to thank the Center for Wireless Communications, University of California at San Diego (UCSD), La Jolla, and its member companies. The authors would also like to thank Prof. G. Rebeiz and Dr. J.-G. Kim, both with UCSD, for useful discussions. The authors also acknowledge Dr. I. Young, Intel Corporation, Hillsboro, OR, and Dr. X. Wang and W. Ni, both with IBM, San Diego, CA, for foundry support.

REFERENCES

- [1] B. Floyd, S. Reynolds, U. Pfeiffer, T. Zwick, T. Beukema, and B. Gaucher, "SiGe bipolar transceiver circuits operating at 60 GHz," *IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 156–167, Jan. 2004.
- [2] X. Guan, H. Hashemi, and A. Hajimiri, "A fully integrated 24-GHz eight-element phased-array receiver in silicon," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2311–2320, Dec. 2004.
- [3] X. Guan and A. Hajimiri, "A 24-GHz CMOS front-end," *IEEE J. Solid-State Circuits*, vol. 39, no. 2, pp. 368–373, Feb. 2004.
- [4] A. Abidi, "Direct-conversion radio transceivers for digital communications," *IEEE J. Solid-State Circuits*, vol. 30, no. 12, pp. 1399–1410, Dec. 1995.
- [5] L. Sheng, J. Jensen, and L. Larson, "A wide-bandwidth Si/SiGe HBT direct conversion sub-harmonic mixer/downconverter," *IEEE J. Solid-State Circuits*, vol. 35, no. 9, pp. 1329–1337, Sep. 2000.

- [6] K. Tang, S. Leung, N. Tieu, P. Schvan, and S. Voinigescu, "Frequency scaling and topology comparison of millimeter-wave CMOS VCOs," in *IEEE Compound Semiconduct. Int. Circuits Symp. Dig.*, 2006, pp. 55–58.
- [7] R. Kodkani and L. Larson, "A 24-GHz CMOS direct-conversion sub-harmonic downconverter," in *IEEE RFIC Symp. Dig.*, 2007, pp. 485–488.
- [8] H. Jen, S. Rose, and R. Meyer, "A 2.2 GHz sub-harmonic mixer for direct conversion receivers in 0.13 μm CMOS," *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, pp. 1840–1849, 2006.
- [9] S. Zhou and M. Chang, "A CMOS passive mixer with low flicker noise for low-power direct-conversion receiver," *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1084–1093, May 2005.
- [10] A. Shahani, D. Shaeffer, and T. Lee, "A 12-mW wide dynamic range CMOS front-end for a portable GPS receiver," *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 2061–2070, Dec. 1997.
- [11] K.-J. Koh, M.-Y. Park, C.-S. Kim, and H.-H. Yu, "Subharmonically pumped CMOS frequency conversion (up and down) circuits for 2-GHz WCDMA direct-conversion transceiver," *IEEE J. Solid-State Circuits*, vol. 39, no. 6, pp. 871–884, Jun. 2004.
- [12] F. Huang and K.-O. Kenneth, "A 0.5- μm CMOS T/R switch for 900-MHz wireless applications," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 486–492, Mar. 2001.
- [13] E. Bautista, B. Bastani, and J. Heck, "A high IIP2 downconversion mixer using dynamic matching," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1934–1941, Dec. 2000.
- [14] D. Shaeffer and T. Lee, "A 1.5-V, 1.5-GHz CMOS low noise amplifier," *IEEE J. Solid-State Circuits*, vol. 32, no. 5, pp. 745–759, 1997.
- [15] J. Crols and M. Steyaert, "A single-chip 900 MHz CMOS receiver front-end with a high performance low-IF topology," *IEEE J. Solid-State Circuits*, vol. 30, no. 12, pp. 1483–1492, Dec. 1995.
- [16] "IBM CMOS8RF (CMRF8SF) Design Manual," IBM, Essex Junction, VT, 2005, pp. 1–520.
- [17] B. Razavi, "A 60-GHz CMOS receiver front-end," *IEEE J. Solid-State Circuits*, vol. 41, no. 1, pp. 17–22, Jan. 2006.
- [18] M. Hossain, B. Frank, and Y. Antar, "Performance of a low voltage highly linear 24 GHz down conversion mixer in 0.18 μm CMOS," in *IEEE Silicon Monolithic Integr. Circuits RF Syst. Dig.*, 2005, pp. 135–138.
- [19] T.-H. Wu, S.-C. Tseng, C.-C. Meng, and G.-W. Huang, "GaInP/GaAs HBT sub-harmonic Gilbert mixers using stacked-LO and levelled-LO topologies," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 5, pp. 880–889, May 2007.
- [20] T. Yang and H. Chiou, "A 28 GHz sub-harmonic mixer using LO doubler in 0.18 μm CMOS technology," in *IEEE RFIC Symp. Dig.*, 2006, pp. 239–242.
- [21] F. Ellinger, "26–34 GHz CMOS mixer," *Electron Lett.*, vol. 40, no. 22, pp. 1417–1419, Oct. 2004.
- [22] A. Verma, L. Gao, and K. K. O, "A K -band down conversion mixer with 1.4 GHz bandwidth in 0.13 μm CMOS technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 15, no. 8, pp. 493–495, Aug. 2005.



Rahul M. Kodkani (S'05–M'07) received the B.E. degree in electrical and electronics engineering from Bangalore University, Bangalore, India, in 1997, the M.S. degree in electrical engineering from West Virginia University, Morgantown, in 2002, and is currently working toward the Ph.D. degree at the University of California at San Diego (UCSD), La Jolla.

During Summer and Fall 2005, he was a Design Engineering Intern with Sierra Monolithics Inc., Redondo Beach, CA, where he was involved in RF integrated circuit (RFIC) design. During Fall 2006 and Winter 2007, he was an Engineering Intern with Qualcomm Inc., San Diego, CA, where he was involved with a research project in transmitter ICs. His research interests include RF and millimeter-wave integrated circuits in CMOS and SiGe for wireless applications.

Mr. Kodkani was the recipient of the Third Prize Student Paper Award presented at the 2006 IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF). He was also the recipient of the CAL(IT)² Fellowship (2002–2003) presented by the University of California at San Diego.



Lawrence E. Larson (S'82–M'86–SM'90–F'00) received the B.S. and M.Eng. degrees in electrical engineering from Cornell University, Ithaca, NY, in 1979 and 1980, respectively, and the Ph.D. degree in electrical engineering and M.B.A. degree from the University of California at Los Angeles (UCLA), in 1986 and 1996, respectively.

From 1980 to 1996, he was with Hughes Research Laboratories, Malibu, CA, where he directed the development of high-frequency microelectronics in GaAs, InP, and Si–SiGe and microelectromechanical systems (MEMS) technologies. In 1996, he joined the faculty of the University of California at San Diego (UCSD), La Jolla, where he is the Inaugural Holder of the Communications Industry Chair. He is currently Director of the UCSD

Center for Wireless Communications. During the 2000–2001 academic years, he was on leave with IBM Research, San Diego, CA, where he directed the development of RF integrated circuits (RFICs) for third-generation (3G) applications. During the 2004–2005 academic year, he was a Visiting Professor with the Technical University of Delft, Delft, The Netherlands. He has authored or coauthored over 250 papers. He holds 31 U.S. patents.

Dr. Larson was the recipient of the 1995 Hughes Electronics Sector Patent Award for his research on RF MEMS technology. He was corecipient of the 1996 Lawrence A. Hyland Patent Award of Hughes Electronics for his research on low-noise millimeter-wave HEMTs, the 1999 IBM Microelectronics Excellence Award for his research in Si–SiGe heterojunction bipolar transistor technology, and the 2003 IEEE Custom Integrated Circuits Conference Best Invited Paper Award.