Linearity and Efficiency Enhancement Strategies for 4G Wireless Power Amplifier Designs

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Abstract

Next generation wireless transmitters will rely on highly integrated silicon-based solutions to realize the cost and performance goals of the 4G market. This will require increased use of digital compensation techniques and innovative circuit approaches to maximize power and efficiency and minimize linearity degradation. This paper summarizes the circuit and system strategies being developed to meet these aggressive performance goals.

1. Introduction

The linear microwave power amplifier/module industry has historically been dominated by non-standard semiconductor technologies (like GaAs and Si-LDMOS), relatively low levels of integration (hybrid assembly techniques are still common), and little interaction with baseband signal processing. In this regard, the typical power amplifier module today resembles the low-frequency analog/data converter module of forty years ago. This raises the question of whether microwave power amplifiers are poised to undergo a shift to highly integrated, richly digital, implementations — much the way analog and mixed-signal circuits (and indeed RF transceivers in general), transitioned to full CMOS within the last decade.

There are several factors that are pushing power amplifier technology towards higher levels of integration, and co-integration with other portions of the transceiver. The first is the relentless cost pressure of the modern consumer wireless industry, where every penny saved is important in a 1 Billion unit/year market. The second is the significant performance gains that can be realized if *baseband* information is used to improve the performance of the *RF* chain. This baseband information is readily available if the PA is co-located with the baseband digital processor, or if there is a common digital interface between the baseband processor and the RF transceiver.

At the same time, the performance of microwave power amplifiers (in terms of linearity and dc power consumption) is exquisitely sensitive to the characteristics of the device, and decades of III-V HBT/PHEMT and Si-LDMOS device optimization has made the performance and cost of these solutions very impressive. This continuing refinement is one of the reasons these technologies continue to dominate the power amplifier market while silicon-based technologies have taken over all remaining RF transceiver functions. In addition, the relatively low breakdown voltage of scaled silicon devices (SiGe HBTs or CMOS) makes it difficult to achieve the high power output required for many applications. Finally, the move towards wideband OFDM waveforms — with their high peak-to-average ratios — has reduced the power-added efficiency achievable using standard circuit techniques. For example, typical OFDM power amplifiers achieve PAE's of only 20-30%, which for a 27 dBm output power means that as much as 1-2W of waste heat is generated. Raising this efficiency to 40-50% would have an enormous impact on the battery life and capabilities of mobile devices.

This paper will examine these tradeoffs, with particular attention to the circuit and signal processing techniques being developed in highly integrated silicon-based wireless power amplifiers. The key challenges for silicon-based power amplifiers are improving efficiency, increasing output power, and enhancing linearity.

2. Signal Characteristics of Wireless Standards

Power amplifier performance is largely dictated by the baseband waveform characteristics, the center frequency, and the output power. As shown in Table 1, there are several ways to characterize the waveform characteristics. The Peak-to-Average Ratio (PAR) compares the peak modulated output power to its short-term average; as the industry move to more spectrally efficient modulation formats like OFDM this ratio is growing, creating additional linearity and efficiency challenges. Power amplifier efficiencies typically peak at the maximum saturated output power, but decline precipitously as the power is reduced, so a high PAR waveform implies that the power amplifier is spending most of its time in a low-efficiency "backed-off" mode of operation.

The Error Vector Magnitude (EVM) is a modulation quality metric widely used in digital RF communications systems, especially in 3G and OFDM-based modulation standards. It is essentially a measure of the in-band accuracy of the modulation of the *transmitted* waveform, i.e.

$$EVM = \frac{\sqrt{\sum_n |e(k)|^2}}{n} \quad (1)$$

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Table 1. Signal Characteristics of Modern Wireless Standards.

System	PAR(dB)	PMR(dB)	PCDR(dB)	Bandwidth(MHz)	Access Type
GSM	0	0	0	0.2	TDMA
EDGE	3.2	17	30	0.2	TDMA
CDMA ONE	5.5-12	∞	60	1.25	CDMA
UMTS	3.5-7	∞	80	5	CDMA
CDMA 2000	4-9	∞	80	1.25	CDMA
802.11a/g	8-10	∞	25	20	TDMA
WiMax	8-10	∞	25	20	TDMA

where $e(k)$ is the normalized magnitude of the error vector at symbol time k, and n is the number of samples over which the measurement is made.

The EVM is essentially an in-band measure of the waveform quality, while spectral regrowth is an out-of-band measure of waveform quality. This is typically measured by the adjacent channel power regrowth (ACPR) and the alternate channel power regrowth (AltCPR). The ACPR is typically measured as the ratio of the signal power in the desired channel to the distortion power in an adjacent channel; the alternate channel power regrowth is a measure of the ratio of the signal power in the desired channel to the distortion power in the alternate channel. These two measures are shown in Figure 1.

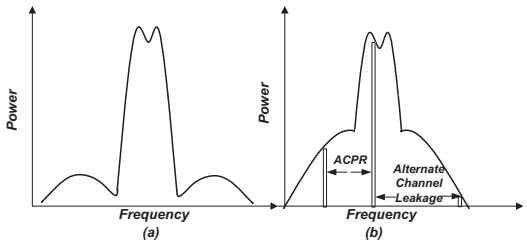

Figure 1. Spectrum of transmitted signal: (a) Spectrum of ideal transmitted modulated signal. (b) Spectrum of distorted signal illustrating ACPR and alternate channel regrowth.

The performance of the power amplifier can be dramatically improved if the peaks of the waveform can be reduced, lowering the PAR, while keeping the average power and bandwidth the same, and this is the basis for a variety of *crest-factor reduction* (CFR) algorithms [1–3]. These algorithms rely on tone reservation and carrier phasing techniques, or on selective clipping of the waveform. The clipping algorithms lower the peak by adding an "inverse" of the peak to the original waveform at the appropriate time. Viewed from the perspective of a typical OFDM waveform, these peaks occur at a time when all the individual carriers add coherently, so removing the peak adversely affects all of the carriers at the same time, with detrimental effects on the error vector magnitude (EVM) performance and resulting spectrum regrowth. In addition, the spectrum of this added inverse peak is often very broad, creating significant spectral regrowth outside the band of the original signal. A variety of clever algorithms have been developed to minimize these limitations.

Sperlich [4] uses an interpolation technique to reduce CFR by selectively adding uncorrelated in-band noise to the signal. This improves spectral regrowth at the expense of EVM performance. Vaananen [5] adopts a peak windowing method to minimize adjacent channel power regrowth. Baxley [6] adopts a technique where in-band and out-of-band components are separately optimized, and in-band processing minimizes EVM and out-of-band processing minimizes regrowth.

A sophisticated signal processing engine is required to accomplish these improvements, and an example of a CFR engine is given by Wegener [7]. The circuit was fabricated using a 130 nm CMOS process, and required 1.8M gates at a power dissipation of 2.8 W when operating in two-channel transmit diversity mode. In this case, successive clipping of multiple peaks and filter stages were required to minimize the overall spectral regrowth and minimize EVM for CDMA, WCDMA, and OFDM signals. Typical reductions in PAR of 2-3 dB are achievable; this level of improvement seems modest, but can result in a 50% reduction in power amplifier dc power consumption in some cases. Clearly, as VLSI technology improves and the algorithms become more sophisticated, the overhead associated with the CFR reduction will drop dramatically.

A second method to characterize the waveform is by the Peak-to-Minimum Ratio (PMR), which is the ratio of the peak waveform power to the minimum waveform power, again measured over a short period of time. A high PMR waveform presents a challenge to the power amplifier from an efficiency perspective, and it can also make certain linearization techniques difficult to implement. In these cases, the output power reaches near zero for a brief period of time.

The Power Control Dynamic Range (PCDR) is a measure of the maximum variation in the average output power, measured over a long period of time (measured in days or even weeks). This variation is especially large in CDMA-based systems, because of the power control loop required to prevent near-far interference in spread-spectrum systems. A high PCDR presents problems for maximizing power amplifier efficiency, since the long term average output power is typically well below that where the peak efficiency occurs. In most CDMA mobile systems, the average output power is log-normally distributed, with a mean of roughly

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0 dBm and a peak of approximately 30 dBm. So, the PCDR is typically over 60 dB in most CDMA-based systems. OFDM-based systems like WiMax can have similar PCDR constraints.

3. Power Efficiency Enhancement Strategies

Silicon technology has an intrinsic disadvantage compared to III-V technology with respect to achievable efficiency (due to the lower f_T and breakdown voltage) so design-oriented approaches are required to realize the necessary dc power consumption goals. The use of varying classes of operation (like Class-AB, B, D, E, etc.) to achieve these improvements is of limited comparative value, since III-V devices can use them just as easily as Si-based devices. So, more sophisticated techniques are required for dc power reduction in silicon-based power amplifiers, and the two most popular are *DC Bias Variation* and *Load-Line Variation*. These techniques are illustrated in Fig. 2.

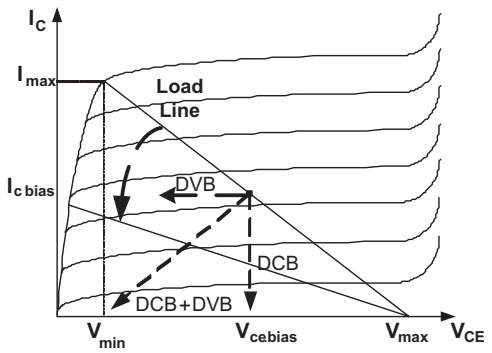

Figure 2. Illustration of efficiency enhancement techniques. Dynamic current biasing (DCB) alters the dc bias current in response to changes in the RF output power. Dynamic voltage biasing (DVB) alters the bias voltage in response to the RF power changes. The load-line presented to the transistor can also be changed in response to changes in power.

DC Bias variation techniques have been thoroughly investigated, and fall into several categories. Dynamic Current Bias (DCB) variation approaches have found their way into several commercial power amplifier products [8]. In their simplest embodiment, the dc bias current is reduced in response to reductions in the RF output power, as shown in Fig. 2. This simple approach can achieve reductions in dc power consumption, although a typical microwave power amplifier will exhibit significant gain reduction when its bias current is reduced, and this effect requires compensation. A better approach may be to switch parallel devices in and out with MOSFET switches to alter the dc bias current, which will maintain a constant power gain even as the dc current consumption drops [9]. In the simplest case, the power amplifier can be switched from a "low-power" version to a "high-power version."

DC bias variation can also be applied to the drain/collector voltage of the transistors, with even greater effect, and these Dynamic Voltage Biasing (DVB) techniques are known as Envelope Tracking (ET) or Envelope Elimination and Restoration (EER). These techniques have a long pedigree — in fact, EER was developed initially in the 1930's as an efficiency enhancement technique for kilowatt AM transmitters [10]!

Dynamic power supply schemes are usually separated into two types: Envelope Elimination and Restoration (EER) and Envelope Tracking(ET). Figure 3 shows the principles of traditional EER and ET systems. EER uses a combination of a high efficiency switched-mode PA with an envelope re-modulation circuit [11–15]; ET utilizes a linear PA and a controlled supply voltage, which closely tracks the output envelope. When the supply voltage tracks the instantaneous output envelope, it is known as Wide Bandwidth ET (WBET) [16–19]; when the supply voltage tracks the long-term average of the output envelope, it is known as Average ET (AET) [20, 21]. AET techniques are especially useful for power control schemes, such as the reverse link in CDMA, where the long-term variation in average power is much greater than 20dB [22]. However, they improve the efficiency only modestly for high PAR signals such as OFDM.

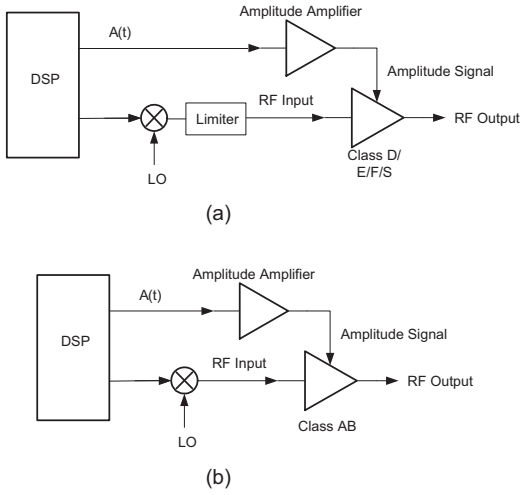

Figure 3. Block diagram of (a) Envelope Elimination and Restoration (EER) power amplifier and (b) Envelope Tracking (ET) amplifier

In both EER and wideband ET systems, the collector/drain supply of the RF power transistor dynamically changes with the output envelope, so the RF transistor operates with higher efficiency over a wide dynamic range of output power. Theoretically, EER is more efficient than ET, since the RF transistor is always operating in a switching mode. In the traditional EER system, the input RF signal is

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applied to a limiter (as shown in Figure 3); this is a problem for some wide dynamic range OFDM signals, where the peak-to-minimum ratio is essentially infinite [23]. By contrast, ET systems are better positioned to accommodate high peak-to-minimum signals because the amplifiers operate in a linear (if slightly compressed) mode at all output power levels, so the resulting gain variation is manageable.

Due to the nonlinear operations of the transformation of the I and Q signals to amplitude and phase, the bandwidths of the amplitude signal $A(t)$ and the phase signal are much wider than that of baseband signal. This imposes practical challenges to the traditional EER transmitter, and typically limits it to narrow-bandwidth applications [24, 25]. By contrast, the ET system requires a lower envelope amplifier bandwidth and less precise time-alignment between the envelope and RF paths [26]. Therefore, it is more easily applied to applications requiring a wide signal bandwidth such as OFDM.

The use of wideband ET techniques can boost the RF PA drain/collector average efficiency, but the total system efficiency is determined by the product of the envelope amplifier efficiency and the RF transistor drain/collector efficiency [27–29]. Thus, a high-efficiency envelope amplifier design is critical to the EER/ET system. This design is itself quite challenging, since the amplifier needs to provide a signal to a load (the power amplifier collector or drain) of several ohms or less, at a frequency of well over 20 MHz. Fortunately, efficient switching-mode dc-dc converters have been demonstrated with bandwidths sufficient for wideband OFDM modulation. In many cases, these converters can be integrated along with the power amplifier to realize a completely monolithic solution (except for the external inductor). A recent example of a monolithic SiGe BiCMOS envelope-tracking power amplifier (PA) for 802.11g OFDM applications was demonstrated at 2.4 GHz. The die included a high-efficiency high-precision envelope amplifier and a two-stage SiGe HBT PA. The two-stage amplifier exhibited a 12-dB gain, $< 5\%$ EVM, 20-dBm OFDM output power, and an overall efficiency (including the envelope amplifier) of 28% [30].

The output of the envelope amplifier has to be time-aligned to the output of the RF amplifier, so that extra distortion is not created by the resulting time mismatch between the two paths. Fortunately, the wideband ET system is less sensitive to this misalignment effect than the traditional EER amplifier, and so the effect of small misalignment on EVM is negligible.

Load-line variation techniques have been developed as an approach for reducing PA dc power consumption when the RF output power is reduced. A higher impedance is presented to the device as the power is reduced, maintaining a constant voltage swing a the drain/collector. There are several ways of accomplishing this variation.

The Doherty amplifier [31, 32] utilizes two amplifiers in parallel — the auxiliary amplifier performs a "load pull" on the main device so that the voltage swing across the main device stays roughly constant over the highest levels of the output power, even though the RF current in the main device is increasing, as shown in Fig. 4. When the RF output power is reduced, the auxiliary amplifier turns off, reducing the overall dc current consumption considerably in the "backed-off" mode of operation. Multiple stages of the Doherty can be employed to realize even greater power saving benefits as the RF output power is reduced [33, 34]. Although the Doherty amplifier topology was invented decades ago, it has enjoyed renewed interest recently for base station applications [35–37] and handset applications [38–40].

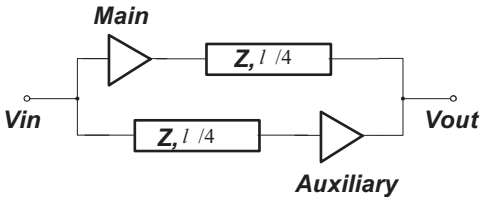

Figure 4. The Doherty amplifier uses a main amplifier and an auxiliary amplifier in parallel. The auxiliary amplifier only provides power for the highest output power conditions, and "load-pulls" the main power amplifier so that its voltage swing remains constant as the output power varies.

The load impedance presented to the transistor can be varied directly to adaptively modify the impedance presented to the transistor in response to the required output voltage. The impedance can be varied with pin-diodes, MEMs devices [41] or by varactor diode tuning of a transmission line impedance transformer, as shown in Fig. 5 [42]. A wide range of impedances can be achieved with this technique and the high efficiency of the power amplifier can be maintained over a broad range of output powers. One example of an adaptively tuned amplifier provided 13dB gain, 27-28 dBm output power at the 900, 1800, 1900 and 2100MHz bands [43]. For the communication bands above 1GHz optimum load adaptation resulted in efficiencies between 30-55% over a 10dB output power control range, a dramatic improvement compared to constant load impedance performance. Dynamic load line modulation techniques can also be employed to provide amplitude modulation of the output waveform, promising an alternative approach for non-constant amplitude modulation.

4. Power Enhancement Strategies

Scaled SiGe HBT and CMOS devices possess a relatively low breakdown voltage, which means that their dc operating voltage must also be low, and therefore their RF output is limited. This limitation is traditionally overcome in microwave circuit design by lossless power-combining techniques like the Wilkinson power combiner shown in Fig. 6(a). Unfortunately, these distributed approaches require a large die area, though this can be reduced through

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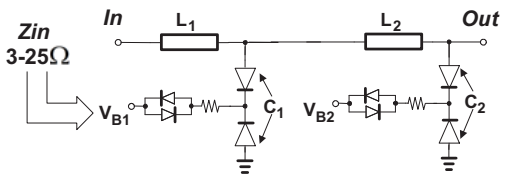

Figure 5. A variable impedance transmission line tuner can present a variety of impedance levels to the power amplifier, so that the voltage swing across the collector remains high even at low output power levels, maximizing efficiency [43].

the use of lumped equivalents of quarter-wave transmission lines.

Transformer-based power combining approaches are more popular for silicon power amplifiers, because of their compact implementation and low-loss. Series/parallel transformer approaches have been described [44–46] where the output is the sum of the output voltages from N parallel power amplifiers as shown in Fig. 6(b). These approaches also take advantage of the inherent symmetry of balanced operation to minimize the return currents flowing through the ground connections, a distinct advantage for monolithic high-power implementations. An example of the feasibility of this concept is a 2.4-GHz 2-W 2-V (450 mW at 1V) CMOS power amplifier with 50-Ω input and output match and power added efficiency (PAE) of 41% [47].

The voltage across the transistor can also be reduced by series operation of multiple devices. This approach was proposed by Sowlati [48] to realize a $0.18\mu m$ CMOS power amplifier that provided 23-dBm output power with a power-added efficiency (PAE) of 42% at 2.4 GHz. The amplifier operated reliably with a 2.4V supply even with short gate length devices. This approach is shown schematically in Fig. 6(c), and the RC-network connecting the upper gate device to the output is designed to equally distribute the total output voltage swing between the two devices.

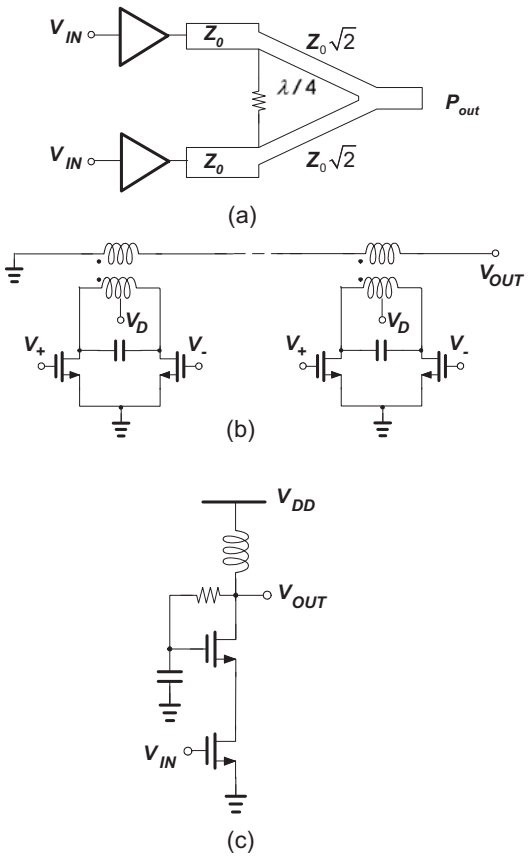

Figure 6. Lossless combiners for power amplifier applications (a) Wilkinson power combiner (b) Transformer combiners add the voltage output of several parallel amplifiers (c) Series connection of low-voltage FETs allows a high voltage to appear across the complete circuit.

5. Linearization Strategies

After efficiency and output power have been optimized, the final step is to improve the linearity of the amplifier. Traditional feedback techniques are of limited utility, because there is little excess gain at microwave frequencies to provide the necessary correction. However, if the high-frequency signal can be translated back down to complex baseband, then the higher available gain at baseband can be used to provide adequate feedback. This is the basis for *Cartesian Feedback*, which has been used for many years in relatively narrow bandwidth communication systems [49], and is shown in Fig. 7(a). The inherent matching of the I and Q channels in the Cartesian feedback approach is a distinct advantage compared to amplitude/phase feedback approaches.

However, the delay around the feedback loop, due to the high-Q output matching network, limits the achievable bandwidth of the system. Recent advances in phase compensation approaches, combined with fully integrated implementations of power amplifiers, have extended the bandwidth of Cartesian feedback techniques into the low-MHz range [50, 51]. However, the achievable bandwidth of any feedback system will always be limited, and broadband modulation approaches will require open-loop approaches. An open-loop analog pre-distortion approach using a polynomial pre-distorter was recently implemented to realize an improved bandwidth [52].

The most promising open-loop approach is to perform pre-distortion using digital techniques at baseband frequencies. This technique is illustrated in Fig. 7(c) and is known as *adaptive digital pre-distortion* [53]. In this case, the AM-AM and AM-PM distortion through the amplifier is determined and a digital signal processor provides the appropriate pre-distorted in-phase and quadrature-phase signals for the baseband upconverter. Several different versions of

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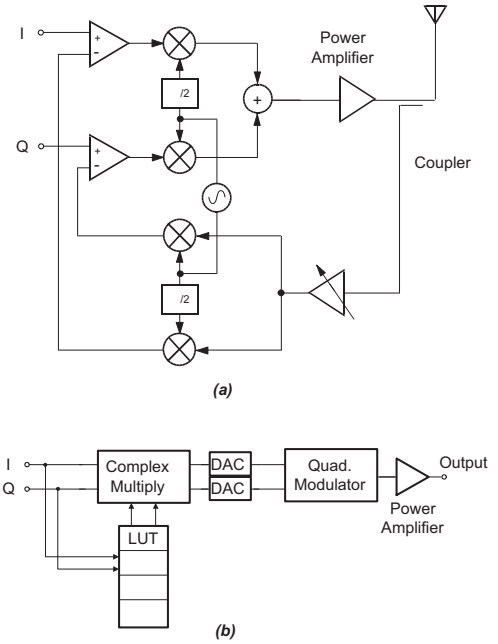

Figure 7. Linearization approaches for power amplifiers (a) Cartesian feedback provides complex baseband compensation of Power amplifier nonlinearities (b) Adaptive digital predistortion compensates the nonlinearities in the digital domain prior to baseband conversion.

adaptive predistortion have been developed [54, 55]. With the increasing sophistication of DSP techniques, as well as lower power high-speed DACs, adaptive digital predistortion has recently become possible for mobile terminals as well [56].

There are several limitations to adaptive digital predistortion: significant bandwidth expansion, a relatively high digital processing overhead, and a susceptibility to memory effects (long time constant variations in the PA gain and phase responses that are difficult to incorporate into the predistorter transfer function). In addition, the predistortion coefficients require constant updating, due to aging, temperature and power supply variation effects over long periods of time. Adaptive digital predistortion works best for standards requiring a high PAR (from Table I) and moderate-low PCDR, such as base stations, wireless LAN cards, and EDGE. It also works best in conjunction with efficiency enhancements schemes such as the Doherty amplifier or Envelope Tracking/EER, since it does little to enhance the overall efficiency of the basic amplifier, but it can have an enormous effect on linearity.

Another limitation of digital predistortion is the bandwidth expansion, which puts greater burden on the sampling rate of the DAC, as well as the bandwidth of the subsequent RF stages. The magnitude of the bandwidth expansion depends on the desired linearity improvement; if IM3 is the main source of the undesirable distortion, then a bandwidth expansion by a factor of three is required.

6. Conclusions

Upcoming 4G wireless systems will require innovations in all areas of power amplifier design and development. The migration of power amplifiers from III-V to silicon-based technologies and the use of digital techniques to correct the imperfections and limitations of RF power amplifiers represent the next stage of development for high-frequency wireless devices, especially since transistor technology is nearly "maxed-out" in performance. These new approaches will lead to dramatic improvements in the efficiency and bandwidth capabilities of multi-mode wireless transmitters.

7. Acknowledgments

The authors wish to thank Professors Ian Galton and Gabriel Rebeiz of UCSD and Professor Leo DeVreede of TU Delft for valuable discussions. We also acknowledge the generous support of Ericsson, Nokia, Conexant, Motorola, Freescale, Cree, Nitronex, ST Microelectronics, the UCSD Center for Wireless Communications and the California Institute for Telecommunications and Information Technology for their support.

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