A Low-Power 5GHz Transceiver in 0.13 μm CMOS for OFDM Applications with Sub-mm^2 Area

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Abstract – **A 5GHz direct conversion transceiver is fabricated in a 0.13µm CMOS process for WLAN 802.11a applications. The transmitter achieves -56 dBc LO leakage, -36 dBc sideband rejection, -43 dBc 3rd harmonic suppression at 5.4GHz, and an EVM of 3.4% at 5.1GHz with 60mW power consumption. The receiver achieves 3.3 dB NF, 27 dB conversion gain, -12 dBm IIP3, and a measured 1/f noise corner of 110 kHz with 36mW power consumption from a 1.2V supply voltage. The active area was 0.9 mm^2.**

Index Terms — **CMOS, Transformer, Low Voltage, Low-Power, Transmitter, EVM, Receiver, Direct conversion**

I. Introduction

In today's WLAN chipset environment, highly integrated, low-cost and low-power solutions are needed. Although CMOS transceivers for 802.11 a/b/g systems have been extensively developed[1-2], demand for even lower power and fewer off-chip components has increased for portable applications. The upcoming 802.11n MIMO standard [3] will require integration of multiple transmitter/receiver chains on the same die, which further increases the demand for area efficient, highly integrated low-power designs. To meet those requirements, a highly integrated 5GHz direct-conversion transceiver is presented that meets the OFDM WLAN requirements and covers the 4.9~5.5GHz band. The design techniques described result in a higher level of integration, as well as outstanding performance at a lower power consumption, than existing techniques.

II. Circuit Design

Fig. 1 shows the block diagram of the transceiver. The transmitter employs a direct conversion architecture, which consists of up-conversion mixers, quadrature LO generation, a PA drive amplifier and an on-chip transformer. Input analog I/Q baseband signals are mixed with quadrature LO signals and up-converted to a single-sideband RF signal. The RF signal is further amplified by a driver amplifier to drive a single-ended off-chip PA. The receiver uses a direct conversion architecture, consisting of a single-ended LNA with an on-chip transformer to drive the following second LNA, passive mixers, and I/Q transimpedance amplifiers form a single-pole filter to provide analog I/Q outputs.

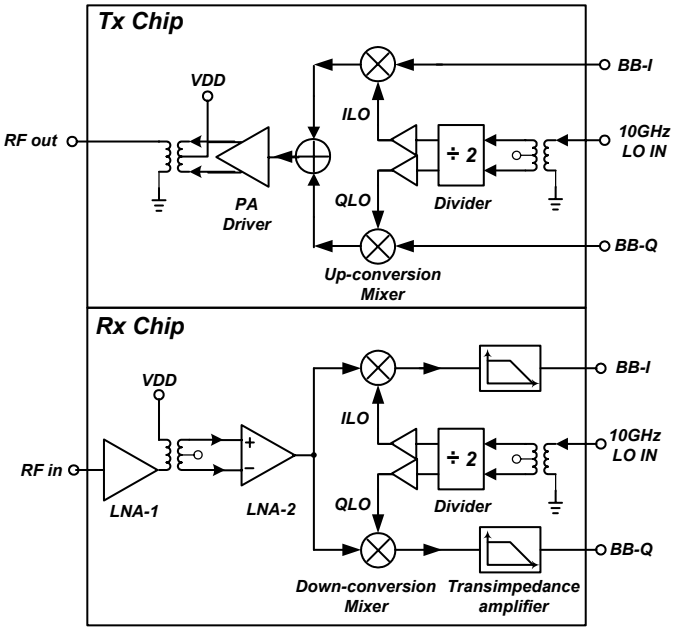


Fig. 1. Transceiver block diagram.

A. Transmitter Design

Upconversion Mixer Design: For the baseband input of direct conversion transmitters, a rail-to-rail voltage swing is desired to achieve maximum SNR and dynamic range, especially with the 1.2V supply voltage. In order to achieve high linearity at a low supply voltage, a virtual ground is created at the baseband input nodes by regulating the cascode device *M3* and *M4* as shown in Fig. 2, and resistors *R1* and *R2* convert the input voltage to current with higher linearity [4]. Component mismatch between input devices, which will create a DC offset and I/Q mismatch leading to LO leakage and a sideband signal at the transmitter output, is minimized through the use of interdigitated layouts.

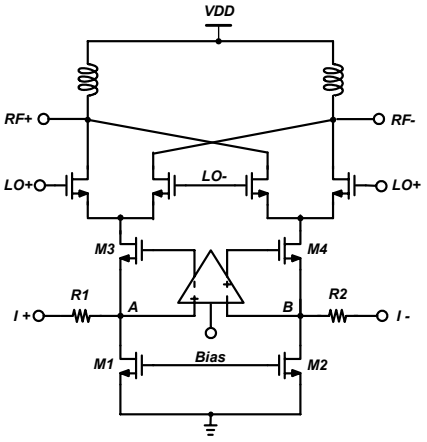
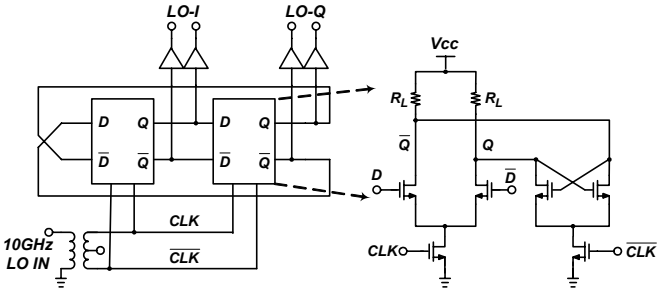
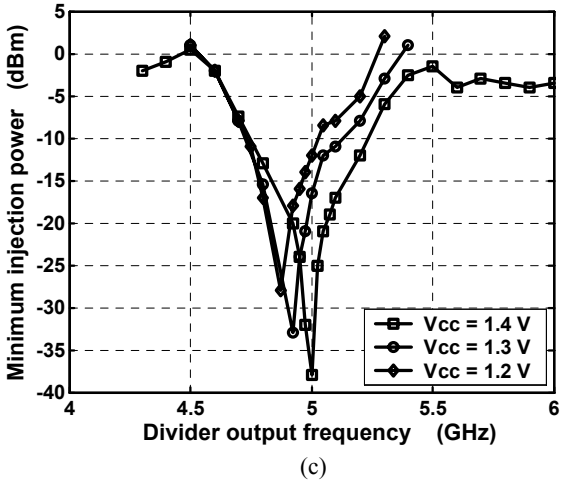


Fig. 2. Up-conversion mixer.

Inductorless Quadrature LO Generation- Quadrature LO signals are required to drive the I/Q mixer pairs. In this design, 5GHz quadrature LO signals are generated by an on-chip divider, which divides an external 9.8-11GHz signal by two, and then buffers the signal to drive the mixer cores. To reduce the die area, no inductors are used. As shown in Fig. 3(a) and (b), the divider is composed of two differential analog D flip-flops configured as a two-stage ring oscillator.



(a) (b)

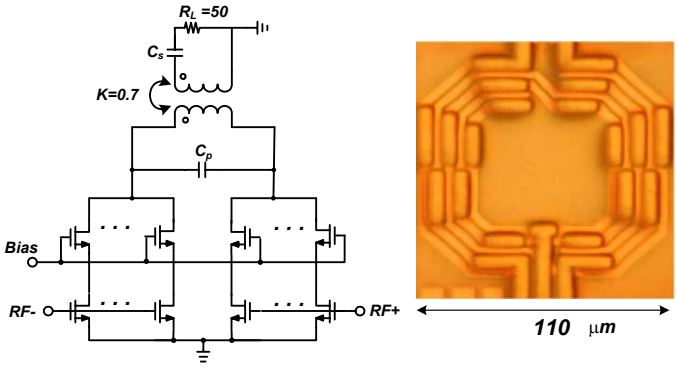


(c)

Fig. 3. Inductorless 10GHz divider (a) Block diagram (b) Schematic of one stage (c) Measured divider sensitivity.

During normal operation, the divider is injection-locked by an external 10GHz signal. Due to the limited locking range, the divider self-oscillation frequency is set to the middle of the operating frequency range and the measured self-oscillation frequency is 5GHz. The measured minimum required injection signal power versus the divider operating frequency is shown in Fig 3(c), which demonstrates that the divider covers the frequency band (4.9-5.5GHz) successfully.

PA Driver with On-Chip Transformer - The single sideband RF signal from the mixers is further amplified to drive an off-chip PA. The pseudo-differential drive amplifier is shown in Fig. 4(a). The cascode devices improve isolation and stability of the amplifier. An on-chip balun matches the output to 50 Ohms. The 1.5:1 balun has both primary and secondary coils located at second thick metal layer as shown in Fig. 4(b), and has an area of only 110μmx110μm.



(a) (b)

Fig. 4. (a) Driver amplifier schematic (b) On-chip transformer.

B. Receiver Design

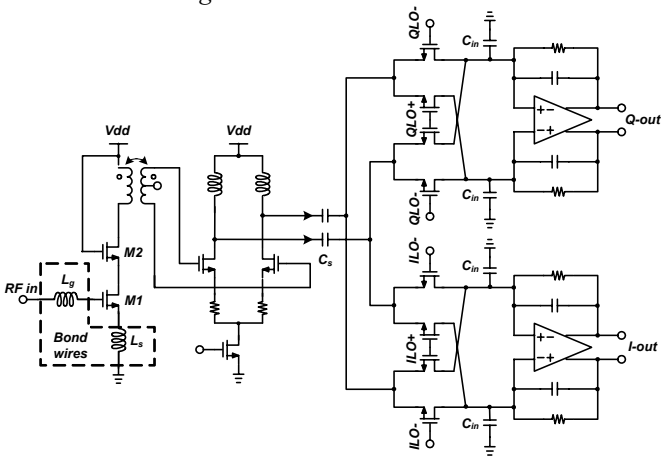


Fig. 5. Receiver architecture.

LNA design – A simplified schematic of the receiver is shown in Fig. 5. The gate and source inductors of LNA1 were implemented with bond wires to provide a 50 ohm match, the two stage LNA had a simulated NF of 2.6 dB including transformer loss. In order to have a high RF impedance at the mixer input, a symmetric inductor was used at LNA2 output to resonate all the parasitic capacitors. The LNA2 also functions as a buffer to reduce the LO-RF leakage.

Passive mixer design - A passive mixer is employed due to the headroom and 1/f noise limitations of the doubly-balanced active mixer [5]. A passive mixer operating with a relatively low load impedance is used to maximize the dynamic range. As a result, the voltage swing at the source/drain of the mixer core is reduced, which provides improved linearity [6].

Fig. 6 shows the simplified passive mixer with an equivalent *RLC* tank at the input and impedance Z_{OUTL} at the output provided by a transimpedance amplifier. The low baseband impedance at the mixer output is transferred to low RF impedance Z_{INL} at the mixer input. The high RF impedance Z_{INS} is transferred to an equivalent high baseband source impedance Z_{OUTS} at the mixer output in the same manner.

Since there is no dc current flowing in the mixer, it contributes very low 1/f noise with zero power consumption [6]. High mixer linearity enables higher gain for LNA1 and LNA2, which reduces the noise contributions from the following stages. Furthermore, a high baseband source impedance Z_{OUTS} reduces voltage noise from the mixer and operational amplifier at the baseband output. All these factors contribute to a receiver with excellent noise and linearity performance.

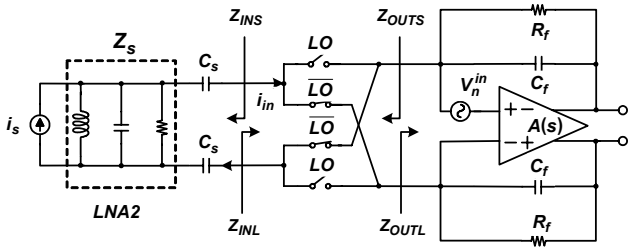


Fig. 6. Simplified passive mixer architecture.

III. Measurement Results

The circuit is fabricated in an IBM 0.13 μm RF CMOS process, with eight metal layers [7]. At -8dBm average output power and 5.1GHz output frequency, the measured transmitter EVM of a 64QAM OFDM modulated signal is 3.4% (-29dB). The corresponding spectrum is shown in Fig. 7, and it falls within the spectral mask defined by IEEE 802.11a standard. Fig. 8 shows the major transmitter parameters: EVM, sideband rejection, LO leakage and 3rd harmonic suppression versus operation frequency. The transmitter performance degrades slowly when it operates at higher frequency, due to the increased I/Q mismatch.

Fig. 9 shows the receiver DSB Noise Figure(NF) and Conversion Gain(CG) over operation frequency from 5.0-5.4GHz. The receiver achieves 27 dB CG. The minimum NF is 3.3 dB and 1/f noise corner is less than 110kHz. Linearity measurement was performed with two 500kHz space tones center at frequency of 5.204GHz, the measured receiver input IP3 is -12 dBm. The measured I/Q amplitude and phase mismatches are 0.3dB and 0.6^o, respectively. The transmitter and receiver chip microphotographs are shown in Fig. 10 and Fig. 11 with active area of 0.3 mm^2 and 0.6 mm^2 respectively. Table I and II summarize the measured transceiver performance.

IV. Conclusion

A 5GHz 0.13 μm CMOS direct conversion transceiver operating with a 1.2V power supply is presented. The transmitter and receiver consume 60mW and 36mW respectively with total active area of only 0.9 mm^2. This is one of the smallest transceiver chips ever reported. These results demonstrate that a high performance, low power, sub-mm^2 transceiver is achievable in a deep sub-micrometer CMOS process.

Acknowledgement

The authors would like to thank Dr. Brent Myers and Dr. Xi Li for useful discussion, Dr. Xu Dong Wang of IBM Microelectronics for supporting the chip fabrication and Sonnet for providing the EM software This work was sponsored by Conexant and the California Institute for Telecommunications and Information Technology through a UC Discovery Grant.

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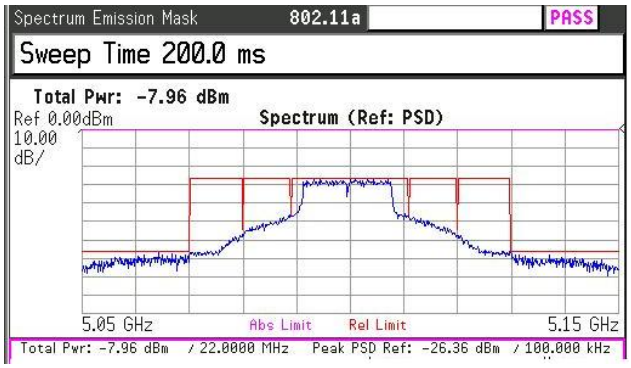

Fig. 7. Measured modulation spectrum versus emission mask.

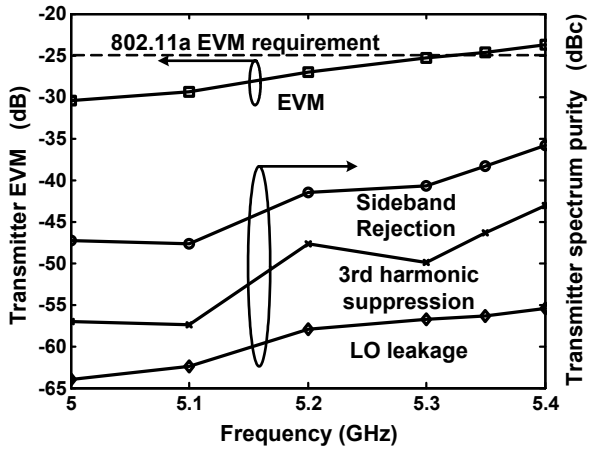

Fig. 8. Measured transmitter performance versus frequency.

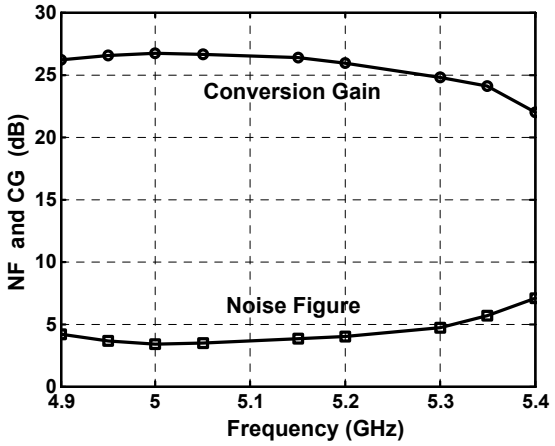

Fig. 9. Measured receiver NF & Gain versus frequency.

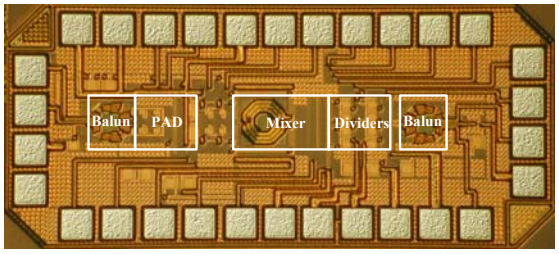

Fig. 10. Transmitter microphotograph.

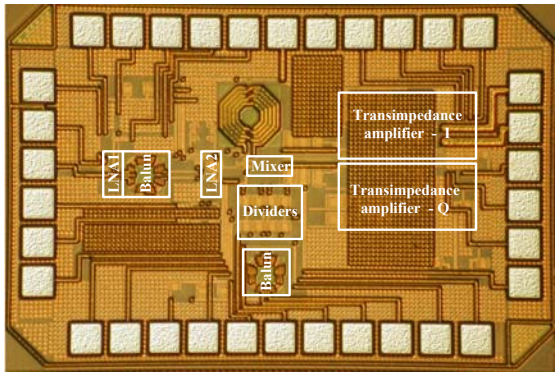

Fig. 11. Receiver microphotograph.

TABLE I. Transmitter Performance Summary

	Measured	Units
Operation Frequency	4.9 – 5.5	GHz
EVM @ P_{out} = -8 dBm	-29	dB
Sideband Rejection	-36	dBc
LO Leakage	-56	dBc
3rd Harmonic Suppression	-43	dBc
OP1dB	3	dBm
OIP3	13	dBm
S22	< - 6	dB
Supply Voltage	1.2	V
Current Consumption	50	mA
Technology	0.13 µm CMOS	
Active Area	0.3	mm^2

TABLE II. Receiver Performance Summary

	Measured	Units
Operation Frequency	4.9 – 5.5	GHz
Minimum DSB NF	3.3	dB
1/f Noise Corner	< 110	kHz
Maximum Conversion Gain	27	dB
Input P1dB	-22	dBm
IIP3	-12	dBm
IIP2	+28	dBm
Average I/Q Amplitude Mismatch	0.3	dB
Average I/Q Phase Mismatch	0.6	degree
LO-RF Leakage	-72	dBm
DC Offset	0.2	mV
Supply Voltage	1.2	V
Current Consumption	30	mA
Technology	0.13 µm CMOS	
Active Area	0.6	mm^2