A 24-GHz CMOS Direct-Conversion Sub-Harmonic Downconverter

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***Abstract* — A 24 GHz sub-harmonic mixer based downconverter is presented. Fabricated in a 0.13 um CMOS process the downconverter includes a pre-amplifier and an IF buffer and consumes 13.6 mW with a 1.6 V supply. The quadrature LO buffer consumes 15 mA at 1.2 V. The circuit includes a single-ended to differential phase splitter for the LO. The downconverter has a conversion gain of 3.2 dB and DSB Noise Figure of 10 dB. The measured input referred 1 dB compression point is -12.7 dBm.**

***Index Terms* — Passive mixer, Sub-harmonic, CMOS, Wireless, Millimeterwave.**

I. Introduction

Gigabit-per-second wireless data is now possible in high-frequency millimeter and near-millimeter wave bands, and the use of silicon technology provides an opportunity for deployment of these systems at low cost [1,4]. Unlicensed bands around 24 GHz and 60 GHz provide high bandwidth enabling high speed wireless networks. Current CMOS and SiGe technologies offer high f_T and f_{MAX} and can be used for applications in the millimeterwave bands such as automotive radars and high data rate wireless communications. The goal of this research is to realize a high performance, low dc power, low area, 24 GHz direct-conversion mixer for phased-array applications.

In direct conversion receivers, the 1/f noise of the mixers is extremely critical since it falls within the bandwidth. Other design issues in direct conversion receivers include DC offsets and LO-RF feedthrough [3]. To overcome these issues, a passive sub-harmonic mixer is chosen. The LO is a sub-harmonic of the RF frequency alleviating the DC offset due the LO-RF feedthrough.

An integrated downconverter for use in zero-IF receivers using this passive sub-harmonic mixer is shown in Fig.1. It includes a pre-amplifier, a passive sub-harmonic mixer, an IF buffer and LO buffers. The design and measurement results of this downconverter implemented in a 0.13 um CMOS technology is discussed in this paper.

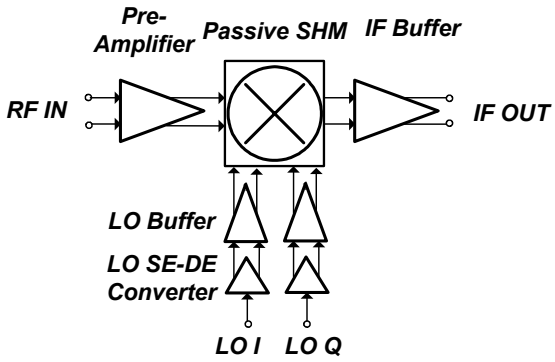

Fig.1. Architecture of down-converter with a sub-harmonic mixer.

II. Circuit Design

A. Passive Sub-Harmonic Mixer

The core of the downconverter is the passive sub-harmonic mixer. The 24 GHz RF is mixed with an LO at half the RF frequency i.e. 12 GHz to downconvert to baseband.

Fig. 2. shows the schematic of the sub-harmonic mixer. By successive mixing with quadrature LO signals, one can obtain sub-harmonic mixing [5,6]. This topology is balanced for RF, LO, 2LO and IF signals. Transistors M_1 – M_8 form a regular double-balanced passive mixer. M_{1Q} – M_{8Q} form the second stage of the passive sub-harmonic mixer.

The gates of these transistors are driven by 12 GHz quadrature signals. The transistors should switch at 50 % duty cycle for best noise and conversion loss performance. This is achieved by a biasing the gate at a voltage which is above the source (or drain) by the threshold voltage of the transistor. Fig. 3 shows the simulated conversion loss as a function of the dc gate-source voltage.

The size of the transistors determines the noise and conversion gain performance of the mixer. Large transistors have smaller on resistance and hence have better noise performance. On the other hand, as the transistor size increases, the capacitance at the second

stage increases reducing the current through the second stage of the mixer which degrades the noise figure. This behavior is seen in simulations and is shown in Fig. 4. An optimum size of 30 μm x 0.13 μm was chosen.

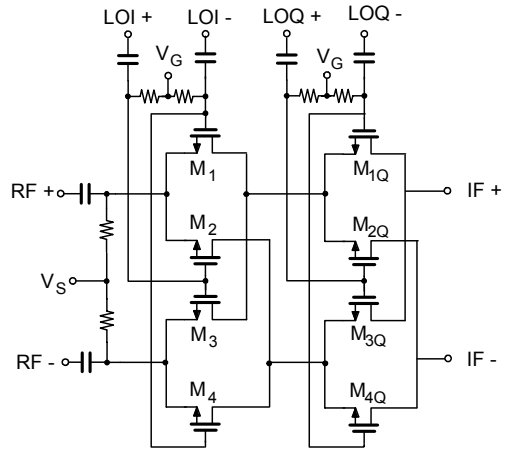

Fig.2. Schematic of the passive sub-harmonic mixer.

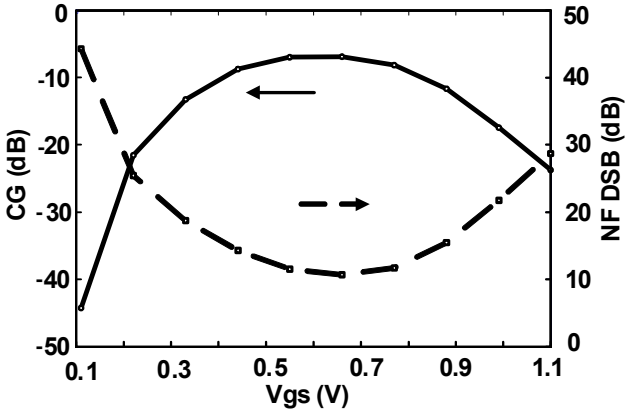

Fig.3. Simulated Conversion Gain and Noise Figure as a function of gate-source bias voltage.

Another important design parameter for the sub-harmonic mixer is the LO swing. A 1.8 V peak-peak differential swing was chosen to obtain hard switching and to reduce the on resistance of the switches with the LO amplitude.

The conversion loss from RF to IF current of this topology based on a square wave mixing is π/2 or 3.9 dB. Since the circuit is balanced for 2LO, ideally, this topology has no 2L0-RF feedthrough.

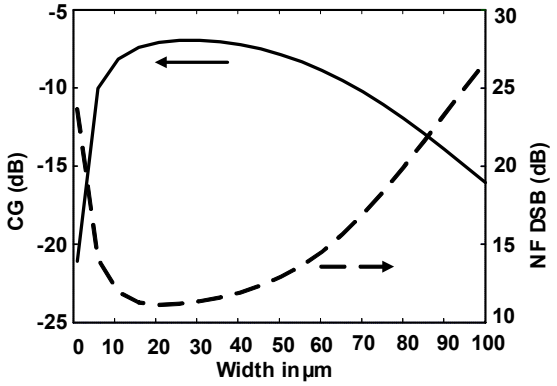

Fig.4. Simulated Conversion Gain and Noise Figure as a function of device size.

The mixer is not very sensitive to the phase accuracy of the quadrature LO. Simulations showed a change in the Noise Figure by less than 1 dB and less than 0.8 dB in the conversion loss for a +/- 10° phase error.

B. Pre-amplifier Design

The pre-amplifier is a standard cascode amplifier designed for low-noise. The NMOS transistors are sized 40 um x 0.13 um with 10 fingers to reduce the gate resistance contribution. The common-gate stage in the cascode provides input-output isolation and hence helps in stability. Differential source inductor and gate inductor are used at the drain and the source to provide input matching to a 100 ohms differential source. The pre-amplifier draws 5 mA at 1.6V. The simulated gain of the pre-amplifier is 9.4 dB and it has a Noise Figure of 3.8 dB.

C. LO and IF Buffers

The LO circuit includes a 12 GHz single-ended to differential phase splitter and a LO buffer.

A simple resistor loaded common-source stage with resistive degeneration provides 0° and 180° phase-splitting if the outputs are taken at the source and drain respectively. Adding another transistor M2 can help in balancing the phase and amplitude inaccuracies due to the imbalance in the capacitances at the drain and source at high frequencies [7]. The schematic is shown in Fig. 5. Simulations showed a 0.3 dB amplitude mismatch and a 3 degree phase error in the differential signals obtained. The phase-splitter consumes 2.5 mA with a 1.2V supply.

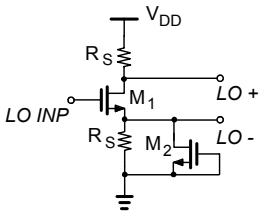

Fig.5. Schematic of active single ended-to-differential converter.

Following the active balun, an inductor loaded differential pair is used as the LO buffer. The differential inductor resonates with the capacitance of the switching mixer transistors. A differential 1.8V swing is obtained at the gates of the mixers for better mixer performance. The LO Buffer consumes 5 mA each. The total current consumed by the LO circuitry is 15 mA at 1.2 V.

For testing purposes, a simple 100 Ω resistive loaded differential pair is used for the IF stage. It provides 1.5 dB of gain. The size of the NMOS transistors was chosen to be 300 um x 0.25 um representing a trade-off between its 1/f noise contribution and bandwidth. A 1:√2 off-chip balun is used to match to the 50 ohms load. In real applications, a baseband amplifier with much higher gain can be used.

III. Measurement Results

The sub-harmonic downconverter was fabricated in the IBM 8RF 0.13 µm CMOS process [12]. The chip microphotograph is shown in Fig. 6. The active die area is 0.9 x 0.65 sq. mm.

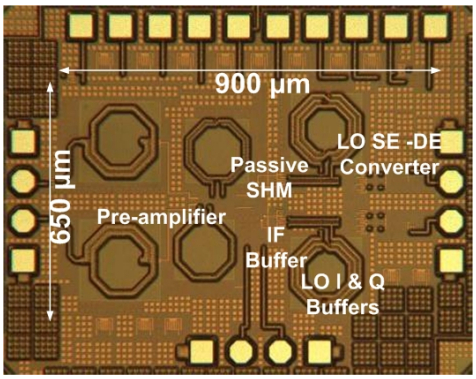

Fig.6. Chip microphotograph.

On-wafer probe testing was carried out using GSSG probes. A coaxial 180° hybrid was used for generating the 24 GHz differential signal. The quadrature 12 GHz LO was generated using a 90° hybrid. A 1:√2 off-chip balun is used to match to the 50 Ω load at IF.

The input return loss was less than 10 dB between 22.5 – 26 GHz. For a RF frequency of 23.1 GHz and an IF of 30 MHz, the measured DSB Noise Figure and Conversion Gain as a function of the gate bias is shown in Fig. 7.

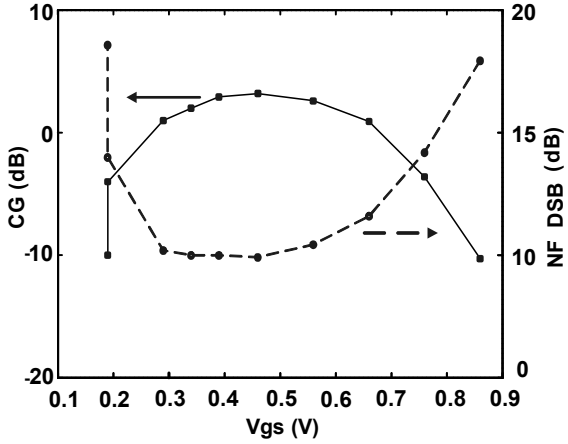

Fig. 7. Measured Conversion Gain and Noise Figure vs. dc gate-source bias voltage.

The measured input referred 1dB compression point was -12.7 dBm. This corresponds to an estimated IIP3 of -2.7 dBm. Fig 8. shows the input referred 1 dB compression point.

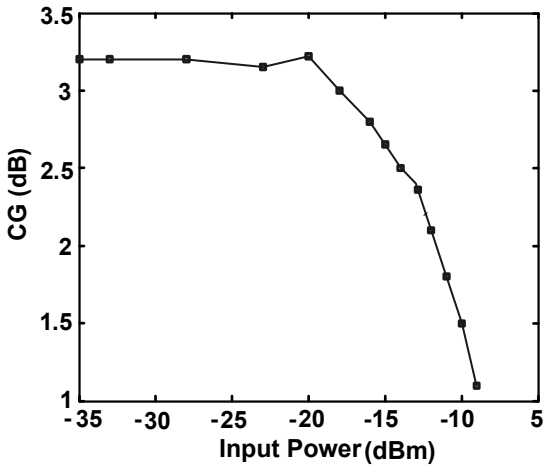

Fig. 8. Measured Input referred 1 dB Compression Point.

The IF 3 dB Bandwidth was 670 MHz, sufficient for GBPS data rates. The 2LO-RF isolation was 57 dB at 24 GHz. The S11 measured with and without LO switching was same indicating excellent 2LO-RF isolation.

Table I. summarizes the performance of the downconverter chip and also compares the performance with recently published work.

IV. Conclusion

This paper presents a downconverter based on a completely balanced passive sub-harmonic mixer in CMOS for 24 GHz direct-conversion applications. The downconverter has a conversion gain of 3.2 dB and a DSB Noise Figure of 10 dB. The input referred 1 dB compression point is -12.7 dBm. The mixer core including the pre-amplifier and the IF buffer consumes 8.5 mA at 1.6 V. The LO circuitry consumes 15 mA at 1.2 V. This downconverter can be used for zero-IF applications due to its high 2LO-RF isolation and 1/f noise performance. The downconverter can be preceded with a LNA in silicon or III-V technologies to set the overall system Noise Figure. Being completely balanced, it is very suitable for millimeter wave frequency bands.

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Reference	Frequency (GHz)	CG (dB)	DSB NF (dB)	IP_{1dB} (dBm)	Mixer Topology	Power Consumption (mW)	Technology
JSSC 2004 [2]	24	13	14.5	-	Gilbert Cell	40.5 *(includes IF amplifier)*	0.18 µm CMOS
ISSCC 2006 [6]	2.2	5	11	-10	Passive Double-Bal. SHM	7.2 *(includes pre-amplifier)*	0.13 µm CMOS
SiRF 2006 [8]	24	2	-	10	PMOS Folded Gilbert Cell	2 V – current not mentioned	0.18 µm CMOS
RFIC 2006 [9]	28	-11.02	8.6	-2.7	Passive Unbal. with LO Doubler	0.64	0.18 µm CMOS
Elec. Let. 2004 [10]	30	-2.6	10.5	-12.5	Gilbert Cell	20	90 nm CMOS
MWCL 2005 [11]	19	1	6	-12	Gilbert Cell	6.9	0.13 µm CMOS
This Work	**24**	**3.2**	**10**	**-12.7**	**Passive Double-Bal. SHM**	**13.6** ***(includes pre amplifier and IF buffer)***	**0.13 µm CMOS**

Table I. Performance comparison with recently published work.