A 10GS/s 5-bit Ultra-Low Power DAC for Spectral Encoded Ultra-Wideband Transmitters

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***Abstract* — A 5-bit 10Gs/s DAC for Spectral Encoded UWB transmitters is presented. A test counter is integrated on-chip to facilitate performance measurement. The chip has dimensions of 1.0x1.5mm, and is implemented in a 0.18µm SiGe BiCMOS process. The DAC operates at conversion rates of over 10Gs/s with a power dissipation of 12mW. Linearity results of the DAC at 5GS/s are presented, with the DNL < ±0.5LSB and INL < ±0.8LSB.**

***Index Terms* — 10GS/s, 5-bit, DAC, low power, spectral encoding, UWB.**

I. Introduction

An ultra-wideband (UWB) system, as defined by the FCC, operates in the 3.1GHz-10.6GHz frequency band, and has a minimum bandwidth of 500MHz [1]. As a result, UWB systems can overlay existing narrowband systems, such as the unlicensed band around 5GHz where 802.11a wireless local area networks (WLAN) and cordless telephones operate, as well as the 3.7GHz band for WiMAX [2]. As a result, UWB systems and these narrowband systems can mutually interfere.

To mitigate the interference caused by UWB systems, various spectral shaping techniques have been reported. For impulse radio based systems, such as pulse position modulation (PPM) [3], techniques such as pulse shapers [4] or coding [5] can be used to insert notches at the narrowband system frequencies. In OFDM-based UWB systems such as Multi-band OFDM (MB-ODFM) [6], cancellation tones can be used to insert in-band spectral notches [7].

Another method that can be used to perform spectral shaping is a technique called Spectral Encoding [8]. Its primary advantage is the ability to insert arbitrary spectral notches in a UWB spectrum to reduce the interference caused by UWB systems at the transmitter, and filter out unwanted interference caused by the narrowband systems at the receiver.

Implementation of such a system can be difficult. As described in [8] and [9], the Spectral Encoding algorithm can be implemented via the use of off-chip Surface Acoustic Wave (SAW) filters, which tend to be lossy and relatively expensive. To minimize cost, an integrated solution is favored over one that requires off-chip discrete SAW filters. As a result, a high-speed digital-to-analog converter (DAC) is required. Furthermore, the DAC must consume as little power as possible. The DAC will be connected directly to the antenna, and produces the output power of -41.5dBm/MHz.

In this paper, a 10GS/s 5-bit ultra low power DAC designed for Spectral Encoded UWB transmitters is designed, and initial results are presented. In Section II, the real-time Spectral Encoding algorithm will be briefly reviewed. Section III will describe the specifications and design of the DAC. Section IV will present some results on the performance of the implemented DAC. Conclusions will be given in Section V.

II. Spectral Encoding

Spectral Encoding can be considered a frequency domain counterpart to CDMA. The input signal is multiplied by a spreading sequence in the frequency domain, and the resulting signal is spread in *time*. Multiple access is achieved, in a manner similar to CDMA, by assigning different spreading sequences to different users.

As reported in [8], the Spectral Encoded system can combat narrowband interference (NBI). At the transmitter, the spreading sequence chips at the NBI frequencies are nulled. The resulting signal is still spread in time, but has a spectral notch at the NBI frequencies. At the receiver, the despreading operation involves multiplying the received signal's spectrum by the complex conjugate of the spreading sequence, including the nulled chips, which simultaneously despreads the desired waveform and nulls out any received NBI. Hence, this technique inherently provides interference mitigation at both the transmitter and receiver.

A block diagram of the real-time Spectral Encoded transmitter is shown in Fig. 1. It is composed of three blocks: the Fourier Transform (FT) block, the spectral encoding block, and the Inverse Fourier Transform (IFT) block. The FT an IFT blocks are both implemented using chirp transforms, and it has been suggested [8] that the

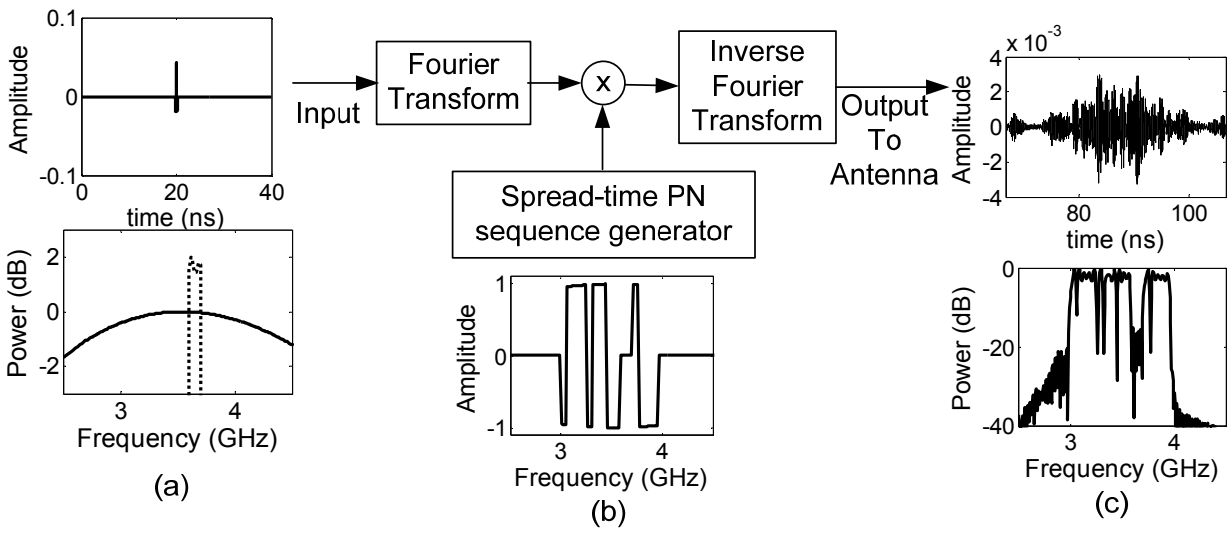

Fig. 1. Block diagram of the real-time Spectral Encoded UWB transmitter. (a) The unencoded UWB input signal waveform and spectrum, with a narrowband interferer at 3.6GHz. (b) Spectral Encoded spreading sequence of chip bandwidth 66.67MHz. The chips at the interference frequencies are nulled out. (c) The Spectral Encoded output waveform (time-spread) and spectrum.

chirp transform can be implemented by either a tap-delay line structure [10] or with SAW filters [11].

Fig. 1(a) shows the time domain representation of a pulse, with its spectrum. The location of the NBI is also shown. The spreading sequence shown in Fig. 1(b) has chips nulled out at the narrowband interferer's frequencies. The resulting Spectral Encoded time domain and power spectrum are shown in Fig. 1(c).

III. Spectral Encoded DAC Design

The DAC described in this paper is based on the system described in [9]. Instead of using SAW filters, a tap-delay line structure is used [8], which can be implemented in a DSP. A simplified block diagram of the system is shown in Fig. 2, which consists of a high speed memory, and the DAC. In this case, the waveform is pre-calculated and stored since the spreading sequence is known *a priori*. This waveform is subsequently fed to the DAC, which in turn is connected to the antenna.

The operational frequency band is from 3.1-5GHz, which is similar to Mode 1 operation for MB-OFDM systems [6], so the required conversion rate is ≥10GS/s. From the simulation results of Fig. 3, the minimum DAC resolution to achieve a 20dB notch depth for a Spectral Encoded system is five bits. Thus, for a 10GS/s 5-bit DAC, if the symbol duration is 35ns for the Spectral Encoded system, then the required memory size for a symbol is approximately 1750 bits.

A current steering architecture is used for this DAC [12]. The switching core for each bit is composed of bipolar transistors, with the LSB using minimum sized transistors. To minimize glitch energy, the two most significant bits (MSBs) are converted into three segmented (equally weighted) bits, and the three least significant bits (LSBs) are binary weighted, as shown in Fig. 4. The DAC operates at Vdd=1.8V, and the total current consumption is 3.2mA including the current mirror biasing circuit. Thus, the expected swing at the outputs in a 50Ω load is 160mV peak-to-peak per leg and a total power dissipation of 5.74mW. From simulation, the instantaneous peak power to average power ratio is roughly 16.5dB, and this corresponds to an average power of 0.5μW, which is compatible with the FCC limit of -41.25dBm/MHz for a UWB signal with a bandwidth of 500MHz.

To facilitate the testing of the DAC at high speeds, a high-speed counter is integrated on chip, and the overall block diagram is shown in Fig. 5. Fig. 6 shows the 5-bit counter. For this type of counter, the speed limiting factor will be the carry path from the LSB to the MSB. As shown in Fig. 6, the longest carry bit path is from bit R1 to bit R4, and can operate at the required 10GHz rate. The counter counts from 0 to 31 before resetting. All of the gates were implemented using standard CML.

The next block is the bit-converter, which converts the 5-bit binary counter output into the six bits that will control the DAC switching cores. Due to the long carry path, the outputs may be valid at different times, and a flip-flop block synchronizes all six signals. Finally, a buffer is inserted between the flip-flop block and the DAC to ensure fast switching.

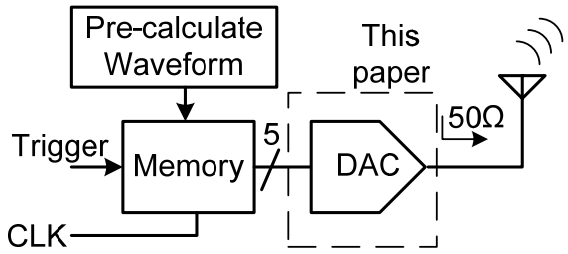

Fig. 2. Block diagram of the Spectral Encoded UWB transmitter, with the DSP, memory, and DAC integrated on chip. The DAC directly drives the antenna.

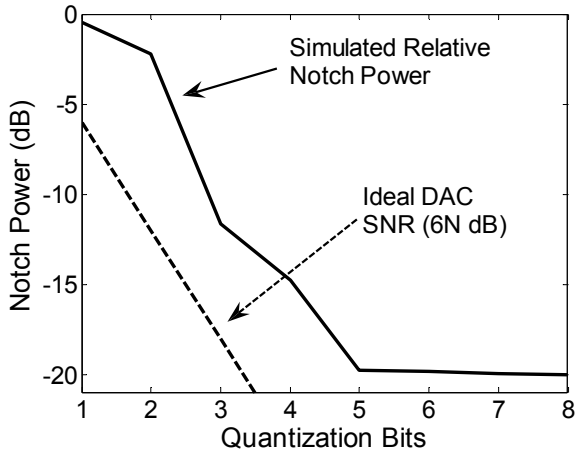

Fig. 3. Simulated notch power vs. DAC resolution. The notch power is limited by the symbol duration [9], which is 35ns for this plot.

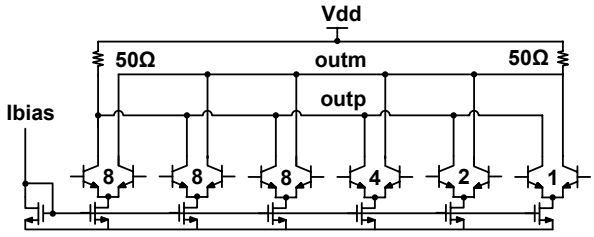

Fig. 4. Circuit diagram of the 5-bit DAC. The three LSBs are binary weighted, and the two MSBs are equally weighted.

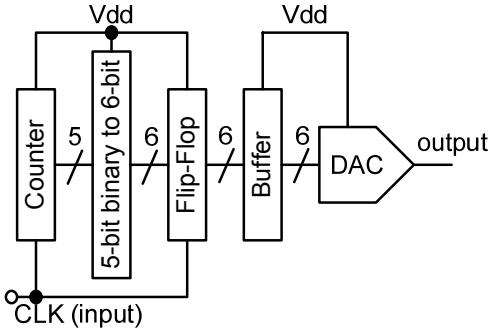

Fig. 5. Test chip block diagram.

IV. Experimental Results

The chip was implemented in Jazz Semiconductor's 0.18μm SiGe BiCMOS process [13]. A micrograph of the chip is shown in Fig. 7, whose dimensions are 1.0x1.5mm. The input to the chip is a sinusoidal clock signal at the desired conversion rate.

Fig. 8 shows the measured DAC output at conversion rates of 2GS/s, 5GS/s and 10GS/s. At 5GS/s, Vdd is set at 1.7V and the DAC consumes 10.2mW. At 10GS/s, it consumes 12mW. The dynamic INL (integral non-linearity) and DNL (differential non-linearity) measurements are shown in Fig. 9, and the DNL is less than ±0.6LSB and the INL is within ±1 LSB.

The DAC bias currents and Vdd were tuned at various frequencies to obtain the lowest operating power while maintaining static linear performance. A figure-of-merit (FOM), defined as the ratio between the conversion rate and the product of the dc power and resolution, is shown in Fig. 10. This result shows that this DAC has one of the best FOMs of any reported DAC in this frequency range and resolution.

V. Conclusion

An ultra-low power high speed DAC for use with Spectral Encoded UWB systems is described. The DAC uses a hybrid architecture. The DAC can operate at a conversion rate of over 10GS/s. At 5GS/s, the DNL is within 0.5LSB, INL is within 0.8LSB, and the DAC consumes 10.2mW.

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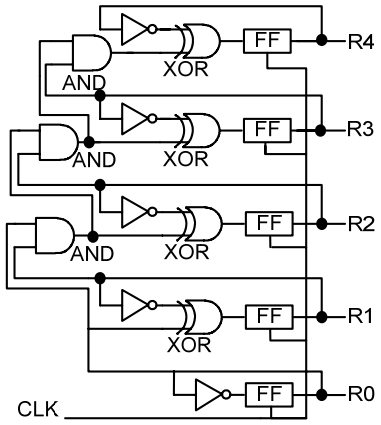

Fig. 6. Five-bit counter block diagram.

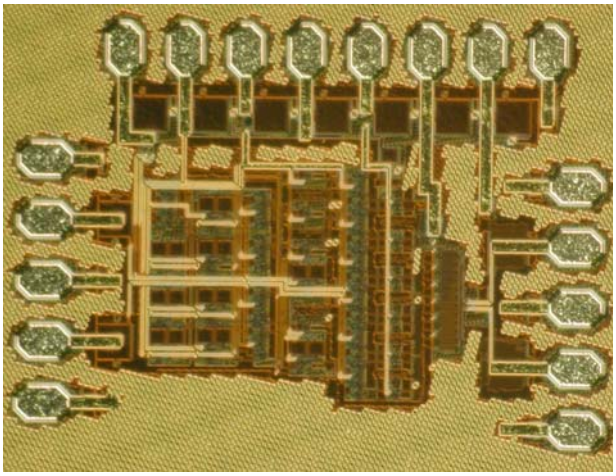

Fig. 7. DAC/Counter microphotograph.

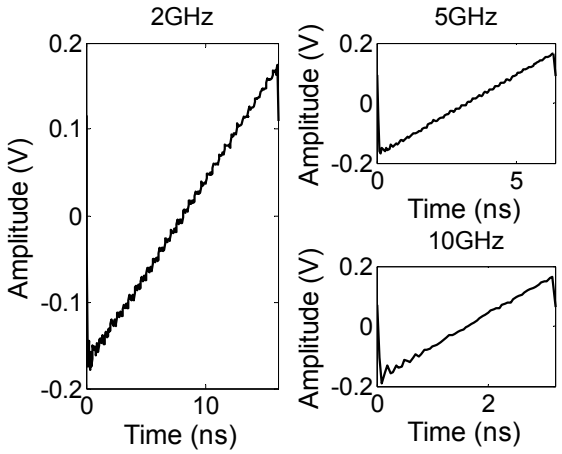

Fig. 8. Measured DAC output at 2GHz, 5GHz and 10GHz.

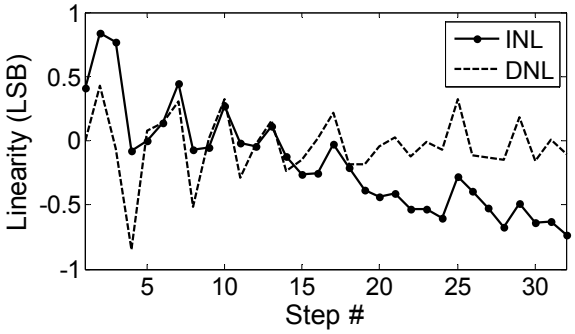

Fig. 9 Dynamic INL and DNL for the DAC operating at 5GHz.

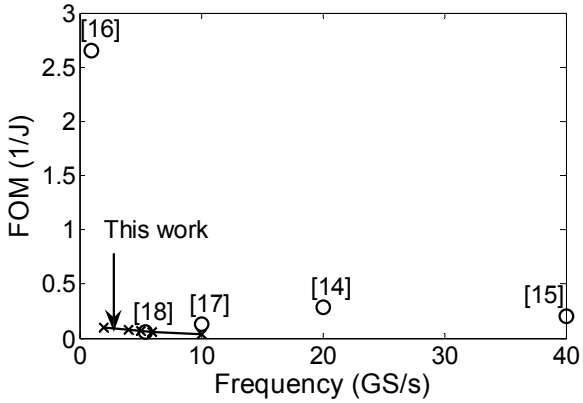

Fig. 10 Figure of Merit (FOM) of the DAC (marked by x) compared with previously reported DACs in this frequency range (marked by circles).