Power/Area Trade-Offs in Low-Power/Low-Area Unary-R-2R CMOS Digital-to-Analog Converters

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Abstract— **Performance trade offs of unary-*R*-2*R* and unary-binary digital-to-analog converters are presented. It is shown that for a given resolution and sampling rate, the active area of the unary-binary converter grows as the operating current of the unit cells approaches the weak inversion region. At very low-currents, the unary-*R*-2*R* architecture has a large area advantage over the unary-binary architecture for medium resolution, medium-speed applications.**

I. INTRODUCTION

Wireless polar transmitters require a very low power, compact, medium-resolution, and medium-speed digital-to-analog converter (DAC) as part of the baseband signal processing [1,2]. A current steering DAC is often used for this application [3-7]. At very low power, the bias current of the individual cells of the current steering DAC approaches the weak inversion region, where the matching between the devices is worse [8,9]. As a result, the converter's active area must grow (in order to maintain acceptable matching) if its unit cells are biased in the moderate to weak inversion region. This is the well-known fundamental tradeoff between area and current consumption in DACs.

A combined *R*-2*R* ladder/unary current-steering array can be used as an alternative to the traditional unary-binary current steering DAC to achieve a compact layout and a sub-μA least significant bit current. This is achieved, with a resulting trade off between current consumption and signal-to-noise ratio [1].

This paper quantifies the performance tradeoffs of the unary-*R*-2*R* architecture and compares them with the unary-binary current steering DAC. Section II reviews basic characteristics of the unary-*R*-2*R* DAC. Static linearity and the trade off between current consumption and the signal-to-noise ratio will be analyzed. The effect of least significant bit (LSB) delay on the output spurious-free-dynamic-range (SFDR) will be presented. Using a simplified area model, the active area of the unary-binary current mode DAC is compared to that of the unary-*R*-2*R* DAC in Section III. It will be shown that the unary-*R*-2*R* architecture benefits from a smaller layout and lower power consumption for medium-resolution medium-speed DAC applications. The paper concludes in Section IV.

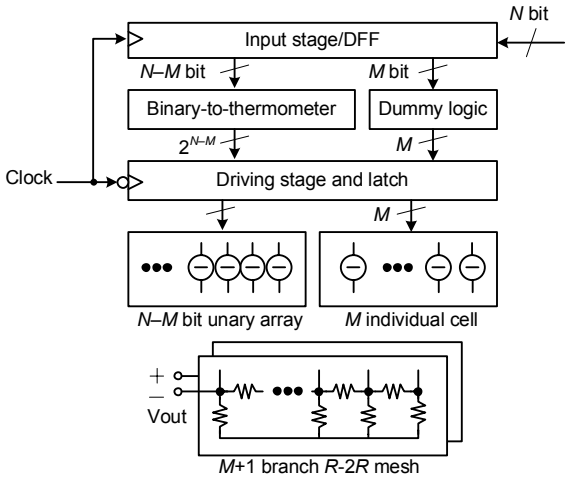

Figure 1 General block diagram of an *N*-bit unary-*R*-2*R* DAC with *M* individual cells (*R*-2*R* bits) and *N*-*M* bit unary array [1].

II. UNARY-R-2R ARCHITECTRURE

Fig 1 shows a general block diagram of a unary-*R*-2*R* voltage-mode DAC. An *N*-bit unary-*R*-2*R* DAC is composed of an *N*-*M* bit unary array and *M* individual current cells connected to an *M*+1 branch *R*-2*R* mesh. Unlike the unary-binary architecture, all the $2^{N-M}+M$ current cells are equal sized [1]. The binary fraction of the LSB current is generated through the resistor ladder. If each current cell has an operating current of *I*, the LSB current will be $I/2^M$. As opposed to the unary-binary architecture, small LSB currents can be achieved without biasing the current cells in weak inversion. This relaxes the required matching when a low power DAC is desired.

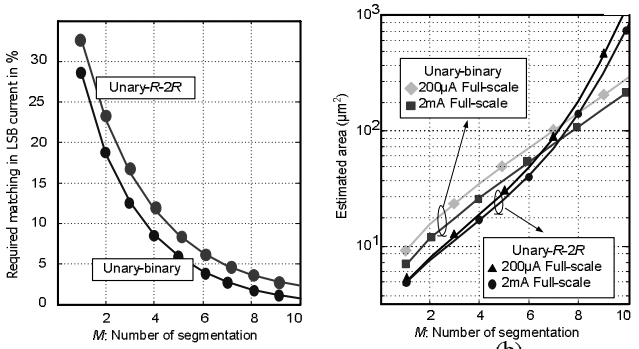

Figure 2 (a) Required matching in LSB current for unary-binary and unary-*R*-2*R* DAC in % (b) Estimated active area of the unit cell for a unary-binary and unary-*R*-2*R* DAC when the full-scale is 200μA and 2mA.

A. Static Linearity Requirements of Unary R-2R Architectre

Assuming each unit current cell has a random error, the maximum differential nonlinearity (DNL) occurs during the transition when the first M individual unit cells switch from one to zero and a unit cell from the unary array switches from zero to one. To have a DNL less than LSB/2, one can write:

$$I_{\text{out}(M \text{ individual cells}=0 \,\&\, \text{one cell from unary array}=1)} - I_{\text{out}(M \text{ individual cells}=1 \,\&\, \text{unary}=0)} - I_{LSB} \leqslant \frac{I_{LSB}}{2} \quad (1)$$

If each current cell is represented by $I+\Delta I_i$, in which ΔI_i is the random mismatch in the operating current of the current cell, (1) can be rewritten as:

$$(I+\Delta I_{M+1}) - \left(\sum_{i=1}^{M}\frac{I+\Delta I_i}{2^i}\right) - I_{LSB} \leqslant \frac{I_{LSB}}{2} \quad (2)$$

Since the LSB current is $I/2^M$ (2) can be rearranged as:

$$\left(I+\sum_{i=1}^{M}\frac{I}{2^i}-\frac{I}{2^M}\right)+\left(\Delta I_{M+1}-\sum_{i=1}^{M}\frac{\Delta I_i}{2^i}\right) \leqslant \frac{I_{LSB}}{2} \quad (3)$$

The terms in the first parenthesis sum to zero. Since ΔI_i's are independent and normally distributed, the terms in second parenthesis can be written in terms of the probability that holds the inequality:

$$P\left\{\Delta I_{M+1}-\sum_{i=1}^{M}\frac{\Delta I_i}{2^i} \leq \frac{I_{LSB}}{2}\right\} \geq Y \quad (4)$$

In which Y is the required yield and $0<Y<1$. Since the ΔI_i's are zero-mean, independent, and normally distributed, any linear combination of them is also a zero-mean normal distribution. If X is defined as:

$$X \equiv \Delta I_{M+1} - \sum_{i=1}^{M}\frac{\Delta I_i}{2^i} \quad (5)$$

And assuming $\sigma_{\Delta I}$ is the standard variation of ΔI_i, standard variation of X would be:

$$\sigma_X = \sigma_{\Delta I}\sqrt{1+\sum_{i=1}^{M}\frac{1}{4^i}} \quad (6)$$

Rearranging the indexes and solving the geometric series, one can get:

$$\sigma_X = \sigma_{\Delta I}\sqrt{1+\sum_{i=1}^{M}\frac{1}{4^i}} = \sigma_{\Delta I}\sqrt{\sum_{i=0}^{M}\frac{1}{4^i}} \quad (7)$$

$$\sigma_X = \sigma_{\Delta I}\sqrt{\frac{4}{3}\left(1-\frac{1}{4^{M+1}}\right)} \quad (8)$$

Using (5) and the standard normal distribution function, Φ, the left side of the equation (4) can be rewritten as:

$$P\left\{\Delta I_{M+1}-\sum_{i=1}^{M}\frac{\Delta I_i}{2^i} \leq \frac{I_{LSB}}{2}\right\} = P\left\{X \leq \frac{I_{LSB}}{2}\right\} = \Phi\left(\frac{I_{LSB}/2}{\sigma_X}\right) \quad (9)$$

Using (9), (4) can be further simplified to:

$$\Phi\left(\frac{I_{LSB}/2}{\sigma_X}\right) \geq Y \quad (10)$$

$$\frac{I_{LSB}/2}{\sigma_X} \geq \Phi^{-1}(Y) \quad (11)$$

In which $\Phi^{-1}(Y)$ is the inverse standard normal distribution function. Replacing (8) in (11) and using $I_{LSB}=I/2^M$, (11) can be rewritten as:

$$\Phi^{-1}(Y)\frac{\sigma_{\Delta I}}{I} \leq \frac{1}{2\sqrt{(4^{M+1}-1)/3}} \quad (12)$$

Equation (12) defines the required current matching for a given number of R-2R bits, M, and the required yield, Y. In order to compare this result with the matching requirement of the unary-binary DAC, (12) can be rewritten in terms of LSB current:

$$\Phi^{-1}(Y)\frac{\sigma_{\Delta I_{LSB}}}{I_{LSB}} \leq \frac{1}{2}\sqrt{\frac{3\times 2^M}{4^{M+1}-1}} \quad (13)$$

With a similar approach the required current matching to meet the DNL specification in the unary-binary architecture is calculated as:

$$\Phi^{-1}(Y)\frac{\sigma_{\Delta I_{LSB}}}{I_{LSB}} \leq \frac{1}{2\sqrt{2^{M+1}-1}} \quad (14)$$

In which M is the number of binary weighted bits [3]. Equations (13) and (14) show that required matching to meet the DNL specification is generally more relaxed in the unary-R-2R than in the unary-binary architecture. Fig 2(a) shows required LSB matching in the current cell for a unary-R-2R and the unary-binary architecture versus segmentation factor M. Using (12) and the size versus matching relation of the MOSFET drain current [3,7,8,10], the unit cells active areas A_y can be estimated as follows:

$$\frac{4(4^{M+1}-1)}{3}\left(\Phi^{-1}(Y)\right)^2\left(\frac{4A_t^2}{(V_{GS}-V_t)^2}+A_\beta^2\right) \leqslant A_y \quad (15)$$

Where A_t and A_β are empirical coefficients usually provided by the foundry [3,4,7,10]. Using (14) and a similar approach, the active area of the unary-binary unit cell can be estimated [3,7]. Fig 2(b) shows the required unit cell active area for both the unary-R-2R and unary-binary DAC for the cases where the LSB current is approaching the weak and strong inversion regions, corresponding to 200μA and 2mA full-scale current, respectively. The active area is smaller for the unary-R-2R architecture due to relaxed required matching at low segmentation values. The area advantage is

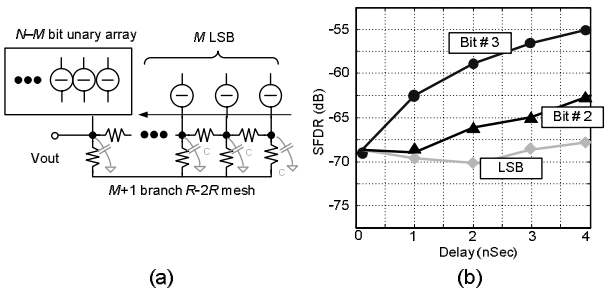

Figure 3 (a) Output resistor ladder of the unary-*R*-2*R* DAC along with the parasitic capacitors create a propagation delay from the LSBs to the output of the DAC. (b) SFDR degradation in a 10-b unary-*R*-2*R* DAC with 3 *R*-2*R* bits due to delay on the first three LSBs.

greatest when the LSB current is very small (full-scale of 200μA), which causes the binary-unary unit cells to be in weak-to-moderate inversion, where matching is worse [1,8-10]. This limitation is not the case for the unary-*R*-2*R* architecture where the current cells are biased a factor 2^M times larger than the LSB and are still in strong inversion.

B. Effects of RC Delay and Effective Bandwidth Considerations

Fig 3(a) shows the resistor ladder of the unary-*R*-2*R* DAC segmented into *M* LSBs, an *N*-*M* bit unary array and their associated parasitic capacitors. There is a delay from the moment an LSB changes its state to the time the output of the unary-*R*-2*R* DAC is affected. This delay is caused by the *RC* time constant through the *R*-2*R* ladder and differs from one LSB to another. It causes distortion at the output of the DAC and limits the spur-free dynamic range (SFDR). SFDR degradation due to this delay depends on the number of *R*-2*R* stages, the input waveform and the sampling rate. Fig 3(b) shows the simulated SFDR degradation versus the delay for the first three bits in a 10-bit 200MHz unary-*R*-2*R* DAC with a 7-bit unary array and a 50MHz full-scale input sine-wave. A 1nS delay on the third LSB drops the SFDR to –62dB; 7dB higher than the ideal case, while a 3nS delay on the first LSB does not significantly affect the SFDR. If the *i*th LSB of a unary-*R*-2*R* DAC switches from zero to one, it goes through *M*–*i* *RC* time constants and has to settle down to $1/2^i$ of its final value before it reaches the output. Then the effective delay of the *i*th LSB bit to the output, d_i, can be estimated as:

$$d_i \approx 0.7 \times i(M-i)\tau \qquad (16)$$

Where *M* is the number of *R*-2*R* bits, and τ is the *RC* product at the output of each *R*-2*R* current cell. Since an *R*-2*R* resistor mesh is used to generate the LSB fractions, the unary-*R*-2*R* DAC usually requires bigger resistor loads for a given voltage swing compared to the unary-binary architecture. This limits the SFDR at high resolution unary-*R*-2*R* DAC when too many *R*-2*R* stages are used. The *R*-2*R* ladder limits the effective bandwidth of the unary-*R*-2*R* DAC. For example, a 10-bit unary-*R*-2*R* DAC with full-scale voltage of 1.0V, 7-3 segmentation, and 200μA of full-scale current requires 2.6KΩ resistor in the loading mesh. If the output of the 7-bit unary array has a parasitic capacitance of 0.6pF, coming from the junction capacitor of the unit cells and their wirings, the output bandwidth would be only 100MHz.

C. Signal-to-Noise Ratio Considerations

At very small LSB currents and a given voltage swing at the output, the signal-to-noise-ratio (SNR) of the unary-*R*-2*R* DAC drops rapidly due to increasing resistor thermal noise [1]. This limits how low the LSB current can go while maintaining the desired SNR. Since all the current cells in a unary-*R*-2*R* DAC have the same size and operating current, the total differential thermal noise at the output will be:

$$i^2 = 2\frac{4KT}{R} + \left(2^{N-M}-1\right)i_n^2 + \sum_{i=1}^{M}\frac{i_n^2}{4^i} \qquad (17)$$

Where i_n^2 is the channel noise of each current cell, $4KT/R$ is the thermal noise of the resistor ladder, *R* is the equivalent resistor of the *R*-2*R* ladder, and i^2 is the total differential noise at the output of the DAC. i_n^2 is given by $8KTg_m/3$ where g_m is the transconductance of the current cell device. If *R* is replaced by the differential voltage swing divided by the full-scale current, (17) can be rewritten as:

$$i^2 = 16KT\left(\frac{I(2^N-1)}{2^M \times V_s} + (2^{N-M} - \frac{1}{3\times 4^M} - \frac{2}{3})\frac{g_m}{3}\right) \qquad (18)$$

Where V_s is the differential full-scale voltage at the output of the DAC. Signal-to-noise-ratio (both quantization and thermal) can then be calculated as the ratio of the full-scale current to the total noise current:

$$SNR = \frac{\frac{I(2^N-1)}{2^M\sqrt{2}}}{\sqrt{16KTB(\frac{g_m}{3}(2^{N-M} - \frac{1}{3}\times 4^{-M} - \frac{2}{3}) + \frac{(2^N-1)I}{2^M \times V_s}) + \left(\frac{I}{2^M\sqrt{12}}\right)^2}} \qquad (19)$$

Equation (19) defines a lower bound for the operating current *I* to meet the SNR specification for any given *N* and *M*. For example, for a 10-bit unary-*R*-2*R* DAC and a 1.0V full-scale voltage at the output, the operating current has to be greater than 1μA so that the SNR doesn't drop below 58dB [1]. Unlike the unary-binary architecture, this puts a lower bound on the static current consumption of the unary-*R*-2*R* DAC. The same consideration applies to the unary-binary DAC but only happens when the LSB current is a few tens of nA.

III. AREA ESTIMATE

Each current steering cell is composed of a cascaded current mirror and a switching differential pair. A digital encoder is used to combine the row-column bits of the unary array into the switching logic [4,7]. Followed by the encoder, there is a driving latch which also provides a make-before-break operation to minimize glitch currents at the

output [1,3,5]. The total converter area is the sum of the area of the current cells and the digital binary-to-thermometer decoders [7], i.e.

$$\text{Area} = (2^{N-M}+M).(A_y+.A_{sl})+2^{N-M}.A_{en}+A_{de}+A_{R-2R} \quad (20)$$

Where, A_y is the active area of the unit cell in the unary-R-2R architecture, A_{sl} is the area associated to the driving latch and the switching differential pair. A_{en} is the area of the row-column encoder of the unary array, and A_{de} is the area of the binary to thermometer decoder. Both A_{en} and A_{sl} are technology dependent parameter and independent of the choice of architecture. A_{de} grows exponentially as the number of bits in the thermometer array increases. Since the decoder is digital combinational logic, it will slightly affect the total area. $A_{R\text{-}2R}$ is the area associated with the R-2R ladder. Using (15), (20) provides a lower bound for the DAC's total active area:

$$\text{Area} \geq C.(4^{M+1}-1)(2^{N-M}+M)(4A_t^2/(V_{GS}-V_t)^2+A_\beta^2)+(2^{N-M}+M)A_{sl}+2^{N-M}A_{en}+A_{de}+A_{R\ 2R} \quad (21)$$

Where C is $(2\Phi^{-1}(Y)/\sqrt{3})^2$ and constant, N is the resolution of the DAC, M is the number of R-2R bits, V_{GS} and V_t are the gate-source and threshold voltage of the current cell device, and A_t and A_β are empirical technology dependent coefficients [3,10]. With a similar approach, the total area of the unary-binary DAC can be estimated in terms of similar parameters [7]. Fig 4 shows an area comparison for both unary-R-2R and unary-binary DAC for a given 10-bit resolution and 1V voltage swing at the output, versus the number of segmentation. The comparison is done for the two cases where the full-scale current is 200µA and 2mA. The Unary-R-2R architecture shows a smaller area due to relaxed matching requirement at small segmentation values. The area advantage is greater when low static current consumption is required (corresponding to 200µA full-scale), in which unary-binary unit cells are operating in weak inversion where matching is worse. The total area is dominated by the encoders' area at low segmentation values and by the active area of the current cells at high segmentation [7].

IV. CONCLUSION

Performance limitations of the unary-R-2R current-steering voltage mode DAC were analyzed. It was shown that the speed of unary-R-2R DAC is limited to the RC delay through the resistor ladder and the effective output bandwidth. A simplified area model of the converter was presented followed by a comparison between the unary-R-2R and unary-binary DAC. It was shown that the unary-R-2R DAC benefits from smaller active area especially in small LSB current, when the current cells of the unary-binary DAC are biased in weak inversion region.

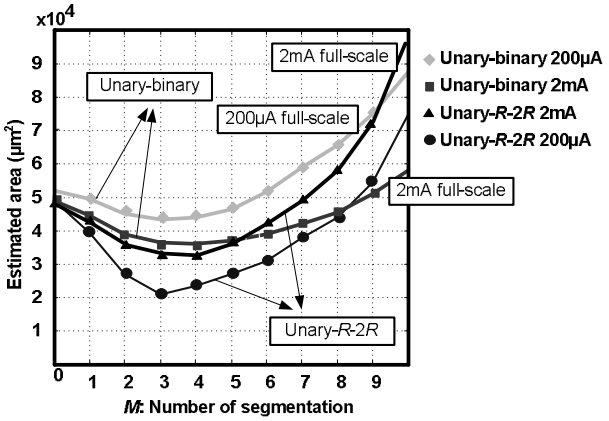

Figure 4 Area comparison for a unary-R-2R and unary-binary DAC. Resolution=10 bit, output full-scale voltage=1V [1].

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