A Monolithic Low-Distortion Low-Loss Silicon-on-Glass Varactor-Tuned Filter With Optimized Biasing

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***Abstract*—A low-distortion varactor-tuned bandpass filter is demonstrated on a high-Q silicon-on-glass technology. The dc bias network is optimized to achieve high linearity, the center frequency of the filter tunes from 2.4 to 3.5 GHz, and the measured loss of the filter is 2–3 dB at 2 GHz, with a stopband rejection of 25 dB. The measured IIP3 of the filter was +46 dBm.**

***Index Terms*—Adaptive systems, distortion, nonlinearities, tunable filter, varactors.**

I. Introduction

NEXT-GENERATION wireless systems require circuit techniques that facilitate radio frequency (RF) adaptivity. Some examples of adaptive circuits include tunable filters, tunable matching networks for low-noise and power amplifiers, and multiband voltage controlled oscillators (VCOs). An ideal tuning element for these applications will exhibit extremely low loss, low dc power consumption, high linearity, ruggedness to high voltage and high current, wide tuning range, high reliability, very low cost, low area usage, and be continuously tunable, with a high tuning speed. High linearity low-loss anti-series varactor diodes [Fig. 1(a)] are promising candidates for these applications [1]–[7]. We analyze an improved biasing scheme for these diodes, and demonstrate the performance of these tuning elements with a low-loss, high linearity, tunable bandpass filter (BPF).

II. Optimized Biasing of Anti-Series Varactor Diodes

As was pointed out in [3], a constant doping profile in the varactor diode results in essentially no distortion in the capacitance of an anti-series pair, which is highly desirable. To avoid linearity degradation by the center-tap impedance of the dc biasing network, this impedance should be significantly higher then the reactance of the varactors. In practical situations this is difficult to achieve, e.g. in a two-tone intermodulation test, the center-tap voltage has a component at the difference frequency Δf. When Δf approaches zero, the reactance of the varactors for this difference frequency component increases without bound. Consequently, the connecting center-tap impedance should become infinite to avoid linearity degradation. Referring to Fig. 1(a) [1], the requirement for linear operation of the varactor stack is

$$R_{BI} \gg \frac{1}{2\pi C_A \Delta f}. \tag{1}$$

For large tone-spacing this condition can be satisfied by an integrated resistor, but the resistance value—and hence the required die area—can become prohibitively large for even moderate tone spacings.

A simple way to implement the high impedance at the center-tap, while keeping the area required for the bias circuit small, is the use of a small anti-parallel diode pair, depicted in Fig. 1(b) [1]. The zero-bias impedance of the diodes is very high, but now the shunt capacitance of the diodes limits the linearity.

The effect of center-tap impedance on linearity is shown with a specific simulation example of IIP3 in Fig. 2. The figure shows three distinct regions of operation: the shunt dc leakage impedance of the diodes R_D limits the linearity at very low tone spacings, the zero-bias capacitance C_D of the anti-diode pair limits the IIP3 to a constant value at moderate tone spacings, and the linearity approaches the ideal infinite IIP3 at high tone spacings. In the regime of ultra-low tone spacing, where (1) cannot be satisfied, the modest IIP3 improvement over a single diode can be almost entirely explained by the factor of two reduction in the RF voltage across each diode. In the moderate tone spacing regime, where the anti-parallel biasing diode

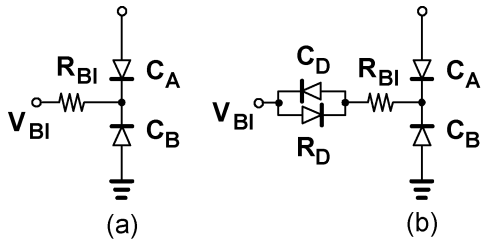

Fig. 1. (a) Low-distortion anti-series diode configuration with resistor bias. (b) Low-distortion anti-series diode configuration with resistor and anti-parallel diode bias for improved performance at low tone spacing.

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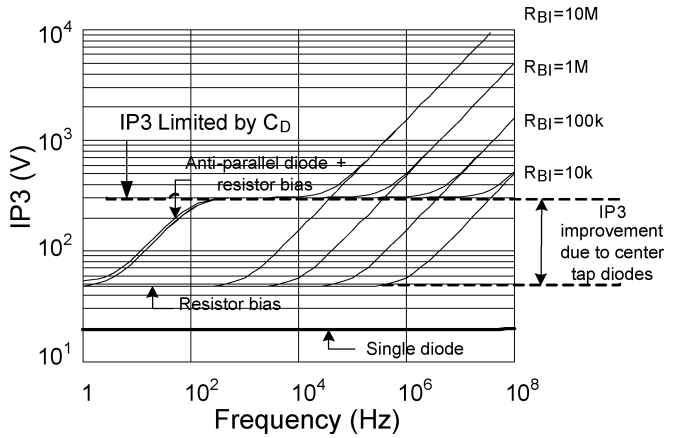

Fig. 2. Simulated IIP3(V) for a single varactor and an anti-series varactor pair as a function of tone spacing and center tap impedance ($f_c = 1$ GHz, $C_0 = 10$ pF, $V_{\text{center tap}} = 5$ V, $n = 0.5$, $C_D = 0.1$ pF).

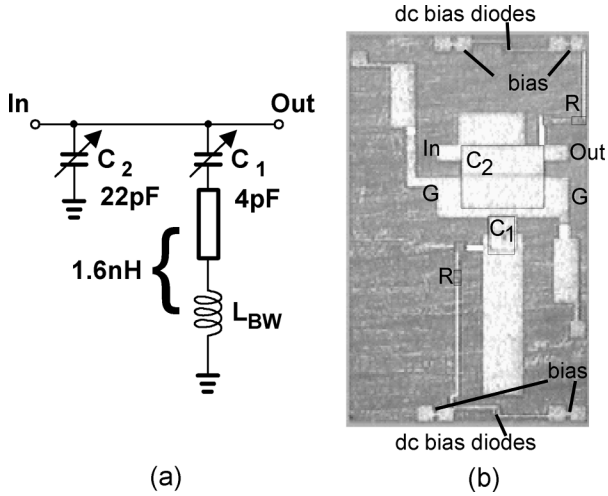

Fig. 3. (a) Schematic of the tunable BPF and (b) microphotograph of the BPF.

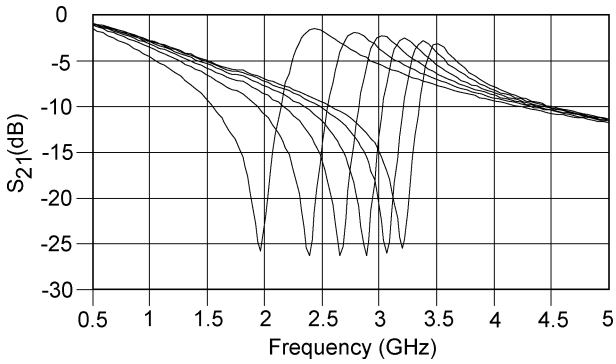

Fig. 4. Measured $|S21|$ versus frequency for tunable BPF.

capacitance limits the linearity, the IIP3 of the anti-series diode pair can be approximated by

$$IIP3(V) \approx 8(\phi + V_{BI})\sqrt{\frac{C_0}{3C_D}} \tag{2}$$

for the uniformly doped case where ϕ is the built-in potential of the diode, V_{BI} is the dc bias voltage, and C_0 is the series equivalent capacitance of the two diodes. This illustrates the importance of maintaining a low parasitic diode capacitance in the optimized dc bias circuit.

III. High Linearity Tunable Varactor-Based BPF

A dedicated silicon-on-glass varactor technology was used for this demonstration [1]. This technology provides a low loss substrate and metal patterning of both the front and back sides of the wafer, so the intrinsic varactor can be directly contacted by thick metal on both sides. The measured Q of the high capacitance (5–20 pF) varactors realized in this technology varied from 100 to 600 at 2 GHz [2].

We implemented a simple tunable single-pole/single zero filter (Fig. 3) in order to demonstrate the capabilities of the technology. A filter like this might eventually be part of a SAW filter replacement in a mobile handset, minimizing transmit leakage to the receiver/mixer in frequency-duplex cellular systems. The requirements for such a filter are extremely low loss in the receive band, high rejection in the transmit band, and high linearity to avoid cross-modulation distortion. A combination of low-loss on-chip microstrip transmission lines and bondwires was utilized to create the required high-Q on-chip inductance.

The measured tunable filter insertion loss and stopband suppression is shown in Fig. 4, and the loss in the passband is 2–3 dB over the 1-GHz center frequency variation. The dc bias was varied from 1 to 13.5 V to tune the filter from 2.4 to 3.5 GHz. Although the dc tuning voltage is quite high, very little dc current is required for the tuning, because the diodes are reverse biased.

The pole-zero spacing for this filter was set to 400 MHz and a triple-beat/XMOD distortion test was performed in order to characterize the large-signal behavior. For this purpose, two signals are presented at the stopband at 1.999 and 2.001 GHz with a power level of -5.6 dBm. A jammer signal ($f_{\text{jam}} = 2.5$ GHz, 0 dBm) signal is presented in the passband. The resulting cross-modulation distortion components at $f_{\text{dist}} = 2.498$ and 2.502 GHz, are -98.5 dBc with respect to the jammer signal. The resulting IIP3 for this test condition is calculated to be

$$IIP3 \approx 10log(2) + P_{txl} - \frac{\Delta P_{xmod}}{2} = 46\,\text{dBm}. \tag{3}$$

In addition, a traditional two-tone test was performed in the passband of the filter, also yielding an IIP3 of $+46$ dBm, confirming the cross-modulation derived IIP3 value.

IV. Conclusion

The performance of the filter, in terms of loss, size, cost, tuning range, power handling, and linearity, are compatible with current requirements in modern communication systems. Our expectation is that these new, cost-effective components providing true RF adaptivity, will dramatically improve the performance of future wireless systems.

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