Design of H-Bridge Class-D Power Amplifiers for Digital Pulse Modulation Transmitters

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***Abstract*—This paper presents an H-bridge class-D power amplifier (PA) for digital pulse modulation transmitters. The class-D amplifier can be driven by two- or three-level digital signals generated by a delta–sigma modulator (DSM) and provides a linear microwave output after filtering. Within the amplifier, the pull-up and pull-down devices are driven separately to improve the amplifier efficiency by minimizing the loss associated with shoot-through current. The H-bridge class-D PA system was tested with code-division multiple-access IS-95 signals at 800 MHz. Using binary DSM signals, a drain efficiency of 31% was achieved with an output power of 15 dBm and an adjacent channel power ratio of −43 dBc. With three-level DSM signals, a drain efficiency of 33% was achieved at same output power. An analysis of the factors governing amplifier efficiency is provided.**

***Index Terms*—Bandpass delta–sigma modulation (BPDSM), class-D amplifier, code-division multiple access (CDMA), complementary metal–oxide semiconductor (CMOS), radio-frequency power amplifier (RF PA).**

I. Introduction

With the rapid advance of CMOS technology, digital signal processing (DSP) techniques can be used at clock frequencies reaching into the microwave region. This permits the implementation of digital radio-frequency (RF) systems that can carry out functions which up to now have been exclusively in the domain of analog circuits [1]–[5]. In digital RF transmitters, signal processing functions such as baseband signal generation, filtering, and frequency conversion are completed in the digital domain. This digital approach increases the flexibility and programmability of the system and avoids the problems of aging, variable component values, and impedance conversion difficulties associated with many analog circuits. It is also conducive to system-on-chip implementation independent of technology node. Fig. 1 shows a possible architecture for a digital pulse modulation transmitter [6]. Via DSP techniques, the modulated baseband signals are generated, up-converted, and sent to a bandpass delta–sigma modulator (BPDSM). The BPDSM quantizes the signals into a binary format to drive the following amplifier stage. The associated quantization noise can be spectrally shaped out of band by the BPDSM. The bandpass filter following the amplifier avoids power dissipation at undesired frequencies to achieve high efficiency. In addition to binary signals, digital transmitters with three-level DSMs are possible [7]. These can potentially exhibit higher amplifier efficiency by encoding more power in the desired frequency band while maintaining the signal quality.

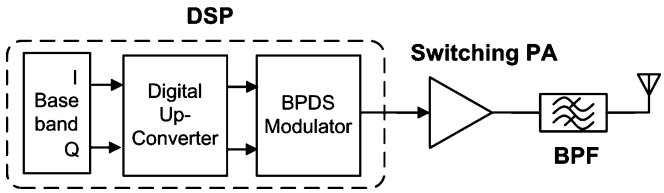

Fig. 1. Simplified block diagram of possible future digital RF transmitters with BPDSMs.

Switching amplifiers are attractive candidates for digital RF transmitters because of their potential to obtain high efficiency. However, the suitable types of switching amplifiers are limited by the fact that the digital driving signals are nonperiodic and broadband. For instance, class-E amplifiers can operate at RF frequencies efficiently by minimizing the output capacitance loss. However, the zero-voltage switching condition for compensating the output capacitance loss cannot be maintained under nonperiodic driving conditions, and thus the conventional class-E amplifier cannot achieve high efficiency when driven by the delta–sigma-modulated signals.

Voltage-mode class-D switching amplifiers have the potential to maintain high efficiency when the driving signals are not periodic [8]–[15]. However, loss associated with the driving circuits, the active devices (including shoot-through current loss), and filters (poor power recycling) can degrade the performance significantly. Previously, a bandpass delta–sigma class-S amplifier was demonstrated at 10 MHz, showing 33% drain efficiency with an IM3 of −40 dBc [16]. A transformer-coupled amplifier was demonstrated at 170 MHz with a drain efficiency of 8% [17]. A class-D power amplifier (PA) with a digital modulator based on quadrature pulse modulation was also demonstrated for EDGE signals [18].

This paper reports an H-bridge class-D amplifier implemented in CMOS which can be used in digital RF transmitters based on DSM for linear and efficient amplification. The pull-up and pull-down devices of the class-D amplifiers were driven separately to minimize the loss associated with the shoot-through currents. The H-bridge amplifier achieved a drain efficiency of 62% with 800-MHz periodic signals. For code-division multiple access (CDMA) IS-95 signals, the amplifier was driven by delta–sigma-modulated signals with

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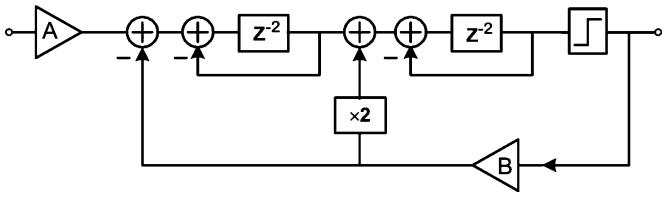

Fig. 2. Block diagram of a BPDSM for two-level DSM signals. This modulator consists of two resonators, two feedback loops, and a two-level quantizer.

a clock rate of 3.2 GHz. For two-level delta–sigma signals, a drain efficiency of 31% was achieved with an output power of 15 dBm and an adjacent channel power ratio (ACPR) of −43 dBc. The drain efficiency of the amplifier was improved to 33% by using three-level delta–sigma modulation signals while maintaining an ACPR of −43 dBc.

The factors degrading the efficiency of the class-D amplifier driven by the DSM signals are considered in Section IV. Analytical expressions for output power and efficiency are provided, which allow estimation of amplifier performance.

II. BPDSM Signals

A. Two-Level Quantization

The driving signals of the H-bridge class-D amplifier were generated by a simulated BPDSM driven by CDMA-like quaternay phase-shift keying (QPSK) signals with bandwidth of 1.23 MHz and a 5.5-dB peak-to-average power ratio. The BPDSM, as shown in Fig. 2, was composed of two resonators, one two-level quantizer, and two feedback loops, running at a clock rate of 3.2 GHz. The spectrum of the output binary signals is shown in Fig. 3. The desired signals are centered at 800 MHz (rather than in the range 825–850 MHz due to limitations on our equipment for signal generation). Fig. 3 (bottom) shows an expanded view of the signal spectrum from 700 to 900 MHz. The quantization noise was spectrally shaped and removed out of band. A bandpass filter is required to further reduce the out-of-band power including the harmonics and the quantization noise.

For CDMA signals, the integrated power over the occupied signal bandwidth (1.23 MHz) is defined as the in-band power. The in-band power ratio, i. e. the ratio of the in-band power to the total power contained in the digital signal, can be controlled and maximized by adjusting the feedback coefficient ratio, also defined as coding efficiency in [15] and given by B/A in Fig. 2. Fig. 4 shows the in-band power ratio as a function of the feedback coefficient ratio B/A. Also shown is the in-band power ratio for the three-level DSM considered below. A lower feedback coefficient ratio gives a higher ratio of the desired in-band power to the total power. DSM driving signals with a higher in-band power ratio lead to higher amplifier output power. In turn, since some loss mechanisms such as capacitance loss are independent of the output power, higher output power leads to higher amplifier efficiency. However, signal quality is degraded with increasing in-band power ratio. Fig. 5 displays the simulated ACPR and error vector magnitude (EVM) of the signals with increasing in-band power ratio. The maximum power ratio is determined by the EVM and ACPR specifications of the system, which determine the tradeoff between PA efficiency and signal quality.

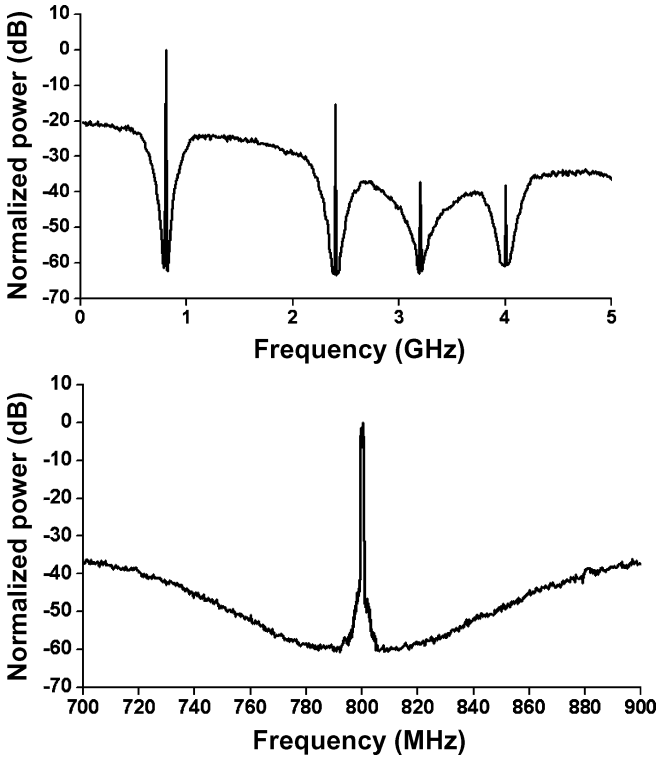

Fig. 3. (*top*) Spectrum of the DSM signals, showing that the quantization noise is shaped and removed out of band. (*bottom*) Expanded spectrum of top figure from 700 to 900 MHz.

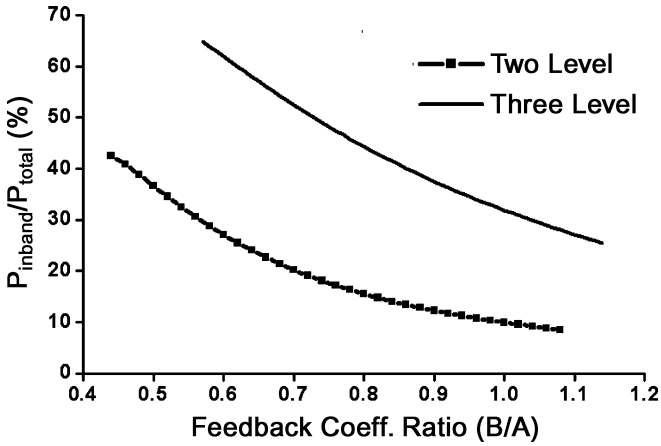

Fig. 4. In-band power ratio as a function of the feedback coefficient ratio B/A.

B. Three-Level Quantization

Signals with higher in-band power ratio for a given signal quality factor (EVM or ACPR) have the potential to achieve higher amplifier efficiency. Changing to a three-level quantizer, as shown in Fig. 6, can increase the in-band power ratio. Fig. 7 shows the simulated ACPR and EVM of the three-level DSM signals as a function of in-band power ratio, with CDMA input signals. Compared with two-level DSM signals, more in-band power can be encoded in the three-level signals for given ACPR

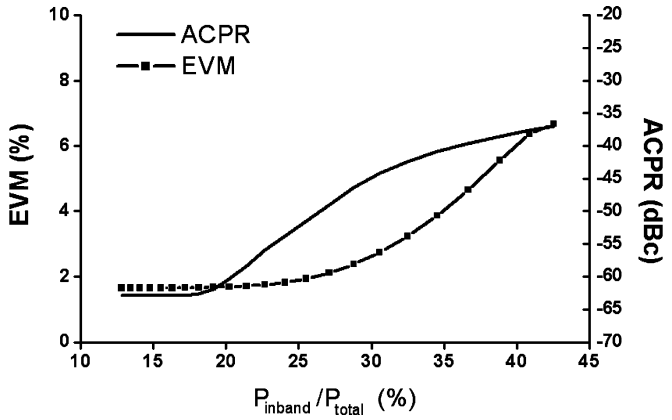

Fig. 5. Simulated ACPR and EVM for CDMA signals after passing through the DSM with a two-level quantizer as a function of in-band power ratio.

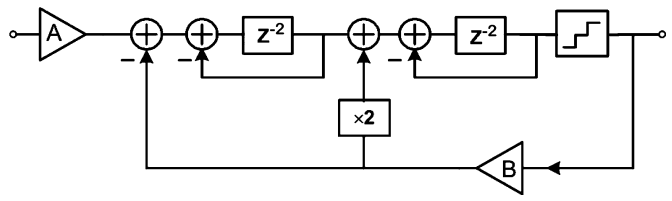

Fig. 6. Block diagram of a three-level BPDSM that uses a three-level quantizer.

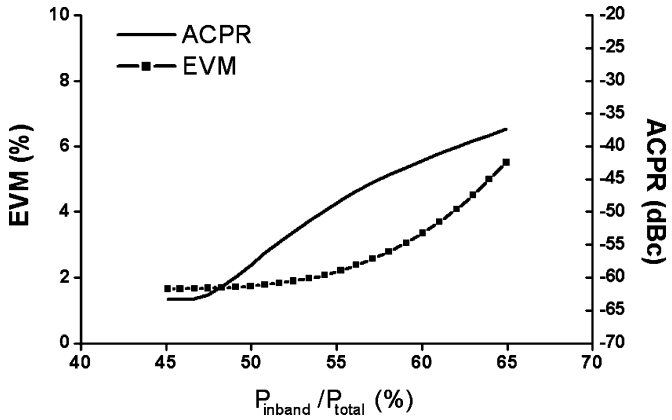

Fig. 7. Simulated ACPR and EVM for CDMA signals after passing through the DSM with a three-level quantizer as a function of in-band power ratio.

and EVM. However, to amplify the three-level delta–sigma signals, the amplifiers are required to differentiate between three input states and generate corresponding outputs.

III. H-Bridge Class-D Amplifiers

In a voltage-mode class-D amplifier, the output transistors are operated as switches. The switched voltage waveform is applied to a series resonator, which exhibits a high impedance at all frequencies except for the resonant frequency, thus removing the out-of-band signals such as harmonics and quantization noise. Since no current flows outside of the desired frequency band, no power is dissipated at these frequencies. Since the two devices are switched alternately, a voltage-mode class-D amplifier can be approximated as a voltage-controlled voltage source, which operates efficiently when feeding a series resonator. This

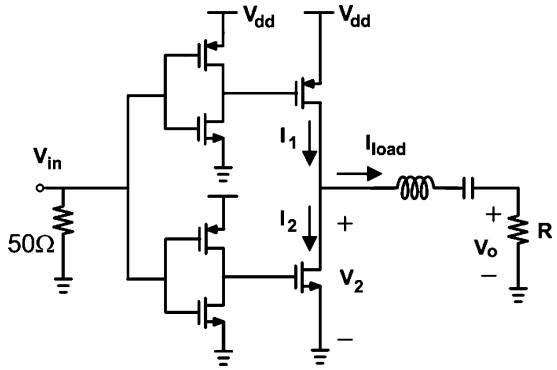

Fig. 8. Schematic of the voltage-mode class-D PA with shoot-through current suppression by separating the driver for pMOS and nMOS at the output stage.

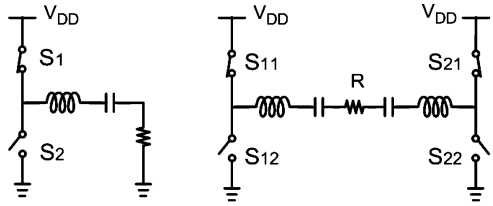

Fig. 9. (*left*) Schematic of a class-D PA. (*right*) Schematic of an H-bridge class-D PA.

high-efficiency feature can be maintained even if it is driven by nonperiodic digital signals, as long as the reverse currents appearing in this condition can be provided by the active devices or parallel diodes during the ON state [9].

During the ON/OFF transition of the active devices, there is generally a short period of time when both pMOS and nMOS transistors are ON, resulting in a low resistance between power supply and ground. A large current (known as shoot-through current) may be induced, which can cause significant energy loss. To minimize this loss, the pMOS and nMOS were designed to have different driving circuits, as shown in Fig. 8. By modifying the pull-up and pull-down device size ratio of the drivers, the overlap of the turn-on time between the pMOS and the nMOS during the transition can be minimized.

A voltage-mode class-D amplifier is suitable for DSM systems employing two-level DSM signals. As shown in Fig. 9 (left), the driving signal states correspond to the two states of the class-D amplifier operation. For example, level 1 corresponds to S1 ON and S2 OFF. Level 0 corresponds to S1 OFF and S2 ON. However, a single class-D amplifier is unable to differentiate the three driving states associated with three-level DSM signals. Thus, two class-D amplifiers were configured in an H-bridge fashion, as shown in Fig. 9 (right). Two pairs of switches operate to produce the three different driving conditions. For example, level 1 corresponds to the condition (S11, S22 ON and S12, S21 OFF). Level -1 corresponds to (S11, S22 OFF and S12, S21 ON). Level 0 corresponds to (S11, S21 OFF and S12, S22 ON).

An H-bridge class-D amplifier with shoot-through current suppression was designed and implemented with 0.18-μm CMOS devices, as part of the Jazz BiCMOS technology [19]. The transistor sizes of the nMOS and pMOS at the switching stage were 1.6 and 4 mm, respectively. The pull-up/pull-down

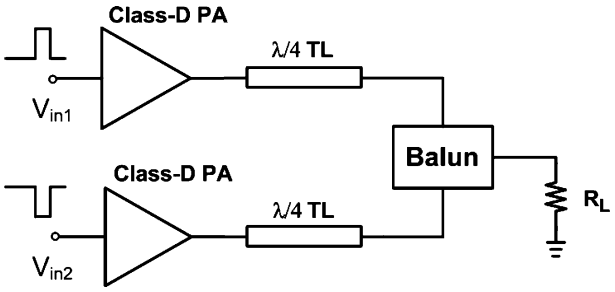

Fig. 10. Schematic of the H-bridge class-D PA.

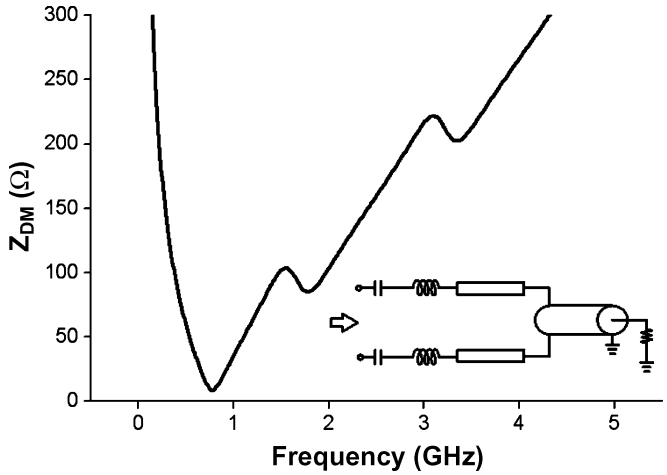

Fig. 11. Differential mode impedance $(Z_{\rm DM})$ of a coaxial balun in series with two resonators and transition lines as function of frequency. $Z_{\rm DM}$ is approximately 7 Ω at 800 MHz.

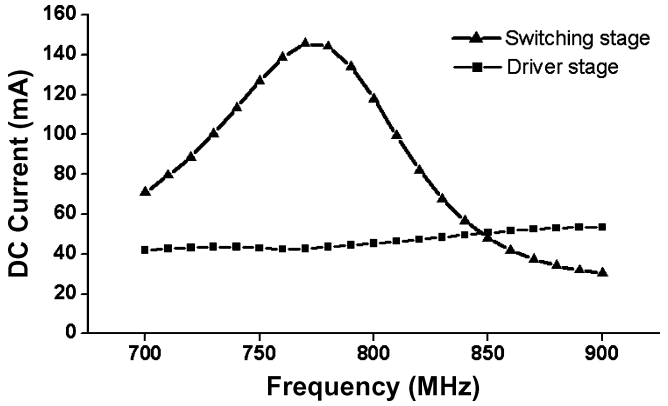

Fig. 12. Measured dc currents for switch and driver stage as a function of frequency.

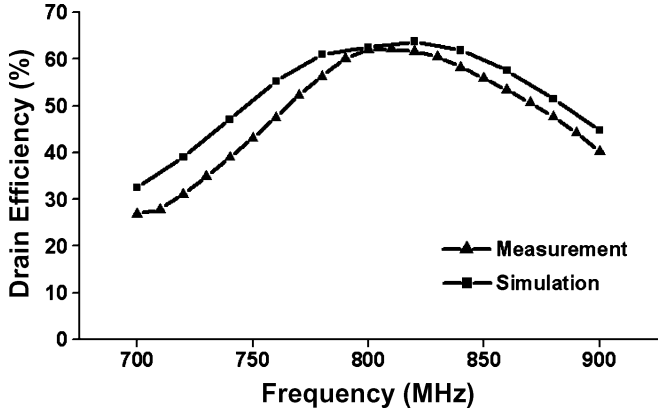

Fig. 13. Measured drain efficiency as a function of frequency.

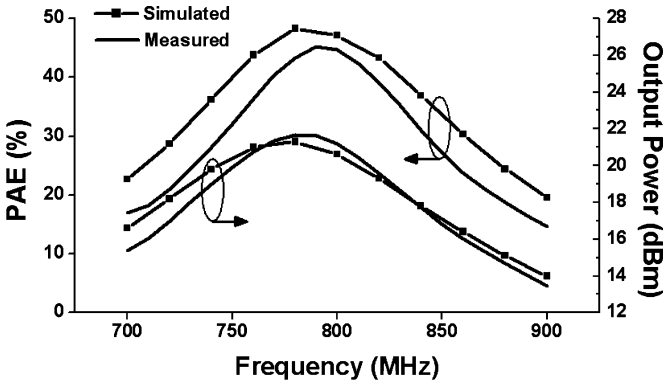

Fig. 14. Measured PAE and output power as a function of frequency.

device ratio of the drivers for nMOS and pMOS were 1:1 and 5:1, respectively. The drain power supply voltage was 2 V. Fig. 10 shows schematically the architecture of the overall of the H-bridge amplifier, which consists of two class-D amplifiers and a power combiner. The driving signals $V_{\rm in1}$ and $V_{\rm in2}$ were complementary for two-level DSM signals and independent of each other for three-level DSM signals. A quarter wavelength of coaxial line combined the output signals and two quarter-wavelength transmission lines implemented the impedance transformation. The simulated differential-mode impedance $(Z_{\rm DM})$ of the coaxial balun in series with the resonators is shown in Fig. 11. $Z_{\rm DM}$ of the output networks is high except for the desired signal frequency. Therefore, the out-of-band signals and quantization noise can be rejected. In this study, the coaxial balun and the matching networks were realized off-chip. Both balun and matching networks can be implemented in an integrated fashion by CMOS technology in future work.

IV. Amplifier Measurement Results

The drain efficiency and dc currents of the H-bridge class-D amplifier were measured with periodic driving signals. Fig. 12 shows that the maximum current occurs at the desired frequency (800 MHz) and drops significantly at out-of-band frequencies, as is expected from inclusion of the series resonators. Fig. 13 illustrates the drain efficiency as a function of frequency. Also shown is the efficiency simulated for the amplifier using Agilent ADS modeling of the transistors and matching components. The power-added efficiency (PAE) and output power are shown in Fig. 14. The peak drain efficiency, PAE, and output power were 62%, 45%, and 21 dBm, respectively. Here, the drain efficiency considers the switching stage power consumption only. The PAE quoted here considers the total dc power consumed by both the driver and switching stage (since the input power to the driver is negligible in an integrated CMOS system).

For characterization of the amplifier for CDMA applications, a CDMA-like QPSK signal with a 1.23-MHz symbol rate and a 5.5-dB peak-to-average ratio was up-sampled and fed to a

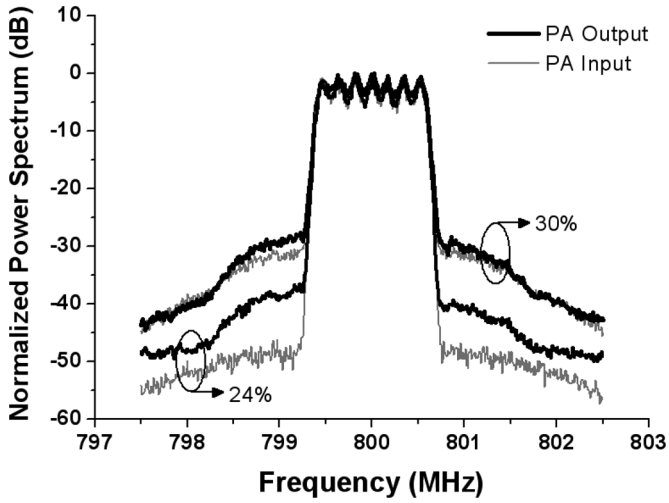

Fig. 15. Measured input and output spectrum for two-level DSM signals with in-band power ratios of 30% and 24%, respectively.

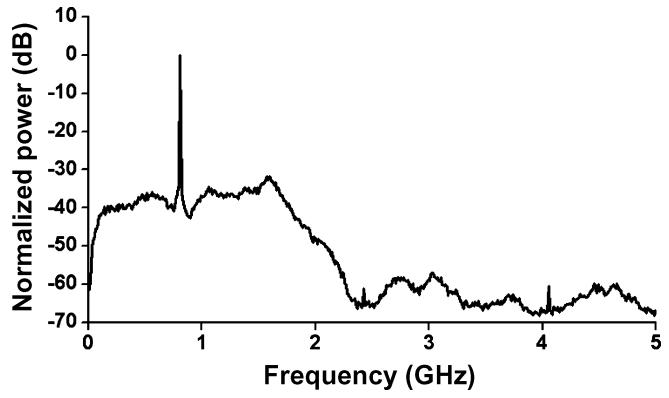

Fig. 16. Measured amplifier output spectrum with DSM signals.

BPDSM in MATLAB. The resulting modulated binary pattern with a length of 12 Mb was stored in an Agilent 81134A pulse pattern generator, which outputs two complementary binary signals with an amplitude of 2 V. These two complementary signals drove the two class-D PAs of the H-bridge amplifier. The input-signal ACPR was measured after combining the differential signals with a quarter-wave coaxial combiner. The drain efficiency and the ACPR of the PA were measured for CDMA signals with different in-band power ratios. For the DSM signals with an in-band power ratio of 24%, the amplifier obtained a drain efficiency of 26% with an ACPR of −49 dBc.

For DSM signals with an in-band power ratio of 30%, a drain efficiency of 31% was achieved with an ACPR of −43 dBc. The amplifier output spectra are shown in Fig. 15; both cases meet the CDMA IS-95 ACPR specification [20] of −42 dBc. Fig. 16 shows the output spectrum over a wide frequency range from 10 MHz to 5 GHz. The out-of-band signals were mainly rejected by the output resonator which has a loaded Q of 6. The residual out-of-band emissions will be further rejected by the duplexer used in front of the antenna. The production of spurious signals within the receive band of a CDMA transceiver remains a problem; however, it could possibly be addressed with an adaptive duplexer filter [21].

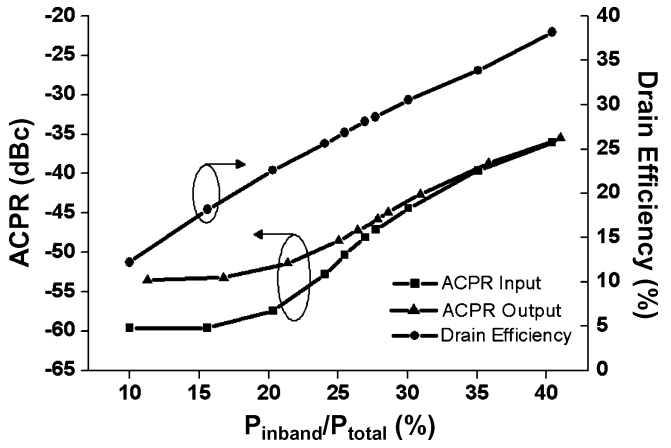

Fig. 17. Measured ACPR and drain efficiency of the CMOS H-bridge amplifier for two-level DSM signals with different in-band power ratios.

Fig. 17 displays the measured ACPR of the input and output of the PA and the drain efficiency. Higher efficiency could be obtained by increasing the encoded in-band power ratio, although the signal quality was degraded at the same time due to the characteristics of the DSM. This signal quality degradation limits the amplifier efficiency in digital RF transmitters.

It is noteworthy that, in order to provide power control as needed in CDMA transmitters, the in-band power can be varied over an appreciable range (>20 dB) during the generation of the DSM signal by varying the B/A ratio. To achieve the large power control range of >70 dB needed in many CDMA systems, however, and to optimize efficiency, it is expected that supply voltage ($V_{\rm dd}$) variation could be used (potentially together with selectable output attenuation at very low power).

The H-bridge amplifier was also measured with three-level DSM signals. Because each class-D amplifier can only differentiate two driving levels, the three-level DSM signals have to be decomposed into two channel signals $V_{\rm in1}$ and $V_{\rm in2}$, and each channel outputs two-level DSM signals, feeding to different branches of the H-bridge class-D amplifier separately. Both DSM data streams were generated in MATLAB and uploaded to the pulse pattern generator.

Fig. 18 shows a comparison of the amplifier efficiency using two- and three-level DSM signals. The system with a three-level DSM shows an efficiency enhancement from 31% to 33% for CDMA signals at an output power of 15 dBm. The ACPR was measured with three-level DSM signals, as shown in Fig. 19. The large ACPR degradation at the low-power region is believed to be related to effects such as imbalance between rise and fall times, mismatch between the two amplifiers, and nonideal common-mode impedance. These effects are less important for two-level DSM signals due to differential operation.

In order to gain insight into the power dissipation of the amplifier, Fig. 20 plots the dc power consumption of the H-bridge class-D PA as a function of the in-band power contained in the input two-level DSM waveforms. The figure shows that the output power linearly increases with the input in-band power. The power consumption at the switch stage gradually increases with the measured input in-band power while the power consumption at the driver stage stays almost constant. The overall

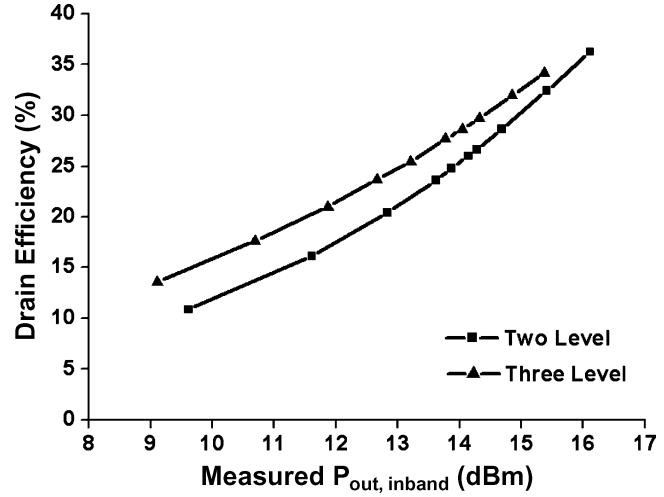

Fig. 18. Measured drain efficiency as function of output power for two- and three-level DSM signals.

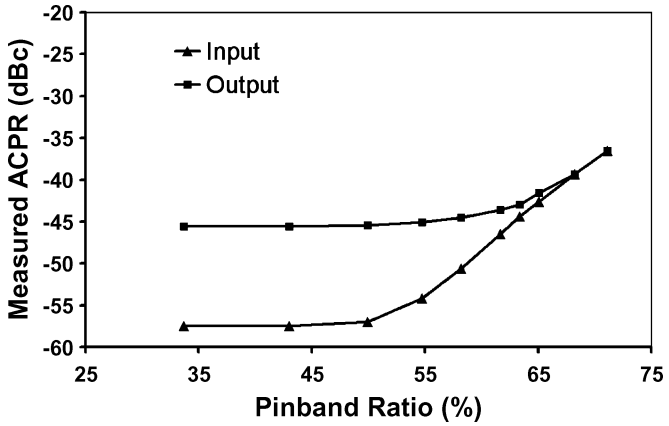

Fig. 19. Measured amplifier input and output ACPR as a function of output power for three-level DSM signals.

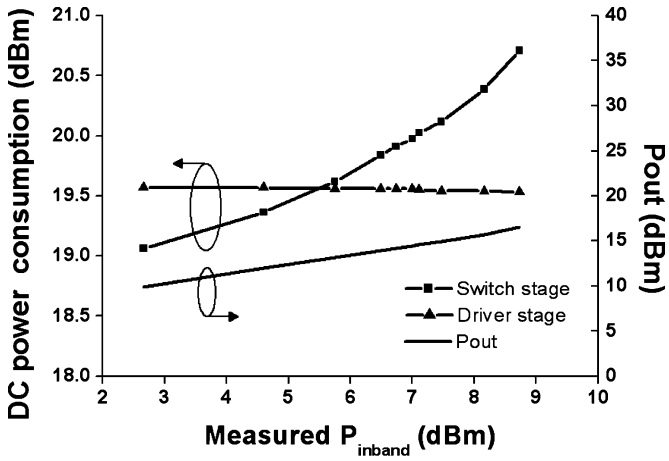

Fig. 20. Measured power consumption at switch and driver stage and output power as a function of output power.

power consumption increases because of switch stage loss contributions such as ON-state resistance $(R_{\rm on})$ loss which increases with output power. The ratio of different loss mechanisms at different output power levels is shown by the analysis in Section V.

V. Voltage-Mode Class-D Amplifier-Efficiency Analysis and Estimation

The efficiency of the voltage-mode class-D amplifier for DSM inputs is closely related to that for operation with conventional narrowband inputs. Because of the resonator load, the amplifier sees a high load impedance at harmonic and out-of-band frequencies with DSM inputs. Therefore, the class-D amplifier only delivers output current for the desired signals at the fundamental frequency. The amplifier is driven by signals with a duty ratio in general not equal to 50%, which sometimes requires reverse currents to flow through the switches. As long as the devices can provide the reverse current required in this condition, the amplifier efficiency is ideally independent of the output power. However, loss mechanisms such as the output capacitance loss remain almost constant for different output power levels, degrading the amplifier efficiency for lower output power.

Factors degrading the class-D amplifier efficiency—apart from shoot-through current loss—are considered next. These include the ON-state resistance $(R_{\rm on})$, overlap of current and voltage during switching transition, device output capacitance (C_p), and parasitic resistance of the resonator. First, we consider a single class-D amplifier driven by periodic signals.

A. Single Class-D Amplifier Driven by Periodic Signals With Non-50% Duty Ratio

Fig. 21 shows the time-domain voltage waveform V_2 of Fig. 8 as a function of θ defined as $2\pi f \cdot t$, where f is the output frequency. The voltage waveform V_2 differs from idealized case because of the ON-state resistance and nonzero transition time. $V_2(\theta)$ can be expressed as

$$V_2(\theta) = \begin{cases} \frac{\theta}{\tau} V_{\rm dd} - I \cdot R_{\rm on} \cdot \cos\theta, & -(D+\tau) \le \theta \le -D \\ V_{\rm dd} - I \cdot R_{\rm on} \cdot \cos\theta, & -D \le \theta \le D \\ V_{\rm dd}\left(1 - \frac{\theta - D}{\tau}\right) & \\ \quad -I \cdot R_{\rm on} \cdot \cos\theta, & D \le \theta \le D+\tau \\ -I \cdot R_{\rm on} \cdot \cos\theta, & (D+\tau) \le \theta \le 2\pi - D \end{cases} \tag{1}$$

where $V_{\rm dd}$ is the dc supply voltage, D defines the ON-time duty ratio in radians, τ is the ON–OFF transition time in radians (assumed to be symmetric), $R_{\rm on}$ is the ON-state resistance, and I is the amplitude of the output current $(I_{\rm load})$.

Due to the high-Q series resonator, the load voltage waveform is only the fundamental Fourier component of $V_2(\theta)$. By using Fourier analysis, the output voltage waveform $V_{\rm out}(\theta)$ can be written as

$$V_{\rm out}(\theta) = \left[\frac{4}{\pi} V_{dd} \cdot \sin(D) \frac{\sin\left(\frac{\tau}{2}\right)}{\tau} - I \cdot R_{\rm on}\right] \cos\theta. \tag{2}$$

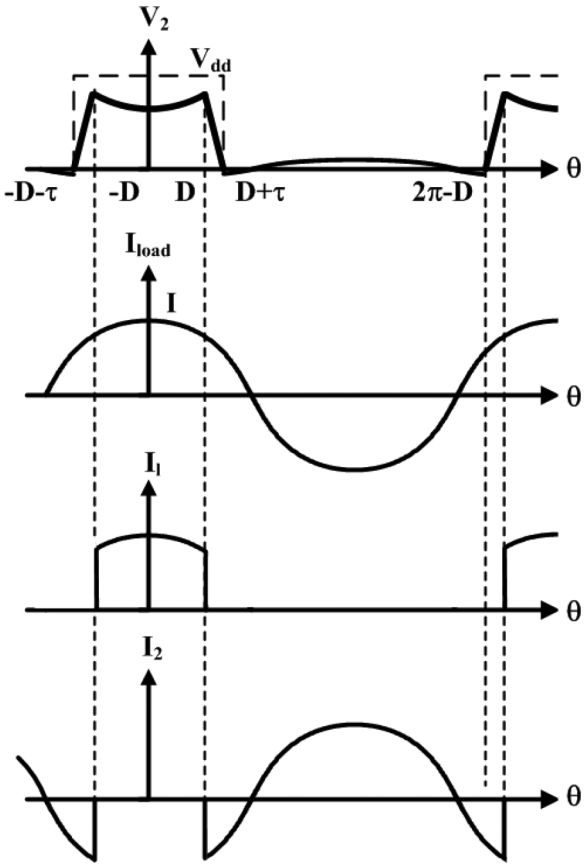

Fig. 21. Class-D amplifier voltage and current waveforms for efficiency estimation.

$I_{\rm load}$ is a function of the output voltage at the load, i.e.,

$$I_{\rm load}(\theta) = I\cos(\theta) = \frac{V_{\rm out}(\theta)}{R}. \tag{3}$$

Therefore, I can be written from (2) and (3) as

$$I = \frac{4}{\pi}\frac{V_{\rm dd}}{R+R_{\rm on}} \cdot \sin(D)\frac{\sin\left(\frac{\tau}{2}\right)}{\tau}. \tag{4}$$

From (4), the amplifier output power can be found to be

$$P_{\rm out} = \frac{1}{2}I^2R = \frac{8}{\pi^2}\frac{V_{\rm dd}^2}{R}\left(\frac{R}{R+R_{\rm on}}\right)^2 \cdot \sin^2(D)\frac{\sin^2\left(\frac{\tau}{2}\right)}{\tau^2}. \tag{5}$$

From (5), the amplifier output power decreases with increasing $R_{\rm on}$ and transition time. For the amplifier driven by 50% duty-ratio signals ($D = \pi/2$) with ideal turn-on resistance ($R_{\rm on} = 0$) and transition time ($\tau = 0$), the amplifier generates the maximum output power, and (5) can be simplified as

$$P_{\rm out} = \frac{2}{\pi^2}\frac{V_{\rm dd}^2}{R}. \tag{6}$$

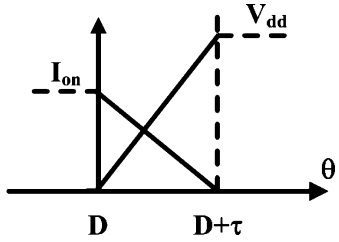

Fig. 22. Overlap voltage and current waveforms across the p-channel transistor during the transition.

To calculate the amplifier efficiency, the dc power consumption can be estimated by

$$P_{\rm dc} = P_{\rm out} + P_{R_{\rm on}} + P_{\rm overlap} + P_{\rm cap} \tag{7}$$

where $P_{\rm out}$ is the output power, $P_{R_{\rm on}}$ is the loss due to the ON-state resistance of the devices, $P_{\rm overlap}$ is the loss associated with transitions, and $P_{\rm cap}$ is the loss due to the output capacitance of the devices. For high-efficiency amplifiers, these contributions are additive to a close approximation.

The first two terms in (7), $P_{\rm out}$ and $P_{R_{\rm on}}$, can be obtained by deriving the dc term of the current I_1, which corresponds to the current flowing through the p-channel device assuming zero transition time and zero output capacitance. Total power for $P_{\rm out}$ and $P_{R_{\rm on}}$ can be written as

$$P_{\rm out} + P_{R_{\rm on}} = V_{\rm dd} \cdot \frac{1}{2\pi}\int_{-D}^{D} I \cdot \cos\theta d\theta = V_{\rm dd} \cdot I\sin D. \tag{8}$$

$P_{\rm overlap}$ comes from the overlap of voltage and current waveform across the device during the transition. The shoot-through current loss is minimized and ignored here. $I_{\rm on}$ is defined as the current level when the transition occurs. Fig. 22 shows the overlap voltage and current waveforms across the p-channel transistor during the transition. The loss associated with the overlap can be written as

$$P_{\rm overlap} = 2 \cdot \frac{1}{\pi}\int_{0}^{\tau} V_{\rm dd} \cdot I_{\rm on}\frac{\tau\theta - \theta^2}{\tau^2}d\theta = \frac{V_{\rm dd}}{3\pi} \cdot I_{\rm on} \cdot \tau \tag{9}$$

where $I_{\rm on} = I \cdot \cos D$.

The device output capacitance loss is $P_{\rm cap}$, which can be written as

$$P_{\rm cap} = C_p(V_{\rm dd} - I\cos D \cdot R_{\rm on})^2 \cdot f \tag{10}$$

where f is the output frequency. With the output power and the dc power from (4) and (6), the amplifier efficiency can be obtained as

$$\eta = \frac{P_{\rm out}}{P_{\rm dc}}. \tag{11}$$

TABLE I
CIRCUIT PARAMETERS USED IN THE ANALYTICAL RESULTS

Frequency	V_{dd}	C_p	τ	R_Q	R_{on}	P_{dB}	R
800MHz	2V	4.7 pF	0.1π	0.8 Ω	0.7 Ω	0.6dB	7 Ω

B. H-Bridge Class-D Amplifier Driven by Periodic Signals With Non-50% Duty Ratio

In (1)–(11), we considered a class-D amplifier and the loss associated with the transistor only. To expand the equations for an H-bridge amplifier with loss associated with passive components, issues such as nonideal Q of the inductor and the capacitor at the output and output combiner loss are considered.

The output power for an H-bridge amplifier can be written as

$$P_{\text{out}} = 2 \cdot \frac{8}{\pi^2} \frac{V_{\text{dd}}^2}{R} \left(\frac{R}{R + R_{\text{on}} + R_Q} \right)^2 \cdot \sin^2(D) \frac{\sin^2\left(\frac{\tau}{2}\right)}{\tau^2} \cdot 10^{\frac{-L_C}{10}} \tag{12}$$

where R_Q is the parasitic resistance due to the finite Q of the inductor and capacitor at the output and L_C is the combiner loss in dB. R in (12) is defined as the differential load impedance.

Considering the parasitic resistance R_Q at the output, the output current amplitude I can be expressed as

$$I = \frac{4}{\pi} \frac{V_{\text{dd}}}{R + R_{\text{on}} + R_Q} \cdot \sin(D) \frac{\sin\left(\frac{\tau}{2}\right)}{\tau}. \tag{13}$$

The total dc power consumption for the combined amplifier with the two class-D amplifier components is

$$P_{\text{dc}} = 2 \times (P_{\text{out}} + P_{R_{\text{on}}} + P_{\text{overlap}} + P_{\text{cap}}) \tag{14}$$

where $P_{\text{out}} + P_{R_{\text{on}}}$, P_{overlap}, and P_{cap} are the same as (8)–(10) except that I is replaced by (13). The efficiency can be obtained by dividing the output power (12) by total dc power consumption (14).

To validate the analytical equations above, the results were compared with simulations and measurements when the H-bridge class-D amplifier is driven by the periodic signals with different duty ratios. The transistor model used for simulation was obtained from the foundry [19]. The circuit parameters such as supply voltage, R_{on}, transition time, and output capacitance are shown in Table I. The transition time τ and the output capacitance C_p were estimated by using transient simulation. The effective output capacitance C_p includes both drain-to-source capacitance and drain-to-gate capacitance and coincides with the OFF-state capacitance defined in [15].

By applying the estimated circuit parameters to (12) and (14), the efficiency and output power for different duty ratios are obtained as shown in Figs. 23 and 24, respectively. Fig. 25 shows drain efficiency for different output power levels. The analytical and simulated results show good agreement with the measurements.

To analyze the loss associated with the transistors, each power loss factor, including $P_{R_{\text{on}}}$, P_{cap}, and P_{overlap}, can be calculated separately. First, the total power loss is defined as the difference between P_{out} in (5) and P_{dc} in (7). $P_{R_{\text{on}}}$ can be calculated by subtracting (8) from (5). P_{overlap} and P_{cap} can be obtained from (9) and (10), separately. Fig. 26 shows the contribution of each power loss component divided by total power loss, as a function of normalized P_{out} obtained with different duty ratios. The efficiency degradation is dominated by the capacitance loss

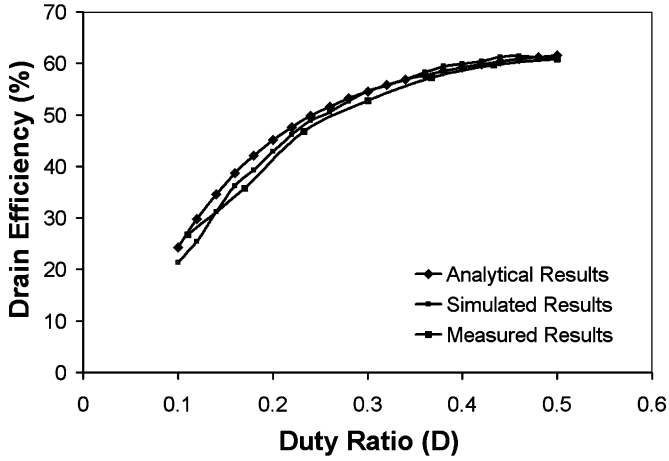

Fig. 23. Comparison of the drain efficiency as a function of duty ratio.

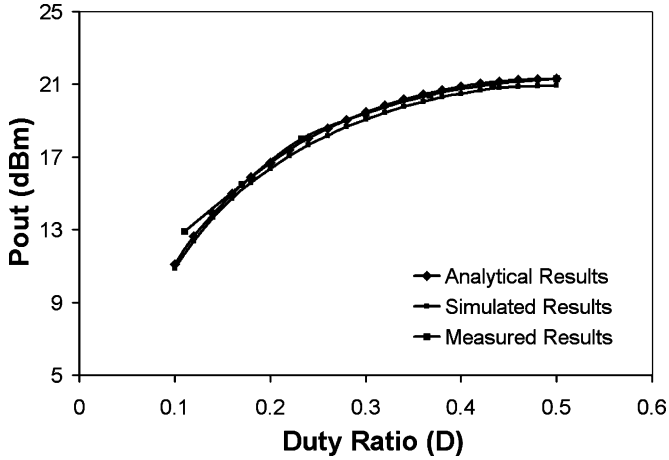

Fig. 24. Comparison of the output power as a function of duty ratio.

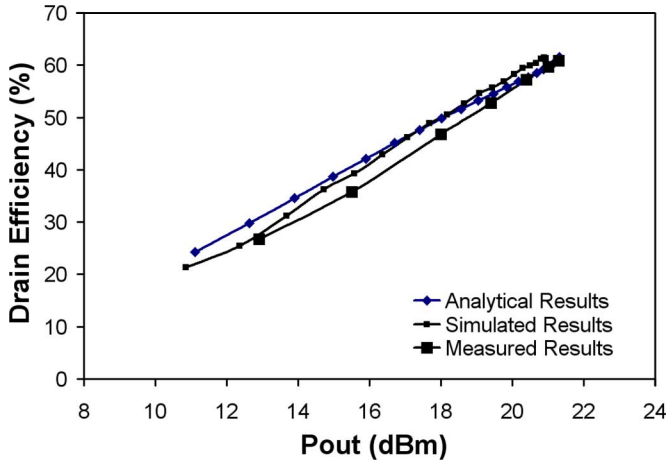

Fig. 25. Comparison of drain efficiency as a function of output power.

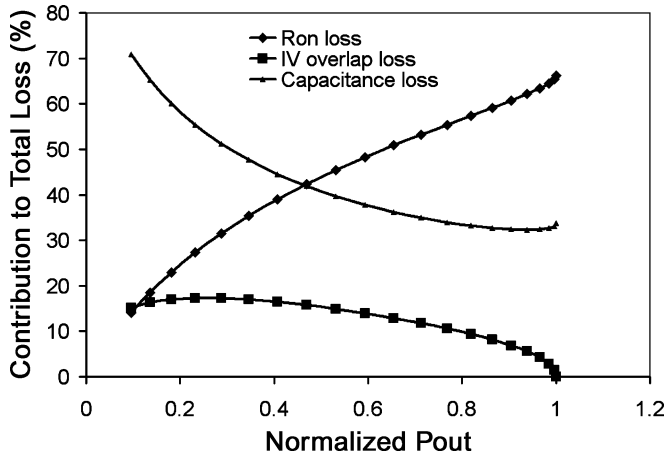

Fig. 26. Power loss ratio for each loss factor as a function of duty ratio.

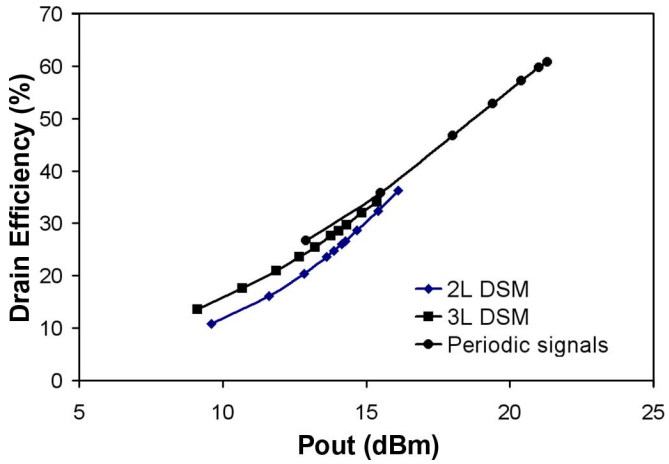

Fig. 27. Measured amplifier drain efficiency as a function of output power.

$(P_{\rm cap})$, which is independent of output power. The ratio of $P_{R_{\rm on}}$ over total power loss decreases with duty ratio due to the fact that smaller currents flow through the transistor at lower output power level.

C. H-Bridge Class-D Amplifier Driven by DSM Signals

Fig. 27 shows the measured amplifier efficiency as function of output power for two-level DSM signals, three-level DSM signals, and periodic signals with different duty ratios. The results show that the efficiency of the amplifier driven by the DSM signals is close to that for the amplifier driven by non-50% duty-ratio signals with the same output power. To further justify this result, possible loss mechanisms differentiating the two situations are discussed below.

1) Output Capacitance Loss: Fig. 26 indicates that the output capacitance loss dominates the efficiency degradation in the low output power region. The capacitance loss depends on the average number of transitions per cycle, assuming the voltage drop due to ON-state resistance can be ignored due to the low current flowing through the transistors. Periodic signals have two transitions per cycle. For the generated DSM signals (when the streams are longer than 1 Mb avoid statistical fluctuations), the average number of transitions per cycle is also very close to

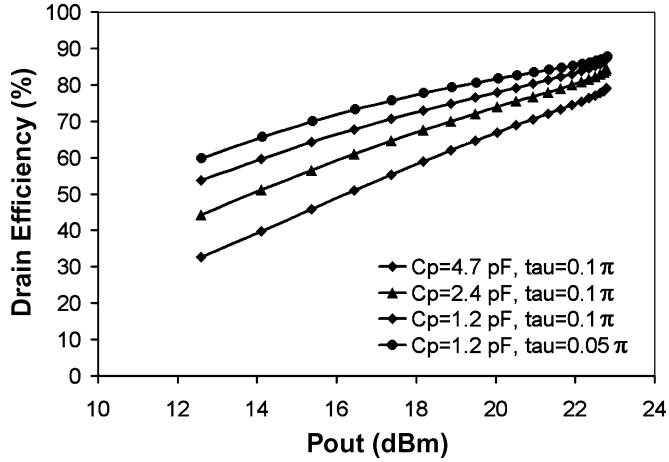

Fig. 28. Estimated drain efficiency as a function of output power with reduced capacitance and transition time. (Based on $f = 800$ MHz, $R_{\rm on} = 0.7\ \Omega$, $R = 7\ \Omega$, $V_{\rm dd} = 2$ V, and no output circuit loss.)

two, which leads to the same capacitance loss as for the periodic driving condition.

2) Loss Associated With Out-of-Band Signals: For the same desired output power, the amplifier driven by DSM signals consumes additional dc power due to generation of nonrecycled out-of-band signals compared with the amplifier driven by periodic signals. The loaded Q of the output resonator determines the out-of-band signal rejection. A higher loaded Q can reduce the undesired power consumption due to the out-of-band signals. The choice of Q for the resonator is dependent on the bandwidth desired as well as by the signal and technology constraints. For the measured H-bridge amplifier, the output resonator has a loaded Q of 6, which leads to only a small difference $(< 0.02\eta)$ between the efficiency η of the DSM and the periodic case.

3) Overlap Loss: The loss due to current and voltage overlap during the transition is a function of the amplitude of the currents when the transition occurs. For periodic signals, the current amplitude $(I_{\rm on})$ is given in (9), which only depends on duty ratio (D) and the amplitude of the load current (I); for a given output power, $I_{\rm on}$ is a constant. However, for DSM signals, the possible current levels at the switching instants depend on the phase difference between the switched voltage waveform V_2 and the load current $I_{\rm load}$. In general, the overlap loss will be different for these different cases. For amplifiers with a short transition time, however, the average overlap loss is expected to be close to that of the periodic signals.

If the differences highlighted in the preceding paragraphs are neglected, the efficiency of the voltage-mode class-D amplifier for DSM inputs is similar to that for operation with conventional narrowband inputs. This provides a simple way to estimate the amplifier efficiency with DSM signal driving signals.

In addition to minimizing the loss associated with the passive components, active device improvements can also improve amplifier efficiency. Transistors based on silicon-on-insulator (SOI) technology can reduce the capacitance loss. Shorter gate-length transistors with a stacked-transistor technique [22] can potentially reduce the transition time, thus lowering the overlap loss. The potential efficiency enhancement from these steps can

be estimated by using the analytical equations (12) and (14). Fig. 28 shows the drain efficiency as a function of output power for different values of output capacitance and delay. At an output power of 15 dBm, amplifier efficiency can be improved from 42% to 63% by reducing the capacitance from 4.7 to 1.2 pF. By further reducing the transition time for 0.1π (62.5 ps) to 0.05π (31.25 ps), the amplifier efficiency can be improved to 70%. The results demonstrate the potential benefit of implementing the class-D DSM amplifier with advanced technology.

VI. Conclusion

An H-bridge class-D amplifier for DSM CDMA signals was demonstrated at 800 MHz. The amplifier efficiency improved for DSM signals with higher encoded in-band power ratio. A drain efficiency of 31% was achieved with an ACPR of −43 dBc for two-level DSM signals, with an in-band power ratio of 30%. An improved drain efficiency of 33% was achieved with an ACPR of −43 dBc for three-level DSM signals. The efficiency analysis shows the contribution of different loss mechanisms as a function of output power. By reducing the capacitance associated with the transistors, the amplifier efficiency can be improved significantly, especially in the low-power region. The results demonstrate the feasibility and potential of using the H-bridge class-D amplifier in digital RF transmitters.

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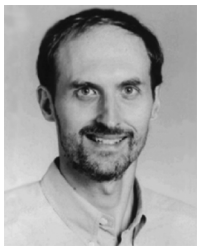

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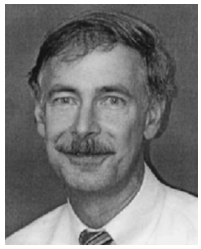

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