CMOS Outphasing Class-D Amplifier With Chireix Combiner

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***Abstract*—This letter presents a CMOS outphasing Class-D power amplifier (PA) with a Chireix combiner. Two voltage-mode Class-D amplifiers used in the outphasing system were designed and implemented with a 0.18-μm CMOS process. By applying the Chireix combiner technique, drain efficiency of the outphasing PA for CDMA signals was improved from 38.6% to 48% while output power was increased from 14.5 to 15.4 dBm with an adjacent channel power ratio of −45 dBc.**

***Index Terms*—Chireix combiners, CMOS amplifiers, outphasing amplifiers.**

I. Introduction

With the increasing demands on power amplifier (PA) efficiency and linearity in modern wireless communication systems, outphasing architectures have drawn increasing attention because of their ability to achieve linear amplification along with potentially high efficiency by applying nonlinear amplifiers [1], [3]–[6]. In 1935, Chireix proposed a reactively compensated combiner technique to further improve the outphasing system efficiency in the power back-off region via a load-pulling effect [2]. However, the reactively compensated combiner is not suitable for some switching PAs such as Class-E amplifiers which achieve high efficiency only for load impedance with a specific phase [3].

In this letter, an outphasing amplifier was demonstrated using two Class-D amplifiers with the Chireix combining technique. A drain efficiency of 48% was achieved for CDMA signals, with an output power of 15.4 dBm and an adjacent channel power ratio (ACPR) of −45 dBc. This corresponds to a relative improvement of 24% compared to the PA without reactive compensation. The proposed outphasing class-D amplifier can be driven by digital signals directly, thus it is suitable for all-digital radio frequency (RF) transmitters.

II. Outphasing Amplifier Design

An outphasing system consists of a signal component separator (SCS), two nonlinear PAs, and a conjugate reactively loaded combiner, as shown in Fig. 1. The SCS converts non-constant envelope signals $S_{\rm in}(t)$ to two constant envelope signals $S_1(t)$ and $S_2(t)$, which drive highly efficient nonlinear PAs, whose outputs are summed. After power combining, the desired amplitude and phase information can be recovered without distortion. This approach is also called Linear Amplification with Nonlinear Component (LINC).

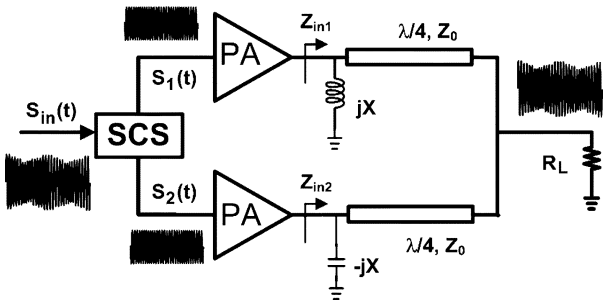

Fig. 1. Simplified block diagram of an outphasing system with a Chireix combiner. The compensation reactances are complex conjugate ($\pm$jX).

The nonlinear amplifiers can be implemented by switching amplifiers to increase system efficiency without degrading the linearity, thanks to the constant envelope driving signals. Two voltage-mode Class-D amplifiers were employed in this work, as discussed in the following.

A. Voltage-Mode Class-D PA

A voltage-mode Class-D amplifier consists of two active devices and a series resonator. If the two devices are switched alternately, a voltage-mode class-D amplifier can be approximated as a voltage source. Therefore, voltage-mode class-D amplifiers can maintain high efficiency even while the phase of the load impedance varies. This makes them promising candidates for Chireix power combining.

During the ON/OFF transition of the active devices, there is a short period of time when both PMOS and NMOS are ON, resulting in a short-circuit between the power supply and ground. A large current spike (known as shoot-through current) may occur, which causes significant energy loss. To minimize this loss, the PMOS and NMOS devices have different driving circuits, as shown in Fig. 2. By modifying the pull-up and pull-down device size ratio of the drivers, the overlap of the turn ON time between the PMOS and the NMOS during the transition can be minimized.

Two voltage-mode Class-D amplifiers, configured for outphasing operation, with shoot-through current suppression were designed and implemented with in a 0.18-μm SiGe BiCMOS technology [7]. The transistor sizes of the NMOS and PMOS of the output stages were 1.6 and 4 mm. The pull-up/pull-down device size of the drivers for NMOS and

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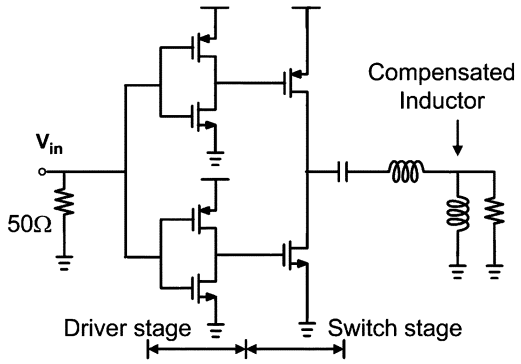

Fig. 2. Schematic of the voltage-mode Class-D PA with shoot-through current suppression and a compensated inductor.

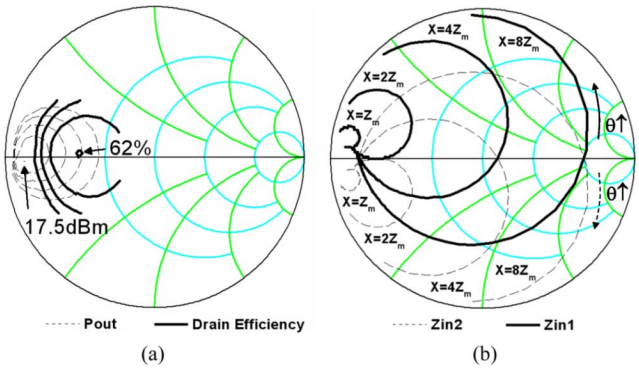

Fig. 3. (a) Simulated efficiency and output power load-pull contours. Max efficiency of 62% and maximum output power of 17.5 dBm were obtained at the peaks, respectively. (b) Simulated Input impedance Z_{in1} and Z_{in2} of the Chireix combiner as the outphasing angle θ is varied.

PMOS were 0.2 mm/0.2 mm and 1 mm/0.2 mm, respectively. The PAs were biased at 1.8 V. An inductor was added at both amplifier outputs, as shown in Fig. 2, to compensate the device output capacitance such that maximum output power and efficiency were achieved with purely real load impedance, resulting in symmetric load-pull contours with respect to the resistance-axis. The 50-Ω resistor at the input was for impedance matching which can be replaced by smaller driver stages as the PA is integrated in digital circuit systems. The simulated drain efficiency and output power contours of each amplifier as a function of load impedance are shown in Fig. 3(a). The corresponding peak drain efficiency and peak output power were 62% and 17.5 dBm, respectively.

B. Chireix Combiner

The Chireix combiner allows the PAs to obtain high power combining efficiency under non-in-phase driving conditions via reactive compensation [2]. This highly efficient power combining occurs at the outphasing angles where the corresponding input impedance of the Chireix combiner Z_{in1} and Z_{in2} are equal and real, because the output signals of two PAs are in-phase after the combiner.

Fig. 3(b) shows the trajectories of the input impedance Z_{in1} and Z_{in2} of the Chireix combiner as the outphasing angle, θ, changes from 0° to 89° for different compensation reactance, X, as defined in Fig. 1. When $X = 2Z_m$, there is one solution

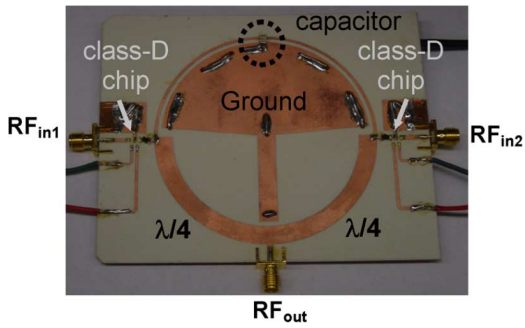

Fig. 4. Photograph of the CMOS outphasing Class-D PA with the Chireix combiner realized by a half wave length transmission line.

(outphasing angle) such that Z_{in1} and Z_{in2} are equal and real, where $Z_m = Z_0^2/2R_L$, Z_0 is the characteristic impedance of the quarter-wave transmission line and R_L is the load impedance. When $X > 2Z_m$, there are two solutions for which Z_{in1} and Z_{in2} are equal and real. With increasing X, one of the impedance solutions moves toward higher resistance. This increase in load resistance can produce a higher efficiency. However, the efficiency improvement is limited by the fact that the optimum efficiency occurs in the low-impedance region, as shown in Fig. 3(a). For $X < 2Z_m$, PA combining efficiency is limited by the fact that the output of both branches are never combining in-phase. Therefore, the reactive compensation X was chosen to be between $2Z_m$ to $4Z_m$ in order to demonstrate the efficiency improvement in the low-power region.

Fig. 4 displays the outphasing class-D amplifier with the Chireix combiner. The Chireix power combiner was realized by a $\lambda/2$ microstrip line with characteristic impedance of 75 Ω. A sliding capacitor shorting the $\lambda/2$ line to ground provides different reactive compensation to the amplifiers depending on the capacitor position [4]. When the capacitor is slid along the line, the impedances of the two compensation components change but still maintain a complex conjugate relationship, as required for the Chireix combiner.

III. Outphasing Amplifier Measurement Results

The CMOS Class-D outphasing amplifier was measured at 800 MHz without reactive compensation. The measured power and efficiency are shown in Fig. 5. A maximum drain efficiency of 61% was achieved with an output power of 20 dBm and the peak power added efficiency (PAE) was 42%, in good agreement with the simulations. The input driving power while having the 50 Ω impedance matching resistors is considerable. However, by embedding the PAs within digital circuit systems, this driving power consumption can be minimized further. Here, the drain efficiency includes only the switching stage power consumption, while the PAE includes the total dc power consumed by both driver and switching stage.

The measured normalized output power with different outphasing angles θ is shown in Fig. 6. Under the in-phase driving condition ($\theta = 0°$), the PA generates maximum output power; as θ is varied, the power closely follows $\cos^2\theta$, as expected.

The outphasing amplifier was measured for reactive compensation with $X = 4Z_m$, $2Z_m$, and Z_m, respectively, as shown in Fig. 7. With the reactive compensation $X = 2Z_m$, a drain

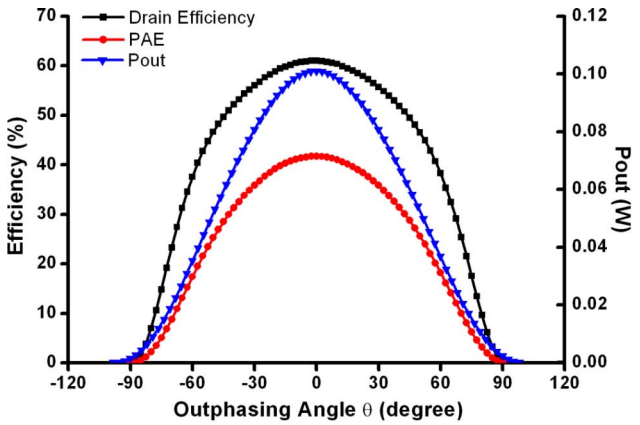

Fig. 5. Efficiency and output power measured with different outphasing angles. Maximum drain eficiency of 62% was achieved, together with a PAE of 42%.

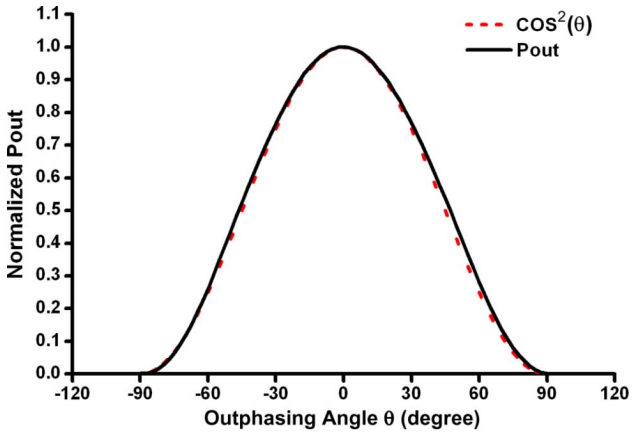

Fig. 6. Normalized measured output power versus outphasing angle θ. A $\cos^2\theta$ curve is shown for comparison.

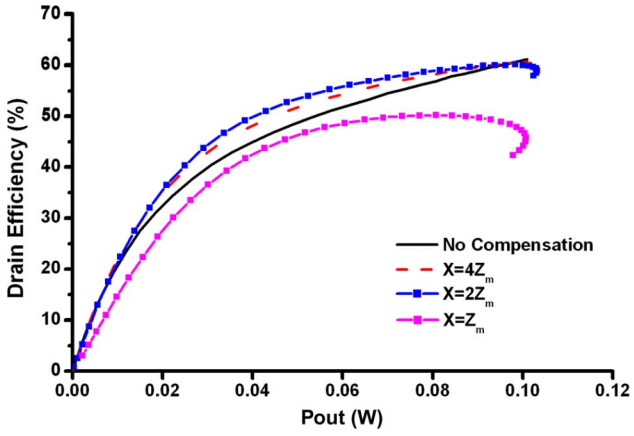

Fig. 7. Drain efficiency measured as a function of output power with different reactive compensations.

efficiency of 46% was achieved at 5 dB power back-off, although the PAE drops to 22% due to the output-power-independent power consumption of the driver stage.

The outphasing class-D PA was also measured with CDMA IS-95 signals which has a peak to average ratio (PAR) of 5.5 dB. The SCS was implemented in Agilent ADS to generate the out-

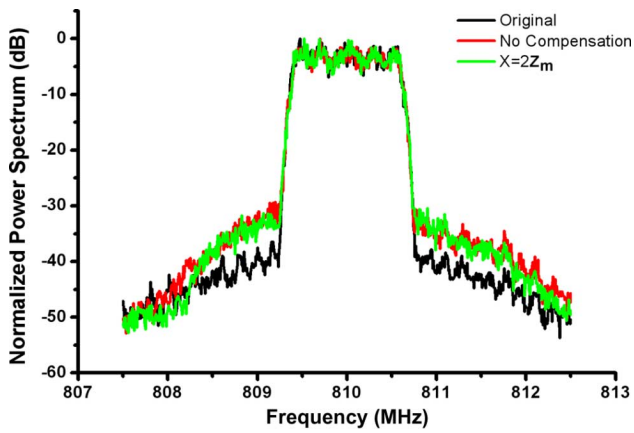

Fig. 8. Measured PA output spectrum with CDMA signals. An ACPR of −45 dBc was achieved.

phasing signals which were uploaded to two vector signal generators with synchronized RF and IQ patterns. By using the Chireix compensation technique, the drain efficiency was improved from 38.6% to 48% (an increase by a factor of 1.24) while output power was increased from to 14.5 to 15.4 dBm. Fig. 8 shows the measured amplifier output spectrum compared to the input signals. A measured ACPR of −45 dBc was also obtained with output power of 15.4 dBm without any predistortion.

The output power and efficiency of this amplifier approach can be expected to further improve with the application of stacked transistor technology [8], as well as reduced gate lengths.

IV. Conclusion

A CMOS outphasing Class-D PA with Chireix combiner was demonstrated. With the Chireix compensation technique, a drain efficiency of 48% was achieved (which represents an improvement factor of 1.24 compared to the PA without compensation). Without any predistortion, an ACPR of −45 dBc was achieved. The outphasing PA is an attractive candidate for use in all-digital transmitters.

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