Hardware Considerations for Spectral Encoded UWB Transmitters

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***Abstract*— Hardware considerations and system parameter tradeoffs are examined for the implementation of a real-time Spectral Encoded Ultra-Wideband transmitter. The effects of symbol length, chirp bandwidth, and spreading sequence are described, and two possible implementations are examined for their spectral shaping performance, cost, and power dissipation. One implementation is based on Surface Acoustic Wave chirp filters to perform the Fourier Transforms in real-time. The other is based on a high speed memory and digital-to-analog converter.**

I. Introduction

An ultra-wideband (UWB) signal, as defined by the FCC, possesses either a fractional bandwidth of greater than 20%, or a 10dB bandwidth of greater than 500MHz; UWB systems are allowed to operate in the frequency spectrum from 3.1-10.6GHz, and are limited to a power spectral density of -41.25dBm/MHz [1]. These systems are intended to overlay existing narrowband systems, such as the 802.11a wireless LANs, cordless telephones operating in the UNII bands at 5.2GHz and 5.8GHz, as well as WiMAX systems.

Several modulation techniques for UWB have been reported, such as pulse-position modulation (PPM) [2], direct sequence spread spectrum (DSSS) [3], and orthogonal frequency division multiplexing (OFDM) [4].

One method to reduce the effect of narrowband interference (NBI) on UWB receivers is to implement notch filtering to reject energy in the NBI frequencies. Since the power within the NBI frequencies will be removed, it follows that at the transmitter, the UWB signal should be spectrally shaped with a notch at the NBI frequencies. Doing so can reduce the interference from UWB transmitters to NBI systems.

Several techniques for spectral shaping UWB signals away from NBI bands have been proposed. For PPM systems, spectral shaping can be performed either by coding algorithms such as LABI [5], or designing time hopping sequences with the desired spectral shape [6]. Also, PPM systems can use pulses such as the duo-binary pulse [7] or the Manchester monopulse [8] to further enhance the spectral characteristics of the signal. In addition, pulse shapers that meet the FCC spectral mask have been reported [9-10].

In this paper, we focus on the hardware implementation of another spectral shaping method: Spectral Encoded UWB [11]. Its chief advantage is its ability to be used both at the transmitter for spectral shaping, and at the receiver for interference rejection. Specifically, we will examine a real-time implementation designed to operate in the 3-5GHz band, which is roughly the same frequency range as Mode 1 UWB devices from the MB-OFDM group [4].

This paper is organized as follows: Section II describes the real-time Spectral Encoding algorithm. Section III will discuss two hardware implementations and the choices on system parameters. Conclusions will be given in Section IV.

II. Real-time Spectral Encoded System

A. Spectral Encoding

Spectral Encoding can be considered a frequency domain counterpart to DSSS. This technique multiplies the input signal in the frequency domain by a spreading sequence [12], as shown in Fig. 1. The resulting signal is spread in *time* (Fig. 1(d)). Similar to DSSS, multiple access is achieved by assigning different spreading sequences to different users.

The Spectral Encoding technique can be extended to achieve spectral shaping to combat NBI [11]. As shown in Fig. 1(c), a Spectral Encoded system can achieve NBI suppression by nulling some of the spreading chips. The resulting signal is still spread in time, but has a spectral null at the NBI frequencies. At the receiver, the de-spreading operation is performed by multiplying the received signal with

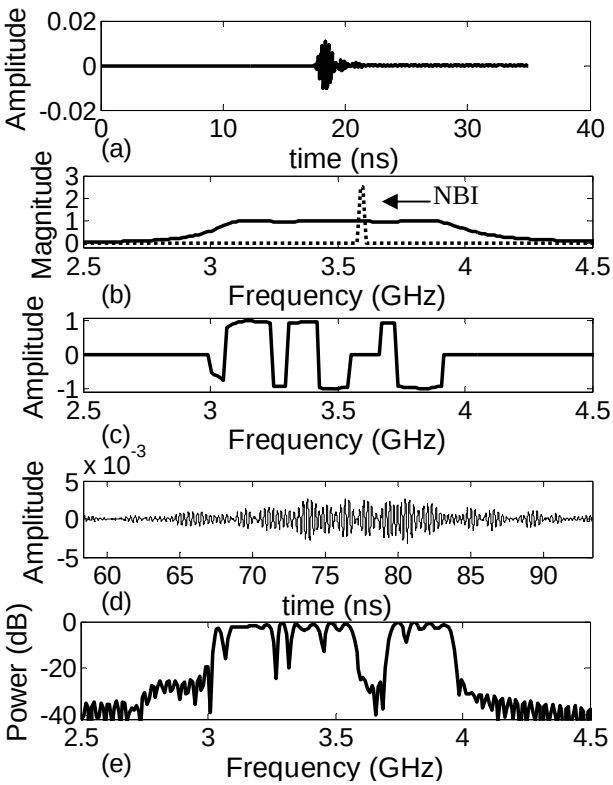

Fig. 1. Spectral Encoding process and interference suppression. (a) Input signal in the time domain. (b) Magnitude of the signal spectrum with a narrowband interferer. (c) Spectral Encoded Spectrum after multiplication with a spreading sequence. Here, the interference is notched out. (d) Spectral Encoded signal in the time domain (time-spread), with (e) the associated power spectrum.

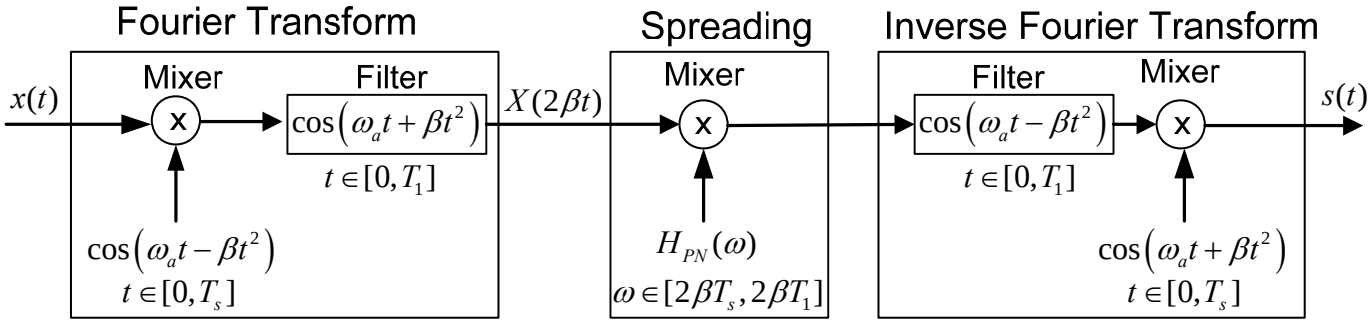

Fig. 2. Block diagram of the real-time Spectral Encoded UWB system.

the complex conjugate of the transmitter's spreading sequence, which notches out the NBI. Hence, a main advantage is that it inherently provides interference mitigation at the transmitter and interference rejection at the receiver. UWB systems based on DSSS or PPM may need other forms of spectral shaping, such as notch filters or those described in [5-10].

B. Real-Time Implementation Overview

The block diagram of a real-time implementation of the Spectral Encoded UWB transmitter is shown in Fig. 2. It is composed of three components: a Fourier Transform (FT) stage, a spreading stage, and an Inverse Fourier Transform (IFT) stage. The FT and IFT stages are implemented using chirp transforms [13]. Specifically the FT stage corresponds to multiplication and convolution of the input signal by chirp (linear FM) signals. The chirp signals can be generated using either SAW filters [11,13,14], or tap-delay line filters [13].

Consider a single symbol $x_{sym}(t)$ of length T for $t \in [-T/2, T/2]$, where $T < T_s$ and T_s is the transmitted symbol duration. The input signal $x(t)$ is defined as

$$x(t) = x_{sym}(t - T_s/2) \tag{1}$$

and is valid for $t \in [0, T_s]$. From Fig. 2, the chirp transform is performed by multiplying $x(t)$ by the chirp signal $\cos(\omega_a t + \beta t^2)$ and convolving the result with a filter whose impulse response is $\cos(\omega_a t + \beta t^2)$ for $t \in [0, T_1]$ where T_1 is the length of the filter. The output of the FT block can be written as

$$\begin{aligned} X(2\beta t) = X(\omega) &= \\ &= \int_0^{T_s} x(\tau)\cos\left(\omega_a \tau - \beta\tau^2\right)\cos\left(\omega_a (t-\tau) + \beta(t-\tau)^2\right) d\tau \\ &= X_R(2\beta t)\cos\left(\omega_a t + \beta t^2\right) - X_I(2\beta t)\sin\left(\omega_a t + \beta t^2\right) \end{aligned} \tag{2}$$

where β and ω_a are the half slope and the starting frequency of the chirp, $X_R(2\beta t)$ and $X_I(2\beta t)$ are the real and imaginary parts of the FT, so $X(2\beta t)$ is the time domain representation of the FT of $x(t)$ where the frequency evolves as $\omega = 2\beta t$. $X_R(\omega)$ and $X_I(\omega)$ are the real and imaginary portions of the FT given by

$$X_R(\omega) = \int_0^T x(\tau)\cos(\omega\tau)d\tau\,, \tag{3}$$

$$X_I(\omega) = \int_0^T x(\tau)\sin(\omega\tau)d\tau\,. \tag{4}$$

$X(\omega)$ is valid only during the time $x(t)$ is fully contained in the chirp filter corresponding to the time interval $t \in [T_s, T_1]$. Therefore the frequencies for which the FT is valid are $\omega = [2\beta T_s, 2\beta T_1]$. β and T_1 must be chosen such that $2\beta T_s = \omega_L$ and $2\beta T_1 = \omega_U$, where ω_L and ω_U are the lower and upper frequencies of the desired FT. Possible values could be 3.1-5GHz, or 3.1-10.6GHz for the entire UWB frequency range.

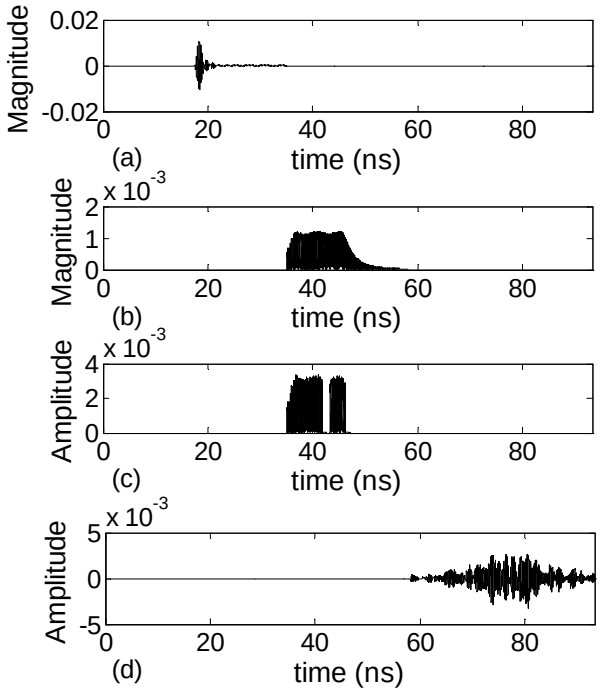

Fig. 3. Operation of the Real-Time Spectral Encoded System, where the signals shown are: (a) the input signal centered about $T_s/2$, (b) the Fourier Transform, (c) after multiplying by the spreading sequence H_{PN}, and (d) the transmitted signal $s(t)$. T_s = 35ns, T_1 = 58.33ns.

Since $X(\omega)$ is only valid in the interval $\omega = [2\beta T_s, 2\beta T_1]$, it is windowed to this interval. Then, it is multiplied by $H_{PN}(\omega)$, which is given by

$$H_{PN}(\omega) = \frac{8\beta}{\pi}[PN_R(\omega)\cos(\omega T_1) + PN_I(\omega)\sin(\omega T_1)] \tag{5}$$

where $PN(\omega) = PN_R(\omega) + jPN_I(\omega)$ is the spreading sequence in the interval $\omega = [2\beta T_s, 2\beta T_1]$, where $PN_R(\omega)$ and $PN_I(\omega)$ consist of a sequence of chips with amplitude ±1 (or zeros for notching).

After the spreading operation, the resulting signal is passed through the IFT block. It can be shown that the final encoded signal $s(t)$ is given by

$$s(t) = \int_{\omega_L}^{\omega_U} X_R(\omega)PN_R(\omega)\cos(\omega(t-T_1)) - X_I(\omega)PN_I(\omega)\sin(\omega(t-T_1))d\omega \quad (6)$$

where in (6), $\omega = 2\beta\tau$. Recall that the FT is only valid during the interval that the signal is fully contained in the convolution filter. Using similar arguments, $s(t)$ is only valid within the interval $t \in [T_1, T_1 + T_s]$, and must be truncated in time to this interval. Hence, the resulting symbol length is T_s. The $\cos(\omega T_1)$ and $\sin(\omega T_1)$ in (5) are used to shift the origin of the IFT output symbol from t=0 to t=T_1 [13], and is done to ensure the valid IFT falls in the interval $t \in [T_1, T_1 + T_s]$. Fig. 3 shows the operation of this algorithm in the time domain, and the associated time delays through the FT and IFT blocks.

III. Hardware Considerations

A. SAW based Implementation

In this section, a SAW filter implementation of the chirp transform will be considered. The choice of systems parameters will be described and the power in the desired notch will be used as a metric for system optimization.

From the previous section, there are three parameters – β, T_s, T_1 – with two equations relating them: $2\beta T_s = \omega_L$ and $2\beta T_1 = \omega_U$. First, the required SAW chirp filter length is related to T_s by

$$T_1 = T_s\omega_U / \omega_L. \quad (7)$$

Since long delay SAW filters are both challenging to realize and are costly to fabricate when the time-bandwidth product grows [15], smaller values of T_1 (and equivalently T_s) are desired.

In the previous section, two signal truncations occur, both of which may affect the performance: one after the FT stage and the other after IFT stage. If the input signal $x(t)$ is a bandpass signal in the frequencies $\omega = [2\beta T_s, 2\beta T_1]$, then the effect of windowing after the FT stage can be neglected [11]. However, the effect from windowing the IFT output can not be ignored. If the spreading sequence of length K is defined as

$$PN(\omega) = \sum_{i=1}^{K} S_{chip}^{i}(\omega) \quad (8)$$

where $S_{chip}^{i}(\omega)$ is the ith chip in the spreading sequence defined as

$$S_{chip}^{i}(\omega) = a_i \Pi_{W_{chip,i}/2}(\omega - \omega_{i,chip}), \quad (9)$$

where a_i is ±1 (or zero), $\omega_{U,chip,i}$ and $\omega_{L,chip,i}$ are the upper and lower frequency bounds of the chip, $W_{chip,i} = (\omega_{U,chip,i} - \omega_{L,chip,i})$ is the bandwidth, and $\omega_{i,chip} = (\omega_{U,chip,i} + \omega_{L,chip,i})/2$ is the center frequency. $\Pi_a(x)$ is the rectangular function defined as

$$\Pi_a(x) = \begin{cases} 1 & |x| \le a \\ 0 & otherwise \end{cases}. \quad (10)$$

Because the spreading operation multiplies $X(\omega)$ by the spreading sequence, a true IFT of this product is a convolution of $x(t)$ by the IFT of (5) using (8) as the PN sequence, which is the ideal Spectral Encoded signal $s_{ideal}(t)$, and is given by

$$s_{ideal}(t) = IFT\{X(\omega)H_{PN}(\omega)\} = x(t) * \sum_{i=1}^{K} \frac{\sin(W_{chip,i}(t-T_1)/2)}{\pi W_{chip,i}(t-T_1)/2} e^{-j\omega_{i,chip}(t-T_1)} \quad (11)$$

where * is the convolution operation, and the Fourier Transform pair $\sin(at)/\pi a \Leftrightarrow \Pi_a(\omega)$ is used. Note that $s_{ideal}(t)$ has infinite duration, while in the real-time implementation $s(t)$ is truncated to a window of length T_s. Hence, $s(t)$ is a truncated version of $s_{ideal}(t)$ in the interval $t \in [T_1, T_1 + T_s]$, and T_s needs to be chosen such that it contains most of the spread-time energy to minimize the effects of windowing on the IFT output.

Applying a rectangular window of length T_s to $s_{ideal}(t)$ causes the desired spectrum $X(\omega)H_{PN}(\omega)$ to be convolved with a *sinc* function. The window and its FT can be written as

$$\Pi_{T_s/2}(t - T_1 + T_s/2) \Leftrightarrow \frac{\sin(\omega T_s/2)}{\pi\omega T_s/2} e^{-j\omega(T_1+T_s/2)}. \quad (12)$$

The windowed spectrum is given by

$$S(\omega) = X(\omega)H_{PN}(\omega) * \frac{\sin(\omega T_s/2)}{\pi\omega T_s/2} e^{-j\omega(T_1+T_s/2)} = \int_{\omega_L}^{\omega_U} X(\gamma)H_{PN}(\gamma)\frac{\sin((\omega-\gamma)T_s/2)}{\pi(\omega-\gamma)T_s/2} e^{-j(\omega-\gamma)(T_1+T_s/2)} d\gamma. \quad (13)$$

Assuming $X(\omega)$ is relatively constant for $\omega = [2\beta T_s, 2\beta T_1]$, it is set to unity and the effects of windowing on a single chip is examined. The spectrum of the chip due to the time windowing is given by

$$S_{chip,win}^{i}(\omega) = S_{chip}^{i}(\omega) * \frac{\sin(\omega T_s/2)}{\pi\omega T_s/2} e^{-j\omega(T_1+T_s/2)} = \int_{\omega_{L,chip,i}}^{\omega_{U,chip,i}} \frac{\sin((\omega-\gamma)T_s/2)}{\pi(\omega-\gamma)T_s/2} e^{-j(\omega-\gamma)(T_1+T_s/2)} d\gamma. \quad (14)$$

where * denotes the convolution operation. Due to the convolution, energy (and power) from a chip now exists outside the chip's frequencies, and as a result, power in the notch is increased.

The actual notch power depends on the location of the nulled chips within the spreading sequence. If we assume the notch is located at the kth chip for K chips, then the spreading sequence in (8) can be written as

$$PN_{win}(\omega) = \sum_{\substack{i=1 \\ i \neq k}}^{K} S^{i}_{chip,win}(\omega) . \quad (15)$$

The contribution to the notch from all the chips can be written as

$$P_{notch} = \int_{\omega_{L\_chip\_k}}^{\omega_{U\_chip\_k}} \left| PN_{win}(\omega) \right|^2 d\omega . \quad (16)$$

(14) is plotted in Fig. 4 for K=15. For a given desired notch depth, the smallest value of T_s can be chosen, which determines the smallest SAW filter length. However, if $X(\omega)$ can not be approximated as constant, then (13) must be calculated instead.

Another important parameter is the spreading sequence. Longer spreading sequences are desired, since the length determines the number of simultaneous users. Each chip that is set to zero reduces the number of users, since the auto-correlation and cross-correlation properties of these sequences will change. This effect can be reasonably ignored for long spreading sequences, since the cross-correlation relative to the auto-correlation changes very little for long sequences. As an example, for a spreading sequence of length 127, zeroing out 2 bits can, in the worst case, reduce the auto-correlation by approximately 2%, and increase the cross-correlation by approximately 2%. Fig. 5 shows the relative notch power plotted versus chip bandwidth for different values of T_s, which for 40ns is approximately 40Mhz in bandwidth to maintain a notch power of -20dB.

Lastly, an appropriate value for ω_a, the starting frequency of the chirp, must be chosen. From [13], ω_a must be chosen to be much higher than the bandwidth of the chirp, though smaller values allow for easier implementation. Since the real-time implementation described above performs spectral encoding at baseband, from simulations the requirement is to choose $\omega_a > 4\omega_u$ .This also implies that the chirp bandwidth needs to be $\omega_u = 2\beta T_1$.

As an example, for the target system operating in the 3-5GHz frequencies with a 1GHz bandwidth, the input to the system is a bandpass signal between 3-4GHz. The spreading sequence consists of 15 chips, two of which are set to zero for spectral shaping purpose. From Fig. 4, it can be seen that below T_s=30ns, the notch depth increases quickly, while there are diminishing returns to the notch depth as T_s increases. Since larger values of T_s increase the cost of the filters and decrease the data rate, the optimal choice is T_s=35ns, since that is the smallest value that maintains the notch depth of -20dB. Thus choosing T_s=35ns sets T_1=58.33ns, β=2.69x10^{17}. ω_a is chosen to be four times the highest frequency, and hence ω_a=20GHz. However, implementation can be challenging, since currently reported SAW filters can operate up to 10GHz in frequency [15] with bandwidths of up to 1.2GHz [17],

B. Monolithic Implementation

While implementation of the real-time Spectral Encoded UWB system with SAW filters is possible, other methods must also be considered, such as an integrated solution on chip with all transmitter components on-chip. This has the advantage of being a lower cost solution compared to using off-chip SAW filters. In this integrated implementation, the Spectral Encoding spreading is assumed to be fixed for each user. Hence, the transmitter can be composed as shown in Fig. 6 where the DSP pre-calculates the waveform that is then stored into a high speed memory. The memory feeds the DAC, which directly drives the antenna. Though no longer real-time, the system described in the previous section can be used to generate the transmitted waveform; instead of using SAW filters to generate the chirp signals, a tap-delay line structure is used [13].

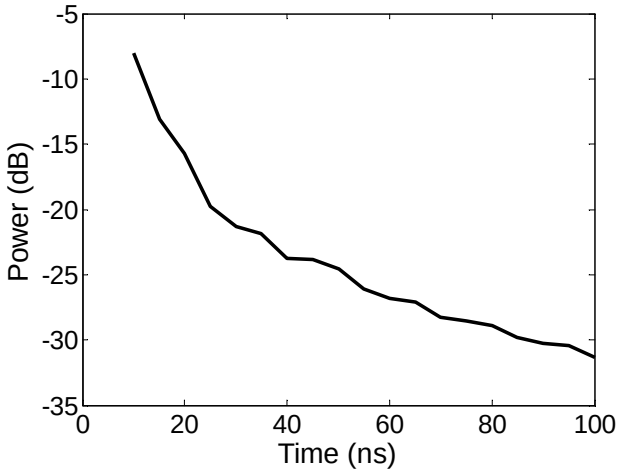

Fig. 4. The power in the notch as a function of T_s, caused by the time windowing of the Fourier Transform on the spreading sequence. A single chip is zeroed to create the notch. K=15, k=10.

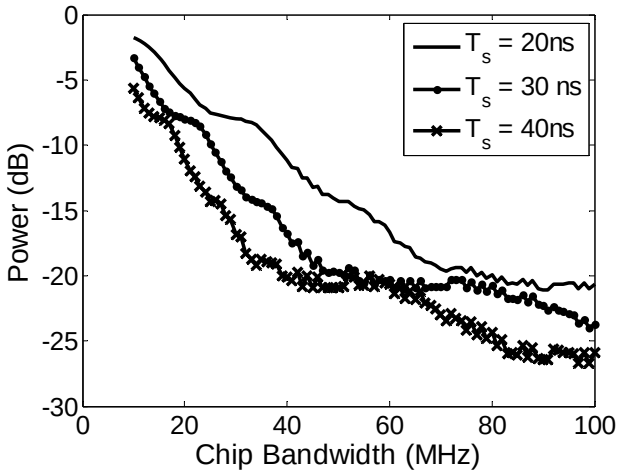

Fig. 5. The power in the notch as a function of the chip bandwidth for various T_s, as a ratio of the notch power to the peak power.

First, we will focus on the design of the DAC. The two main parameters are conversion rate (measured in samples per second), and the resolution (measured in bits). For our target system operating between 3-5GHz, the conversion rate requirement is the Nyquist rate of 10Gsamples/sec. A common topology for DACs running at these speeds is the current-steering topology [19].

Next, the DAC resolution is examined. From [19], each bit provides roughly 6dB of signal-to-noise ratio (SNR),

assuming quantization noise is the primary noise source. While more bits provide a better representation of the signal, each bit also doubles the power consumption and doubles the memory size. Hence, to minimize both the power consumption and memory size, the goal is to choose the minimum number of bits to maintain the desired spectral characteristics. To determine the optimal number of bits, the spectral notch in the Spectral Encoded signal is examined for various bit resolutions. Fig. 7 shows the notch power from (16) plotted against resolution, where values obtained in the previous section are used in the calculations. The minimum number of bits required is five bits, which gives a theoretical SNR of 30dB. Note that while the notch power is at -20dB, which might imply four bits is enough, the spectral characteristics within the notch are as low as -28dB (from Fig. 1(e)), which would require five bits to resolve.

Since DSP devices running at 10GHz are challenging to build, a high speed memory driving the DAC will be considered, which has the advantage of using a slower DSP to pre-compute the Spectral Encoded waveform, and can lead to a lower power implementation. The memory storage requirement is determined by the product of the symbol length T_s, the bit resolution, and the conversion rate. Because the parameter values obtained previously were optimized to maintain the lowest notch power for the smallest SAW filter size, the same parameters and analysis can be used to obtain the smallest memory size. Using the values obtained previously, decreasing the T_s below 35ns (Fig. 4), or reducing the resolution below 5-bits (Fig. 7) will reduce notch performance. The relationship between the memory size and the notch power is summarized in Table 1, where two parameters are varied at a fixed conversion rate of 10Gsamples/sec. Reducing the memory size, which could lead to easier implementation, would require either reducing T_s or the DAC resolution, either of which would increase the power in the notch. Depending on the desired power in the notch, memory size can be reduced significantly. For example, if a notch power of -20dB is desired, from the Table 1 the minimum memory size is 1750 bits. If, on the other hand, a -14dB notch is desired, then it can be seen from Table 1 that choosing T_s = 25ns produces a -14dB notch, as does 4-bit resolution. Therefore, choosing both T_s = 25ns and 4-bit would yield a memory size of 1000 with a notch power of -14dB.

Lastly, for low power implementation, as shown in Fig. 6, the DAC directly drives the antenna without the need of a power amplifier. Thus, the signal requirements at the output of the DAC need to be examined to determine if the DAC can output a signal with enough power. Recall that UWB systems are limited in power to -41.25dBm/MHz [1]. If we assume a 1GHz signal bandwidth, it can be shown that the rms voltage for a sinusoidal wave is 61mV, while a full-band implementation would be 161mV. The DAC needs to be designed to meet these output voltage swings.

The integrated implementation seems to be more realizable with currently reported technology, as a 6-bit DAC using current-steering topology has been reported running at 22Gsamples/sec [21]. However, high speed memory cells with 1750 bits are challenging to design, as the currently reported read speed for a 1024-bit memory is roughly 3GHz [22], shy of the 10GHz minimum for our targeted system.

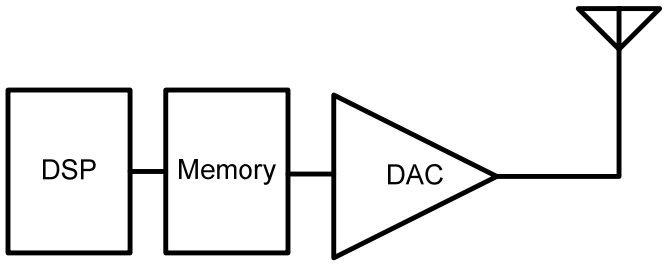

Fig. 6. Block diagram of the Spectral Encoded UWB system, with the DSP,

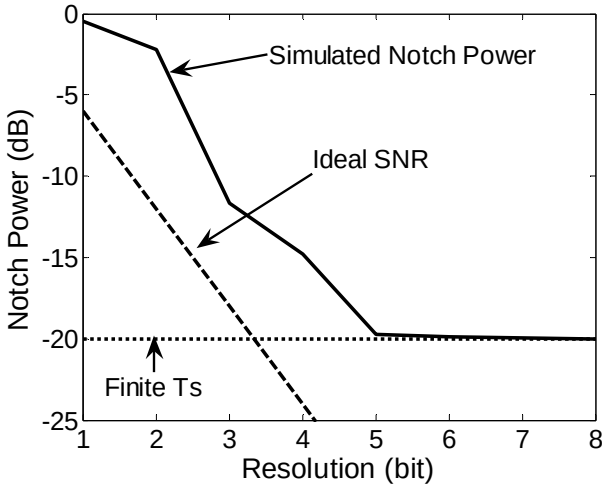

Fig. 7. Notch power vs. DAC resolution. Also shown are the lower bounds from the DAC resolution SNR and the boundary for T_s=35ns.

T_s (ns)	Resolution (bits)	Memory Size (bits)	Notch Power (db)
25	4	1000	-14
35	3	1050	-12
25	5	1250	-14
35	4	1400	-14
30	5	1500	-18
35	5	1750	-20
40	5	2000	-20
35	6	2100	-20

Table 1. The memory size and notch power relationship for various T_s and resolutions, assuming the conversion rate is fixed at 10 Gsamples/sec.

IV. Conclusion

Two possible hardware implementations of a Spectral Encoded UWB transmitter are discussed. The first is an all analog implementation, with the use of off-chip SAW filters to perform the chirp transforms. The advantage of this system is its real-time performance. However, the main challenge for this implementation is the design of SAW chirp filters that have a wide operating bandwidth of at least 5GHz. The second implementation is an integrated one, where the Spectral Encoded waveform is pre-calculated. The resulting

waveform is then stored in a high speed memory, which drives a high speed DAC. This has the advantage of low cost due to integration, and low power with the DAC directly driving the antenna. While high speed DACs meeting the requirements of the Spectral Encoded system have been reported, a high speed memory of that size is challenging to build, and is a possible area for future research.

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