A 25 GHz Quadrature Voltage Controlled Ring Oscillator in 0.12 μm SiGe HBT (Student paper)

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Abstract **- A 25 GHz Ring VCO is fabricated in a 0.12µm SiGe BiCMOS process. The VCO with a 3.3V supply consumes 32mA. The measured phase noise is -105dBc/Hz at 10MHz offset from the center frequency of 24.3 GHz. Design optimization techniques for high performance ring oscillators in a 0.12 µm SiGe HBT technology are discussed.**

Index Terms **— Quadrature Ring Oscillator, Millimeter wave integrated circuits, SiGe, Voltage Controlled Oscillator, Bipolar.**

I. INTRODUCTION

Multi Gigabit-per-second wireless data rates are possible in high frequency millimeterwave bands [1,2]. Advanced Silicon Germanium (SiGe) and CMOS technologies which offer high frequency operation can now be used for developing applications in the millimeterwave bands. Applications for these frequencies include high data rate wireless communications in the 57-64 GHz band and automotive radars in 24 and 77 GHz.

Voltage Controlled Oscillators are used in these systems for frequency synthesis. Ring oscillators take up less die area and have a wider tuning range than traditional LC oscillators. For simple modulation schemes such as BPSK and QPSK, the phase noise requirement is relaxed and ring oscillators can be used despite their phase noise performance. In addition, quadrature local oscillator signals are required for most direct downconversion systems, as well as in subharmonic mixers [3]. A two stage differential ring oscillator can be employed for this purpose as shown in Fig. 2 [4].

Analytical BER versus E_b/N_o curves for QPSK modulation in an AWGN channel for varying integrated rms phase noise is shown in Fig. 1 [5]. As the phase noise increases, the BER performance degrades. For a BER of 1e-6, the degradation in E_b/N_o is less than 1 dB for integrated rms phase noise of about 5° rms compared to without phase noise. Ring oscillators may hence be used in simple modulation schemes such as BPSK and QPSK despite their poor phase noise performance

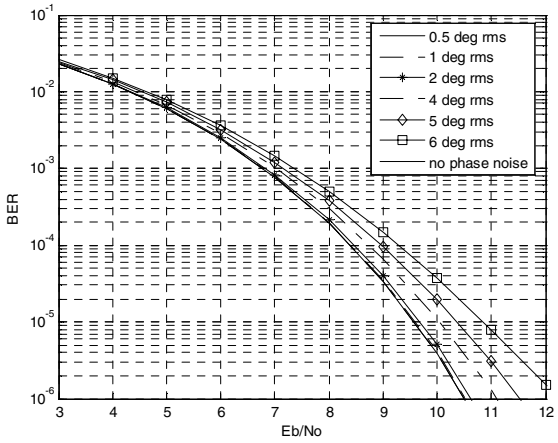

Fig. 1. Effect of phase noise on BER versus E_b/N_o for QPSK

The design of a a two-stage ring oscillator at 25 GHz in a SiGe HBT technology, with the core oscillator consuming 16 mA per stage at 3.3 V, is described here.

II. CIRCUIT DESIGN

A. Two Stage Ring Oscillator

The block diagram of a standard two-stage ring oscillator schematic is shown in Fig 2. For an even number of stages, using differential pairs and cross connecting the output of one of the stages to the input of the next stage, can provide the necessary gain and phase conditions given by Barkhausen criterion for sustained oscillations [6].

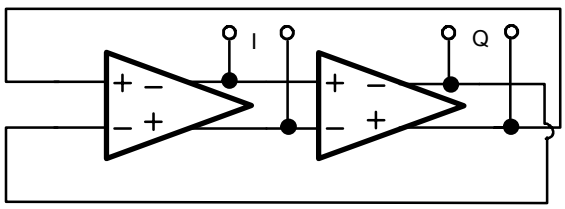

Fig. 2. Block Diagram of a two-stage Ring Oscillator.

The oscillation frequency of an N-stage ring oscillator is depends on the net delay in each stage and is given by

$$f_{osc} = \frac{1}{(2N\tau_{delay})} \quad (1)$$

Here N is the number of stages and τ_{delay} is the large signal delay in each stage.

For an even number of stages, the phase criterion is met when each stage provides a phase shift of π/N. Thus, for a two stage ring oscillator, the phase shift provided by each stage is 90°. Hence, quadrature outputs are obtained after each stage. A higher number of stages can also provide quadrature signals, but they consume more power. Analysis of ring oscillators based on differential topology shows that a minimum number of stages is optimum for phase noise considerations [7]. Hence a two stage ring oscillator is chosen.

B. Circuit Design

The delay cell of the designed two-stage ring oscillator constitutes an Emitter Coupled Logic cell which is a differential pair, followed by an emitter follower buffer as shown in Fig. 3.

The phase noise of a two-stage differential bipolar ring oscillator considering only the collector shot noise and the thermal noise of the load resistor is given by [7]

$$L_{osc}\{\Delta f\} = 10\log\left[\frac{16}{3\eta}\frac{KT}{P}\left(\frac{V_{CC}}{4V_t}+\frac{V_{CC}}{I_{ee}R_C}\right)\left(\frac{f_{osc}}{\Delta f}\right)^2\right] \quad (2)$$

Here, L_{osc} is the phase noise in dBc/Hz at an offset frequency Δf for an oscillator oscillating at frequency $f_{osc.}$ P is the power dissipated in the circuit, K is Boltzman's constant, T is the temperature, I_{ee} is the tail current of the differential pair, V_t is thermal voltage, η is a proportionality constant typically close to unity, and R_c is the load resistor at the collectors of the differential pair. From the above equation, it is clear that increasing the voltage swing, which is given by $2I_{ee}R_c$ reduces phase noise. Design of low phase noise ring oscillators thus involves providing high swing while reducing the noise contributions of the various noise sources.

In addition to buffering, the emitter follower provides a low source impedance to the base of the differential pair transistors Q1 and Q2. The NPN transistors have a BV_{CEO} of 1.7V and a BV_{CBO} of 5.5V. The breakdown voltage for these transistors is BV_{CER} which is between BV_{CEO} and BV_{CBO} because of the low impedance seen by the base. The critical multiplication factor, M is given by [8]

$$M = 1+\frac{1}{\beta}\left[\frac{(\beta+1)V_t}{R_B I_E}-1\right] \quad (3)$$

where I_E is the emitter current, β is the current gain, and R_B is the resistance seen at base. For an open base, the expression reduces to $M=1+1/\beta$ which is the condition for open base collector-emitter breakdown voltage B_{VCEO}. Higher voltage swings are possible without letting the transistors to go into breakdown due to the low impedance seen by the base of Q1 and Q2. Simulations show that the collector-emitter voltage is approximately 2 V at the highest bias current. The differential voltage swing is 1 V. The transistors Q1 and Q2 are sized and biased to maintain a high f_T and also to reduce their base resistance noise contribution.

For a two stage ring oscillator using this topology, the oscillation frequency is given by [9]

$$f_{osc} = \frac{1}{2\pi\sqrt{R_c C_c\left(r_{b1}+\frac{1}{g_{m3}}\right)C_{be_1}}} \quad (4)$$

where C_c is mainly due to the collector to substrate capacitance of Q1 or Q2, R_c is the load resistance at the collectors of the differential pair, r_{b1} is the base resistance of Q1 and C_{be1} is the base-emitter capacitance. The oscillation frequency can be tuned by changing the current which increases the charging current of the parasitic capacitances, increasing the frequency.

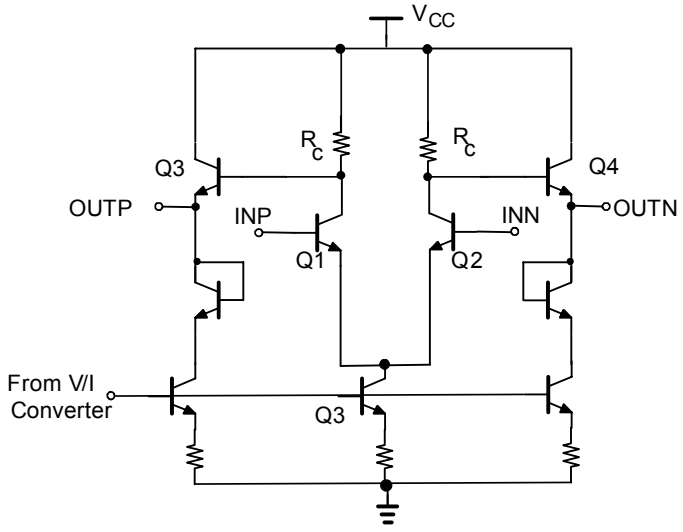

Fig. 3. Schematic of the delay stage of the Ring Oscillator

Tuning is obtained by changing the bias current of the delay cells through a V/I converter. Two buffer stages follow the Ring Oscillator and drive the load through 50 ohm microstrip lines to the bond pads. The transmission lines are formed using thick top metal over bottom metal ground plane.

III. Measurement Results

The circuit is fabricated in a seven metal layer IBM 8HP 0.12 µm SiGe BiCMOS process [12].

The measured spectrum at 24.3 GHz is shown in Fig. 4. The phase noise plot is shown in Fig. 5. At 24.3 GHz, the phase noise is -105 dBc/Hz at 10 MHz offset. The oscillation frequency can be tuned from 18.5 GHz to 25 GHz as shown in Fig. 6.

The VCO core consumes a total of 32 mA at 3.3V, consuming a power of 105.6 mW. The VCO *Figure of Merit* defined as [4]

$$FOM = PhaseNoise(dBc/Hz) - 10\log((\frac{f_{offset}}{f_{osc}})^2 P_{diss-mW}) \quad (5)$$

Here, f_{offset} is the offset frequency where the phase noise is measured, phase noise is in dBc/Hz at the offset

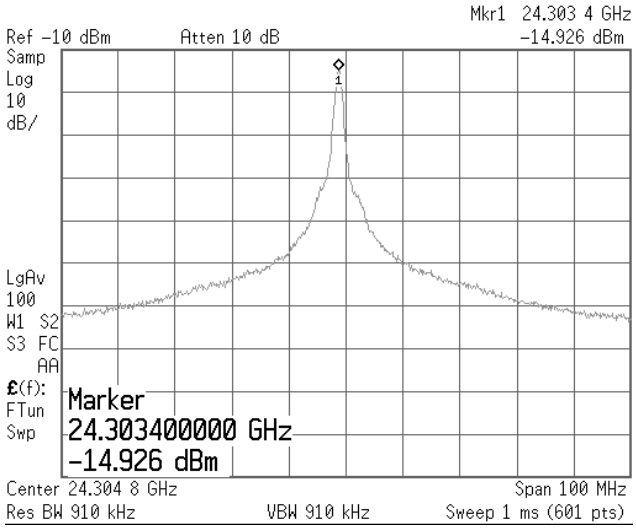

Fig. 4. Spectrum of the Ring Oscillator.

The VCO figure of merit for this oscillator based on the above equation is -152 dBc/Hz. This is comparable to recent high frequency ring oscillators in Silicon bipolar and InP technologies as indicated in Table 1.

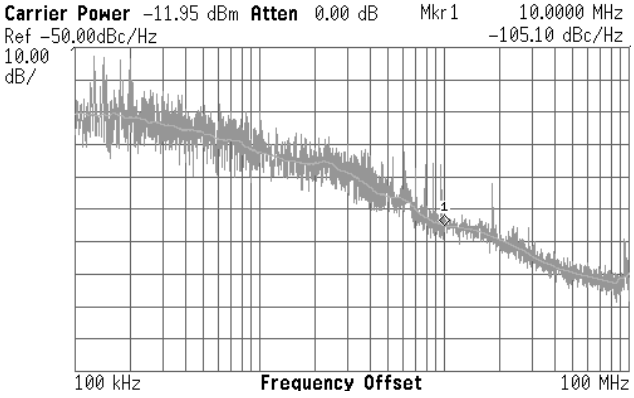

Fig. 5. Phase Noise Specturm the two-stage Ring Oscillator.

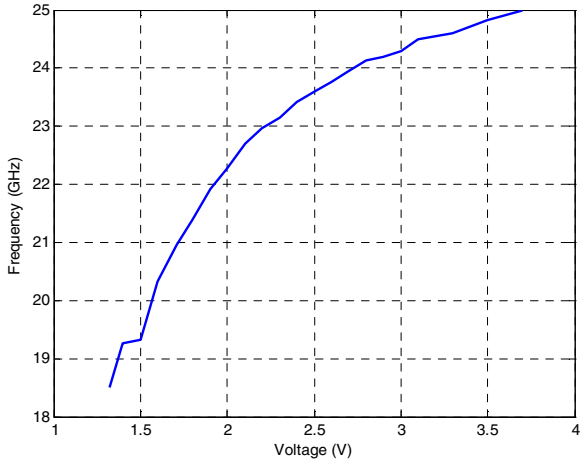

Fig.6. Oscillation Frequency Variation with Tuning Voltage.

	Frequency (GHz)	Phase Noise (dBc/Hz)	I/Q	Power (mW)	Technology	FOM (dBc/Hz)
[4]	11.5	-94.3 @ 2MHz	Yes	75	0.5 µm BiCMOS	-150.7
[10]	18.7	-90 @1MHz	No	80	InP HBT	-156.3
[11]	26	-85 @1MHz	No	250	InP HBT	-149.3
This Work	24.3	-105 @10MHz	Yes	105.6	0.12 µm SiGe BiCMOS	-152.7

Table. I. Comparison of performance with other work

The ring oscillator die photograph is shown in Fig 7. The die occupies a total of 1.3 x 1.3 sq mm. This includes the G-S-G-S-G differential probe pads, the buffers and 50 ohm microstrip lines. The active area of the ring oscillator

including the emitter follower buffers, but excluding the 50 ohm lines and the pads, is 460 x 320 sq.um.

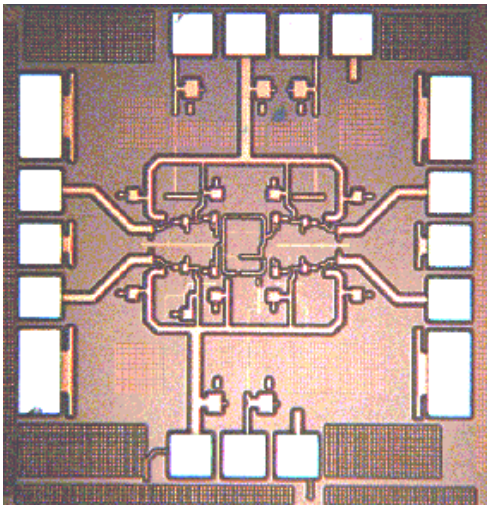

Fig. 7. Microphotograph of the Oscillator.

IV. CONCLUSIOINS

A 25GHz 0.12 μm SiGe Ring VCO operating at 3.3 V power supply and 32 mA current consumption is presented. Measured phase noise is -105dBc/Hz at 10MHz offset with a center frequency of 24.3 GHz: the corresponding figure of merit is -152 dBc/Hz. These results demonstrate for the first time, a two-stage ring oscillator at these frequencies with good phase noise performance for quadrature generation at millimeter wave wireless applications using SiGe technology.

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