A Low-Voltage 12GHz VCO in 0.13 μm CMOS for OFDM Applications

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Abstract **– A low voltage 12GHz VCO is fabricated in a 0.13µm CMOS process. The VCO with a 0.8V supply consumes 6mA. The measured phase noise is -84dBc/Hz at 100kHz and -106dBc/Hz at 1MHz offset from the center frequency. Design optimization techniques for high performance VCOs in a low voltage CMOS process are discussed.**

Index Terms **— CMOS, VCO, High Frequency, Low Voltage, Phase Noise**

I. INTRODUCTION

As CMOS moves into the sub-100nm regime, low voltage circuit design techniques will be required for highly integrated WLAN transceivers. Direct-conversion transceivers are the most highly integrated solutions and, in order to avoid LO-induced DC offset issues, their Voltage-Controlled Oscillators (VCOs) often operate at twice the RF frequency. At the same time, these VCOs need to operate at the very low voltages required by technology scaling while maintaining the low phase noise and residual phase error desired by advanced modulation approaches. The design techniques described here result in a CMOS VCO operating at 0.8V and only 6mA current consumption, while maintaining outstanding phase noise.

II. CIRCUIT DESIGN

The key for achieving good phase noise performance in the low dc voltage regime is to maximize the voltage swing, as well as the loaded quality factor, of the resonator.

A. Optimized Resonant Tank Design

For high operating frequencies, the upper limit on the inductor value is limited by varactors and parasitic capacitors. For our case, the inductance is only 0.5nH. In order to obtain a small inductance value with high Q, we use a single turn octagonal inductor. By selecting the trace width, we can reduce the series resistance and adjust the inductor self-resonant frequency to roughly twice the operation frequency. The tank inductor is a fully

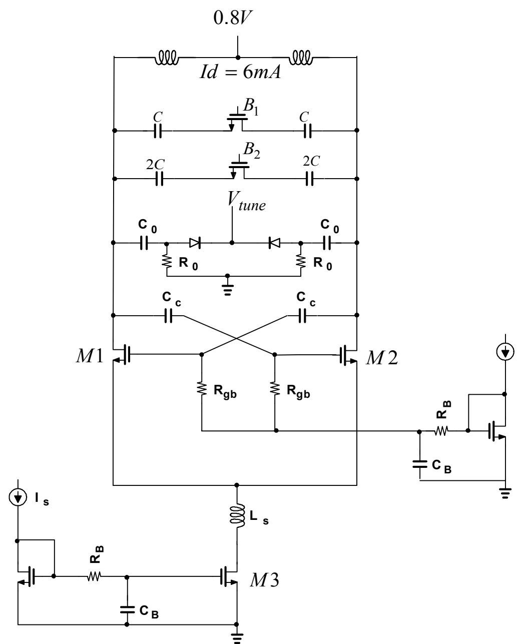

Fig. 1. VCO Schematic

differential single turn structure implemented in the 0.9 µm top layer metal with a Q of approximately 16 at 12GHz. At high operating frequencies, the finite varactor Q will also degrade the resonator quality factor. Here we use a small size PN junction varactor with Q of approximately 12GHz.

B. Voltage Swing Constraint for Low Voltage Operation

The phase noise of a VCO can be empirically described by the modified Leeson's equation as [1]

$$S_{\Delta\phi}(\omega_m) \cong \left(\frac{2 \cdot F \cdot kT}{P_s}\right) \cdot \left(1 + \frac{1}{4Q^2} \cdot (\frac{\omega_c}{\omega_m})^2\right) \cdot \left(1 + \frac{\omega_{1/f^3}}{|\omega_m|}\right) \qquad (1)$$

where $S_{\Delta\phi}(\omega_m)$ is the single sideband output phase noise power spectral density at a frequency ω_m away from the center frequency ω_c. F is often called the "device excess noise factor" and in practice its exact value needs to be

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obtained from fitting of the measurement data or extensive simulation.

For low voltage operation, the output swing (and hence the phase noise) is limited by the breakdown voltage of the process; in this case, the maximum voltage between any two terminals of the transistor should less than 1.2V for reliability constraints. Fig. 2 show a simplified VCO schematic with instantaneous waveform $V_{ds}(t)$ and $V_{gs}(t) - V_{th}$. The maximum swing V_{pk} should satisfied $V_{pk} + V_{DD} - V_s < 1.2$ as show in point A in Fig 2. Also, in order to insure that both M2/M3 operate in the saturation region $V_{ds}(t) > V_{gs}(t) - V_{th}$ as shown by point B in Fig.2. where, Δt is the time period that the transistor is in the linear region and T is the oscillation period. Reducing Δt/T will prevent degradation of tank quality factor by active devices.

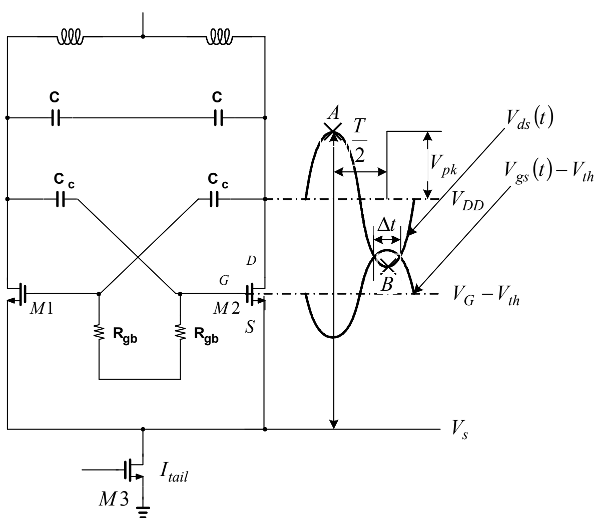

Fig.2. Simplified VCO with Waveform

With the limited Q of the tank circuit, the output swing V_{pk} is directly proportional to the tail current I_{tail}. A higher tail current increases the output swing, but a lower tail current is important for lowing the device 1/f noise and thermal noise. So, there is optimal tail current value to minimize the phase noise.

We selected a large tail current transistor together with a series inductor to form an RF filter to reduce the downconversion of thermal noise from the current source [2]. Simulation verifies that by replacing the current source transistor with an ideal current source, we achieve almost identical phase noise performance. A band switching approach is employed to reduce the K_{vco} to 120MHz/V, and a grounded PN junction varactor is employed for fine tuning. The measured analog tuning characteristic around 11.2GHz is shown in Fig.3.

C. 1/f Noise Reduction

Equation (1), implies that increasing the voltage swing will improve the $1/f^3$ behavior of the VCO. When CMOS devices are scaled down to deep-submicron, their 1/f noise corner frequency increases to 10~100MHz, which can be up-converted to the VCO output to produce $1/f^3$ phase noise. In our case, 1/f noise up-conversion is minimized by choosing a large M3 together with a LPF at the gate bias point to reduce current mirror 1/f noise[3]. Appropriate capacitor coupling between the drain and gate to keep the transistor in the saturation region will also reduce 1/f noise from M1/M2 up-conversion to close-in phase noise[4]. The size of transistors M1/M2 is optimized for increasing linearity - to reduce 1/f noise AM-PM upconversion - and increasing size to reduce the 1/f noise magnitude[5]. The combination of all these design approaches results in a VCO with very low 1/f noise upconversion. The resulting phase noise simulation in Fig. 6 shows the phase noise maintaining 20dB/decade to 10kHz, suggesting the phase noise $1/f^3$ corner can be below 10kHz

III. Measurement Results

The circuit is fabricated in a six metal layer 0.13 μm CMOS process. The VCO was locked to 11.2GHz by an external PLL with a 30kHz loop bandwidth. The measured VCO spectrum is shown in Fig. 4 with -84dBc/Hz at 100kHz offset and Fig. 5 with -106dBc/Hz at 1MHz offset from 11.2GHz, the corresponding phase noise plot is shown in Fig. 7 The integrated rms phase jitter from 50kHz~10MHz is 2.82 degree. Thanks to the use of the design criteria mentioned above, the $1/f^3$ noise corner frequency is less than 30 kHz. The phase noise $1/f^3$ corner is less than the 30 kHz bandwidth of the PLL loop filter.

To compare our VCO performance, the following popular figure of merit (FOM) is used:

$$FOM = L(f_c) - 20\log(f_0/f_c) + 10\log(P_{DC}/1mW) \qquad (2)$$

where $L(f_c)$ is the phase noise measured at offset frequency f_c from the VCO oscillating frequency f_0, and P_{DC} is the power consumption. The VCO Figure of Merit for this circuit is -180 dBc/Hz, which compares favorably to recent CMOS VCOs in this frequency regime *operating at higher voltages* as shown in Table I. This demonstrates that excellent VCO performance can be achieved in the 130 nm and below regime. The VCO die photograph is

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shown in Fig. 8 with size of 0.7mm by 0.7mm including on-chip low pass filter

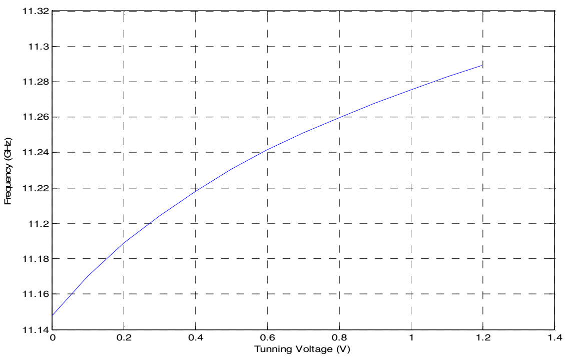

Fig. 3. Measured VCO tuning at 11.2GHz

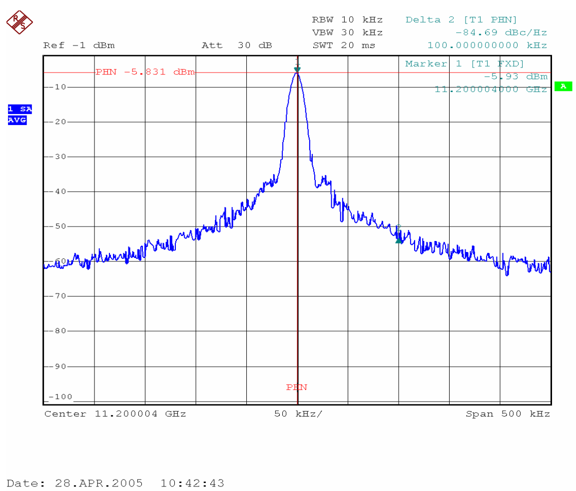

Fig. 4. VCO Spectrum at 11.2GHz, -84.7dBc/Hz@100kHz

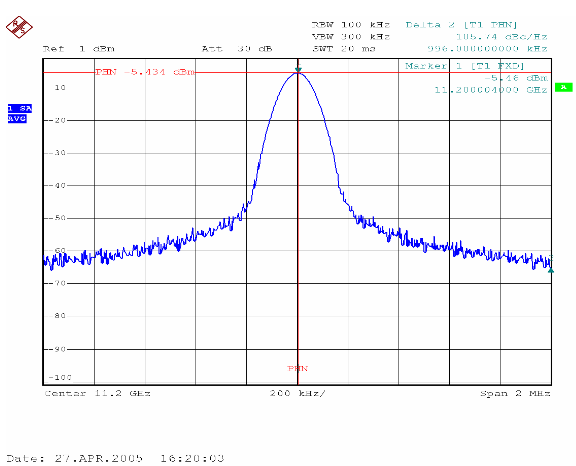

Fig. 5. VCO Spectrum at 11.2GHz, -105.7dBc/Hz@1MHz

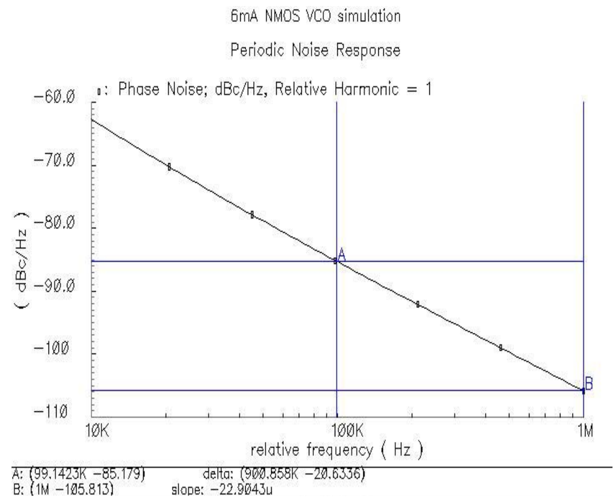

Fig. 6. Simulated plot of VCO Phase Noise

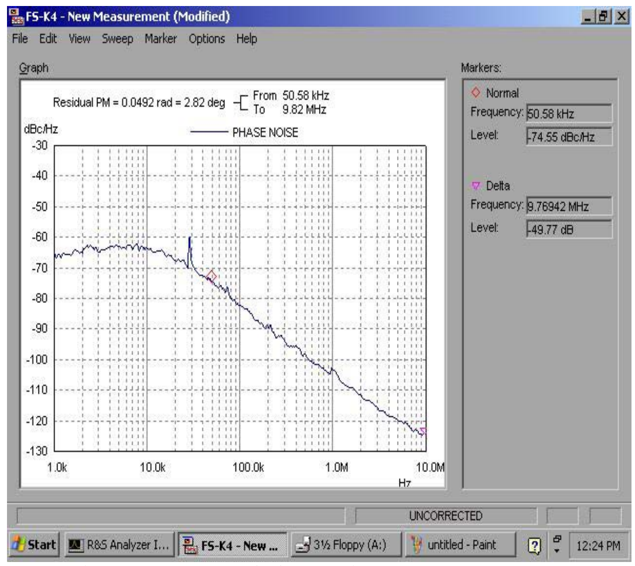

Fig. 7. Measured phase noise at 11.2GHz

	Frequency GHz	Phase Noise dBc/Hz	VDD V	Power mW	Technology	FOM dBc/Hz
[6]	11.64	-103 @ 1MHz	0.7V	2	0.18um CMOS	-180
[7]	8.56	-96 @ 100KHz	1.3V	14	0.18um CMOS	-183
[8]	10	-127 @ 3MHz	2.5V	50	0.25um CMOS	-181
[9]	17	-108 @ 1MHz	1.4V	10	0.25um CMOS	-182
[10]	9.8	-115 @ 1MHz	2.7V	12	0.35um CMOS	-184
This Work	11.2	-106 @ 1MHz	0.8V	4.8	0.13um CMOS	-180

Table I. VCO FOM Comparison

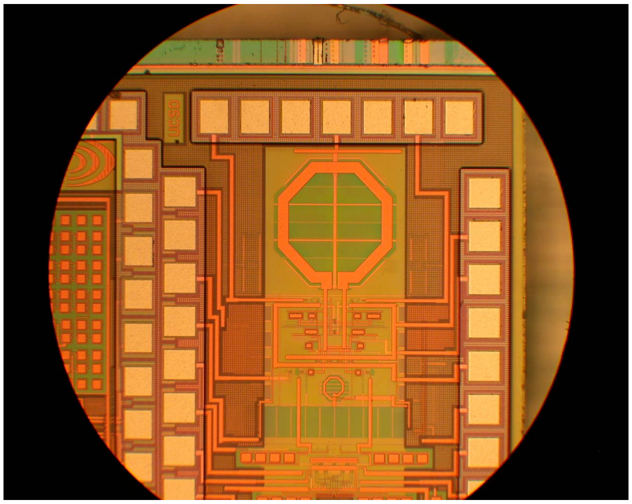

Fig.8. VCO Microphotograph

IV. CONCLUSION

A 12GHz 0.13 µm CMOS VCO operating with 0.8V power supply and 6mA current consumption is presented. The measured phase noise is -84dBc/Hz at 100kHz and -106dBc/Hz at 1MHz from 11.2GHz, and the corresponding figure of merit is -180dBc/Hz. These results demonstrate that careful attention to minimizing the contribution of noise sources in a VCO as well as maximizing the voltage swing can result in a VCO with excellent performance in the sub-1V regime.

Acknowledgement

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