

High-Efficiency Envelope-Tracking W-CDMA Base-Station Amplifier Using GaN HFETs

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Abstract—A high-efficiency wideband code-division multiple-access (W-CDMA) base-station amplifier is presented using high-performance GaN heterostructure field-effect transistors to achieve high gain and efficiency with good linearity. For high efficiency, class J/E operation was employed, which can attain up to 80% efficiency over a wide range of input powers and power supply voltages. For nonconstant envelope input, the average efficiency is further increased by employing the envelope-tracking architecture using a wide-bandwidth high-efficiency envelope amplifier. The linearity of overall system is enhanced by digital pre-distortion. The measured average power-added efficiency of the amplifier is as high as 50.7% for a W-CDMA modulated signal with peak-to-average power ratio of 7.67 dB at an average output power of 37.2 W and gain of 10.0 dB. We believe that this corresponds to the best efficiency performance among reported base-station power amplifiers for W-CDMA. The measured error vector magnitude is as low as 1.74% with adjacent channel leakage ratio of -51.0 dBc at an offset frequency of 5 MHz.

Index Terms—Efficiency, envelope elimination and restoration (EER), envelope tracking (ET), power amplifier.

I. INTRODUCTION

IN ADDITION to excellent linearity, high efficiency is essential for low-cost high reliability wideband code-division multiple-access (W-CDMA) base-station power amplifiers. Si LDMOS has been a popular transistor choice for base-station high-power amplifiers since LDMOS technology can provide reliable and cost-effective solutions [1]. However, in order to obtain better linearity and efficiency for third-generation (3G) wireless base stations, intense research on high-voltage GaAs heterojunction bipolar transistors (HBTs) [2] and field-effect transistors (FETs) [3], as well as GaN heterostructure

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field-effect transistors (HFETs) [4], [5] has been carried out. GaN HFETs can provide higher voltage operation and higher power density at microwave frequencies than other high power devices and thus are attractive for application to commercial high-power base stations.

Recently, high-performance GaN HFETs on Si substrates (instead of the more customary sapphire or silicon-carbide substrates) have been reported, showing 150-W output power with high linearity and high reliability for W-CDMA base-station applications [5]. The use of this GaN power amplifier within an envelope-tracking (ET) architecture was recently reported by the authors in [6]. This paper presents performance characteristics of this amplifier system, which employs a dynamic supply voltage for efficiency enhancement. Section II introduces the configuration of the overall ET system. The high-efficiency performance of the RF power amplifier is analyzed by ADS simulations showing class J/E waveforms. Single-tone measurement results are also given in Section II. The design concept for the envelope amplifier is demonstrated in Section II, along with measurement results. In Section III, the measured performance of the overall ET power amplifier is illustrated including an instantaneous measurement of the RF stage efficiency, which demonstrates the essential characteristics of the ET amplifier-high-efficiency operation of the RF amplifier over a wide output power range. The power dissipation reduction within the transistor is also demonstrated resulting from the ET operation, which improves the reliability and longevity of the device.

II. ET BASE-STATION AMPLIFIER

A. Description of ET Systems

The block diagram of the ET amplifier used in this study is shown in Fig. 1. The W-CDMA signal is generated in the digital domain, and consists of an envelope signal as well as in-phase (I) and quadrature (Q) IF signals. After up-conversion, the resultant RF signal provides the input to the RF amplifier, which is time varying (unlike the case for the envelope elimination and restoration (EER) architecture). The supply voltage for the RF amplifier is modulated by the amplified envelope signal through an efficient wideband envelope amplifier so that the RF amplifier keeps operating close to its saturated power region for all envelope amplitudes to improve average efficiency.

The average efficiency of an ET power amplifier strongly depends on the peak-to-average power ratio (PAR) and probability density function (PDF) of the modulated input signal since the drain bias voltage varies in proportion to the amplitude of input

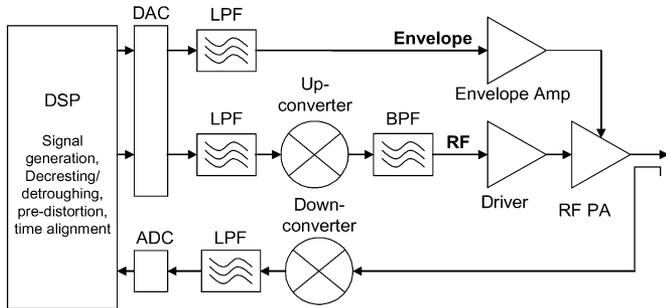


Fig. 1. Block diagram of ET base-station amplifier including signal generation and up/down conversion [6].

signal. It is challenging to maintain high efficiency over a wide range of drain bias due to the dependence of output capacitance and transconductance on drain voltage. As a result, the efficiency of the RF amplifier is usually optimized at the drain bias voltage corresponding to the maximum PDF in order to provide the maximum average efficiency under ET operation [7].

To deal with the high PAR problem, a de-cresting procedure (adjustment of the PAR of the input signal) was employed. This procedure was performed digitally on the envelope of the signal to optimize the efficiency, adjacent channel leakage ratio (ACLR), and error vector magnitude (EVM) performance. The original W-CDMA input signal with 9.8-dB PAR was de-crested to have a PAR of 7.67 dB [7]. This reduction of PAR helps to improve the average efficiency of the RF amplifier and limits the dynamic range of the envelope amplifier. The procedure was carried out in the digital domain as follows. For a baseband input signal $s(n) = A(n)e^{j\phi(n)}$, where $A(n)$ and $\phi(n)$ represent the amplitude and phase of the n th time sample, respectively, an error vector $E(n)$ is calculated from

$$E(n) = \begin{cases} (A(n) - A_m)e^{j\phi(n)}, & \text{if } A(n) > A_m \\ 0, & \text{otherwise} \end{cases}$$

where A_m is the maximum amplitude of the target PAR.

A new error vector $E_p(n)$ corresponding to local envelope peaks is then obtained using

$$E_p(n) = \begin{cases} E(n), & \text{if } |E(n)| > |E(n-1)| \text{ and } |E(n)| > |E(n+1)| \\ 0, & \text{otherwise.} \end{cases}$$

This signal is passed through a low-pass filter to obtain $E_d(n)$. Finally, de-crested signal $s_d(n)$ is generated by $s_d(n) = s(n) - E_d(n)$. This procedure can be iterated to achieve the desired PAR. The degradation of EVM and spectral shape due to de-cresting is minimized by optimizing the cutoff frequency of the low-pass filter. Half the chip rate was used for the bandwidth of low-pass filter in the W-CDMA signal.

To minimize distortion by the time-delay difference between envelope and RF paths, which is known to be one of the major distortion mechanisms in EER or ET systems [8], synchronization is performed by maximizing the amplitude and phase correlation between the input and down-converted output signals [9]. In addition to the differential delay, there are other sources of nonlinearity in the ET amplifier such as AM-AM and AM-PM

distortion created by the varying drain bias voltage. These are called V_{dd} -AM and V_{dd} -PM distortion, respectively [10], and are a result of the variation of the transconductance and output capacitance of the FET with drain bias. The distortion due to nonlinearity of the envelope amplifier itself can also degrade the linearity of the overall power amplifier.

To minimize the distortion caused by the RF amplifier and envelope amplifier, pre-distortion is carried out in the digital domain. The pre-distorted input signal is created by the inverse function of the measured AM-AM and AM-PM characteristics of the overall ET system without separately correcting the V_{dd} -AM and V_{dd} -PM, as well as AM-AM and AM-PM of the envelope amplifier.

To avoid gain collapse of the RF amplifier at low drain voltages, the envelope of the signal was also “detroughed” using an exponential function so that the minimum of drain bias is 3 V.

B. RF Amplifier Using GaN HEMT

An RF amplifier with high efficiency over a wide drain bias range is essential to the ET system. An Si-LDMOSFET amplifier typically exhibits a “peaky” drain efficiency (DE) as a function of the output power in ET applications for W-CDMA input signals due to the high-voltage dependence of the output capacitance, which degrades the average efficiency [7]. On the other hand, the GaN HFET shows a relatively small variation of output capacitance with respect to the drain voltage, as well as a smaller value of capacitance than Si-LDMOS [11]. Thus, the GaN FET is very well suited for ET applications since it can provide a higher efficiency over the full range of output power.

In this study, a Nitronex GaN HFET was used for the high-efficiency RF power amplifier. The device was fabricated on a high-resistivity ($>10^4 \Omega \cdot \text{cm}$) Si substrate with the device structure shown schematically in Fig. 2(a). Two transistor die with 36-mm gatewidth each (for a total gatewidth of 72 mm) were employed to achieve 150-W peak output power. The gate length was 0.7 μm . The implemented linear RF power amplifier with class AB bias showed a 150-W peak output power and maximum PAE of 65% under continuous wave (CW) operation at 2.14 GHz [5]. As will be shown later, maximum DE increased to 80% under ET operation as a result of reduced device temperature and optimized output tuning. Simulations were used to demonstrate how this RF amplifier could obtain that high-efficiency performance.

For accurate simulation of the power amplifier, a nonlinear equivalent-circuit model for the GaN HFET was developed using the empirical large-signal model published in [12]. We slightly modified the equations to better describe the I - V curve around the knee voltage. The drain current is given by $i_{DS} = (\beta v_{GS3}^2) / (1 + v_{GS3}^{\text{pln}} / VL) (1 + \lambda v_{DS}) \tanh(\alpha v_{DS})$, where v_{GS3} is a function of the gate-to-source voltage v_{GS} (refer to [12]). The parameter α of the hyperbolic tangent function corresponds to a third-order polynomial function of the gate voltage v_{GS3} , or $\alpha v_{DS} = (\alpha_0 + \alpha_1 v_{GS3} + \alpha_2 v_{GS3}^2 + \alpha_3 v_{GS3}^3) v_{DS}$, in order to better reflect the knee voltage variation with gate voltage. The simulation speed and convergence were also improved by adopting a simple approximate function for the nonlinear gate charge equation. The gate capacitance was represented in the initial model by a hyperbolic tangent function of

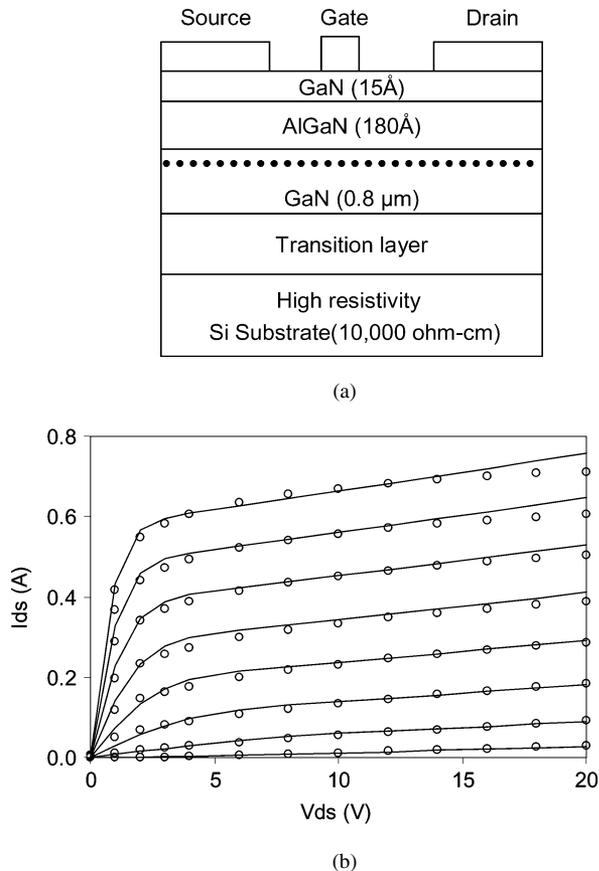


Fig. 2. (a) Nitronex GaN HFET device structure. (b) Comparison of I - V characteristics between measurement (circle) and model (solid line) for a 2-mm GaN FET. Gate bias was swept from -2.6 to -1.2 V with 0.2-V step. The I - V curves were measured on a pulsed basis at quiescent drain and gate voltage of 20 and -3 V, respectively.

gate voltage. We used a square root function to express the non-linear gate charge on the basis that the integral of the hyperbolic tangent $\ln(\cosh(x))$ can be approximated by $\sqrt{x^2 + 1} - 1$. Fig. 2(b) illustrates the excellent agreement between measured pulsed I - V and the predicted curves for a 2-mm GaN FET.

Even though switching-mode amplifiers such as classes D, E, and F are known to provide high efficiency at gigahertz frequencies [13], they are often undesirable for ET applications due to their poor linearity performance. Instead, linear class AB amplifiers are usually employed in ET amplifiers. In this study, an amplifier that approximates class AB operation with quiescent current of 2.0 A was initially designed at 2.14 GHz with harmonic impedance tuning, considering the output capacitance of the RF transistor. In general, for class AB amplifiers, the second harmonic voltage component at the output is minimized with a short circuit to reduce the peak-to-peak drain-to-source voltage swing for a given fundamental component [13].

The GaN HFET used in this study has an output capacitance of 0.5 pF/mm. In practice, this output capacitor does not provide a good short circuit at harmonic frequencies, but rather presents a capacitive load. In [11], it was shown that a capacitive load at the second harmonic frequency can lead to a high-efficiency waveform with a quasi-half-sine-wave voltage and

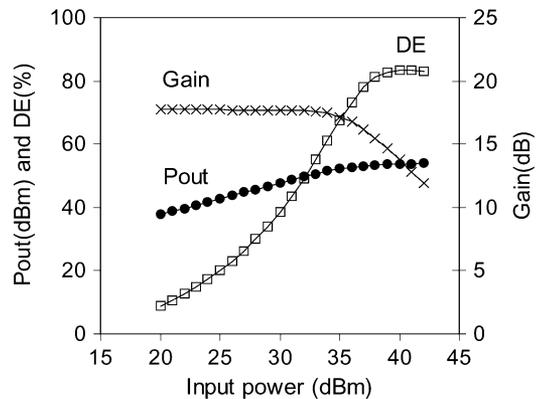


Fig. 3. Simulated output power (P_{out}), gain, and DE as a function of input power at drain bias of 28 V and quiescent current of 2.0 A with fundamental load impedance Z_{L1} of $0.45 + j1.00 \Omega$ and harmonic open circuit.

half-sine-wave current at the drain of the transistor. The corresponding power amplifier with these ideal waveforms has been named “class J” and promises a maximum efficiency of 87% (even though voltage and current waveforms are both nonzero during 90°). The class J amplifier is a quasi-linear amplifier with class AB bias condition, and it has the same harmonic load condition as the class E power amplifier.

A class J amplifier was investigated with the GaN HFET in order to benefit from its high efficiency and simple harmonic impedance tuning. At the second and higher harmonic frequencies, the load impedance was designed to provide an open circuit so that the current source within the FET sees only the output capacitor (like a class E amplifier). To determine the optimum fundamental load impedance for a 72-mm GaN FET at 2.14 GHz, a harmonic-balance simulation was performed by sweeping the load impedance at a drain bias of 28 V. Fig. 3 shows the simulated DE and output power as a function of input power under the optimum load impedance $Z_{L1} = 0.45 + j1.00 \Omega$. The maximum DE was 83.5% at an output power of 53.8 dBm. Note that the class J amplifier shows quasi-linear gain until the transistor saturates. The drain voltage and current waveforms are illustrated in Fig. 4 at the input power of 37.0 dBm, or 1.7-dB gain compression point, where the DE was 78.0%. The current shown corresponds only to the drain current source (output capacitance component is omitted). As can be seen, the drain voltage waveform represents a quasi-half-sine-wave and has a substantial overlap with the drain current. The transistor can be assumed to be a switch at this high input power, thus the operation resembles class E. However, the zero-voltage switching (ZVS) condition is not satisfied at the turn-on instant. Generally, it is difficult to satisfy the ZVS condition over a wide drain bias range of the ET system with the constraints of a fixed conduction angle, which is determined by the gate bias, and output capacitance.

With the current design (unlike the prototype class J [11]), there is a large drop in the drain current waveform when the voltage goes close to zero. This drop in the current waveform reduces the fundamental current component and, in turn, the output power. However, it does not reduce the efficiency since the drop also decreases the dc component of current. It is found from the simulation that efficiency actually increases due to this

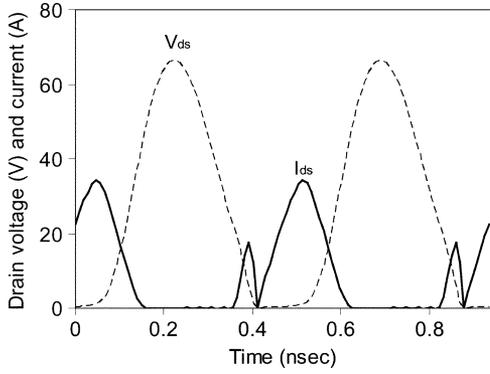


Fig. 4. Simulated drain current and drain voltage waveforms at an input power of 37.0 dBm and DE of 78.0%.

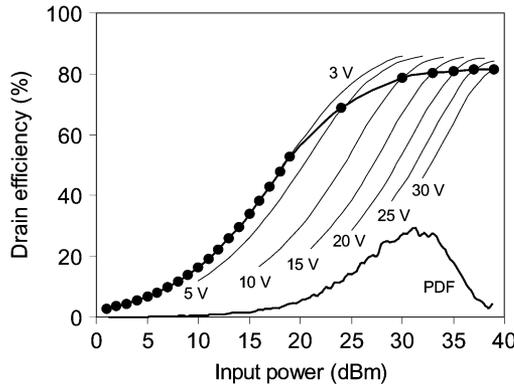


Fig. 5. DE at various drain biases as a function of input power. Dots represent the operating points under ET operation. Also shown is the probability density of W-CDMA input signal.

effect. In summary, the class J amplifier with the tuning achieved in this study provides linear performance at low input power due to the class AB bias and high efficiency at high input power due to class E-like operation.

As mentioned earlier, for high-efficiency ET operation, the RF power amplifier should provide high efficiency over a wide range of drain bias. Thus, the PDF of the input signal should be taken into account in the design of the RF amplifier. Fig. 5 illustrates the efficiency calculated at various drain biases as a function of input power together with the PDF of the W-CDMA input signal. The dots on the efficiency curves represent the operating point of the ET system obtained from the relationship between input power and drain bias. Note that the maximum drain bias was set to 30 V and the corresponding input power was 30 dBm. For input powers less than 19 dBm, the drain bias voltage was kept constant at 3 V.

As shown in this figure, the amplifier provides high efficiency over a wide range of input powers for which the probability is greatest for W-CDMA signals. This relationship results in high average efficiency for ET operation. A higher input power can be used to get higher efficiency, but it results in degraded linearity performance. The operating point represented with dots in this figure corresponds to more than 2-dB gain compression for drain bias higher than 10 V. This combination of input power and drain bias shows a simulated ACLR of 36 dB (without any additional linearization).

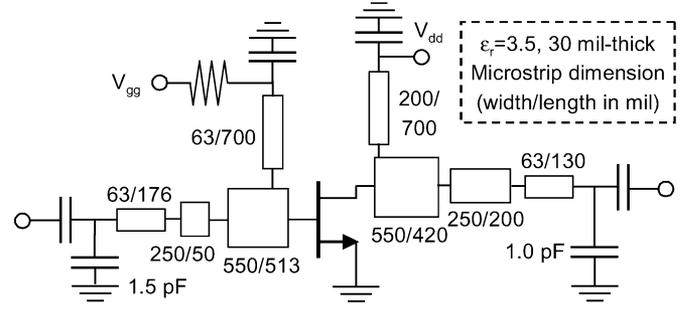


Fig. 6. Circuit schematic of RF amplifier using a 72-mm GaN HFET [6].

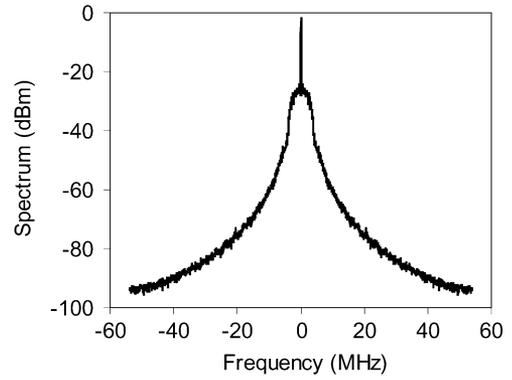


Fig. 7. Power spectrum of W-CDMA envelop signal [14].

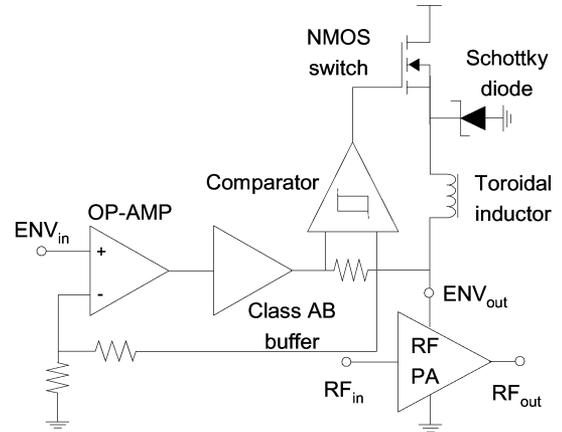


Fig. 8. Block diagram of a proposed wideband high-efficiency envelope amplifier [14].

Simulation of the overall ET system was performed using Agilent's ADS pTolomy. Drain bias was varied according to the input power from 3 to 30 V in a manner similar to the measured results using an ideal envelope amplifier (represented by a behavioral model). A de-crested WCDMA input signal with PAR of 7.67 dB and average input power of 2.0 W was used. The simulated ET power amplifier with an ideal envelope amplifier showed an average output power of 41.7 W and average DE as high as 79.8%. Note that no loss within the output matching circuit was included in the above simulations.

Experimentally, an RF power amplifier was built on a 30-mil-thick substrate, as shown in Fig. 6. To provide the proper impedance to both of the input and output of the FET,

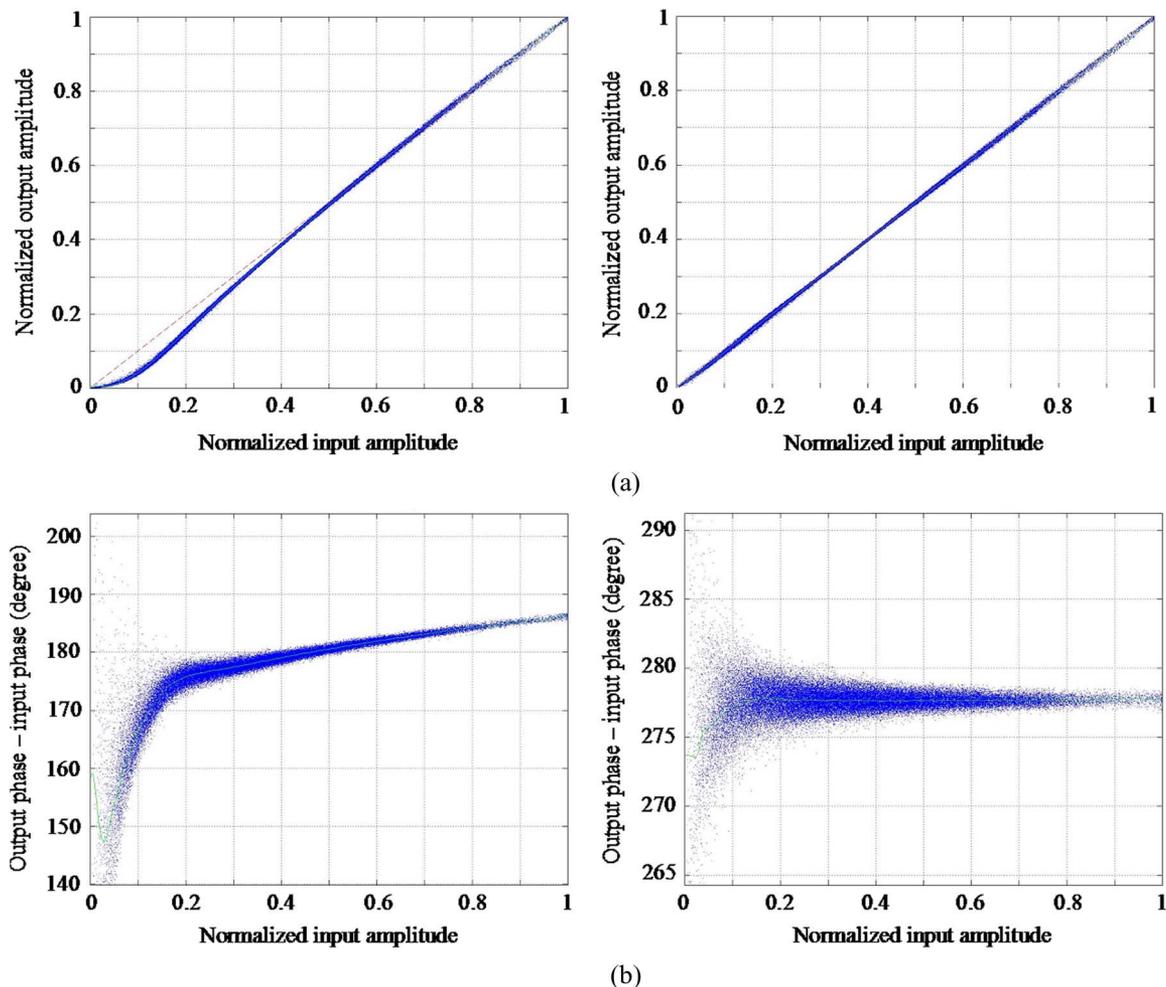


Fig. 9. Measured: (a) AM-AM performance [6] and (b) AM-PM performance. (*left*) Before pre-distortion. (*right*) After pre-distortion.

internal matching circuits were included in the Cu/W ceramic package. Impedance matching via microstrip lines and shunt capacitors was then used on the input and output to meet $50\text{-}\Omega$ terminal impedances, as shown in Fig. 6. As stated earlier, the amplifier showed a 150-W peak output power and maximum PAE of 65% under CW operation at 2.14 GHz. Note that the device temperature under CW operation will be much higher than in ET measurements, which can degrade the CW performance. When measured with constant drain voltage (and ET is not employed), the DE with fixed drain bias of 28 V was as high as 25% at -39-dBc ACLR with a WCDMA signal input (test model 1 with 64 users, PAR of 8.5 dB at 0.1% probability and 9.8 dB at 0.01% probability). The corresponding output power was 19 W and the gain was 15.0 dB at the center frequency of 2.14 GHz [5].

C. Wideband High-Efficiency Envelope Amplifier

Since the envelope signal is related to the I and Q baseband signal in nonlinear fashion, its bandwidth is larger than that of the individual I and Q signals. As a result, conventional dc-dc converters with narrow bandwidth cannot be used for this application. The power spectral density of a W-CDMA envelope

signal is shown in Fig. 7. It illustrates that nearly 85% of envelope power lies between dc and 300 kHz. This spectrum suggests a design methodology for a high-performance envelope amplifier, where dc and low-frequency power is supplied from a very efficient source, and high-frequency power is supplied from a high-fidelity source.

Based on this concept, a high-efficiency wideband envelope amplifier was developed, as shown in Fig. 8. It comprises a linear stage to provide a wideband voltage source and, in parallel, a switching stage to provide an efficient current supply based on the buck dc-dc converter topology [14]. The average switching frequency of the nMOS switch is approximately 1.28 MHz with a W-CDMA input signal. This switching frequency was optimized for best efficiency performance by changing the inductor and hysteresis value of the comparator. The output voltage of the envelope amplifier follows the input envelope signal with assistance of a linear operational amplifier with a voltage gain of 11. The current is supplied to the drain of the RF amplifier from both the linear and switching stages through a current feedback element, which senses the current flowing out of the linear stages and turns the switch on and off [14], [15]. The linear stage provides the difference between the

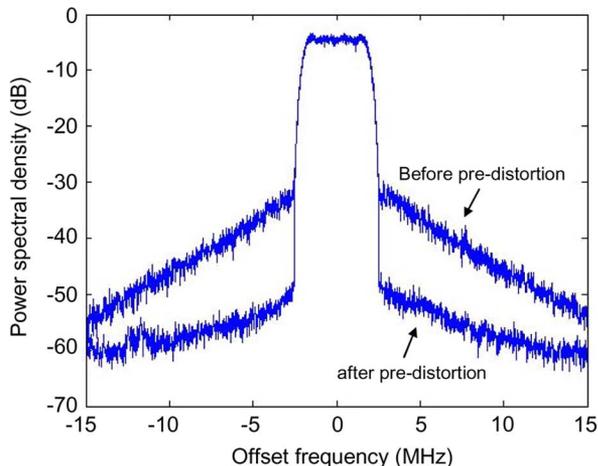


Fig. 10. Measured spectrum of W-CDMA output signal before and after digital pre-distortion [6].

desired output current and the current provided by the switching stage so that the overall error is minimized.

Measurement of the high-voltage envelope amplifier used in this study shows efficiency of 76.7% for W-CDMA signals with peak output voltage of 29.5 V and root-mean-square (rms) voltage of 13.8 V and EVM less than -41.2 dB.

III. MEASUREMENT RESULTS OF ET AMPLIFIER WITH W-CDMA SIGNALS

The overall ET amplifier was measured with single-carrier W-CDMA signals of 3.84-MHz bandwidth. The PAR of the input signals was 7.67 dB. Fig. 9 shows the measured AM-AM and AM-PM performance before and after pre-distortion. The relatively low scatter for the different values of input power indicates a low memory effect in amplitude. The overall excursion in phase (two degrees rms) indicates much lower AM-PM distortion compared to typical results with Si-LDMOS amplifiers, probably as a result of lower drain-source capacitance. As shown in this figure, digital pre-distortion is effective in linearizing the AM-AM and AM-PM characteristics. Its effect is more apparent from the measured output spectrum shown in Fig. 10, where ACLR is improved by 15.0 and 12.0 dB at 5- and 10-MHz offset, respectively, through digital pre-distortion.

The average power-added efficiency (PAE), including dissipation in the envelope amplifier, was found to be as high as 50.7% with average output power of 37.2 W. This is the highest efficiency among reported single-stage W-CDMA base-station power amplifiers. The gain and EVM were 10.0 dB and 1.74% after pre-distortion, respectively. ACLR was also measured to be -51.0 and -58.0 dBc at 5- and 10-MHz offset frequency. Table I summarizes the measured performance of the ET amplifier.

The instantaneous dc voltage and current at the output of the envelope amplifier were probed using a high-speed digitizing oscilloscope, as shown in Fig. 11, under conditions roughly comparable to those used for best efficiency, in order to verify the efficiency of the RF amplifier itself. Parasitics and limitations of the measurement system, however, caused the overall DE to drop to 45.2%. Time-delay differences between

TABLE I
SUMMARIZED PERFORMANCE OF ET POWER AMPLIFIER ACCORDING TO THE DIGITAL PRE-DISTORTION. DE: DRAIN EFFICIENCY, ACLR1 AND ACLR2: ACLR AT 5- AND 10-MHZ OFFSET, RESPECTIVELY

	Gain (dB)	P _{out} (W)	DE (%)	PAE (%)	EVM (%)	ACLR1 (dBc)	ACLR2 (dBc)
Before	10.3	36.5	51.7	49.3	12.1	-36.0	-46.0
After	10.0	37.2	53.4	50.7	1.74	-51.0	-58.0

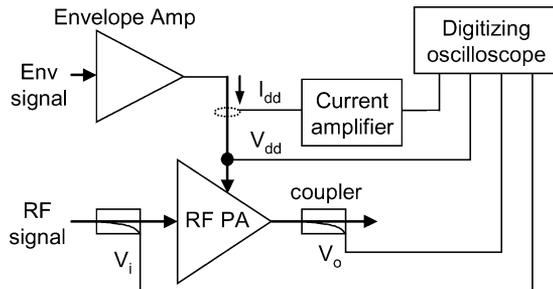


Fig. 11. Measurement of instantaneous performance of RF power amplifier.

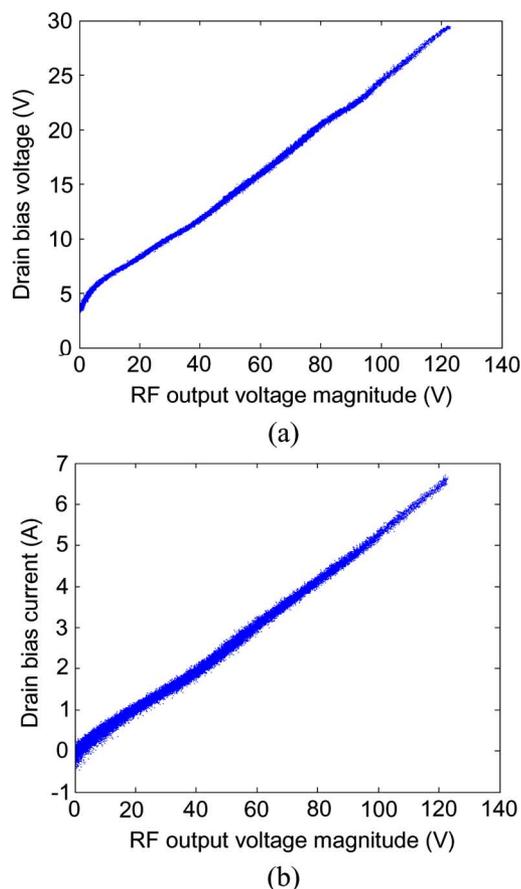


Fig. 12. Measured instantaneous: (a) drain bias voltage V_{dd} and (b) drain bias current I_{dd} versus RF output voltage magnitude.

instantaneous voltage and current waveforms were calibrated to permit accurate calculation of RF power-amplifier characteristics. Fig. 12(a) and (b) illustrates the drain bias voltage and drain bias current versus RF output voltage magnitude, respectively. Bias currents have scatter and occasional negative

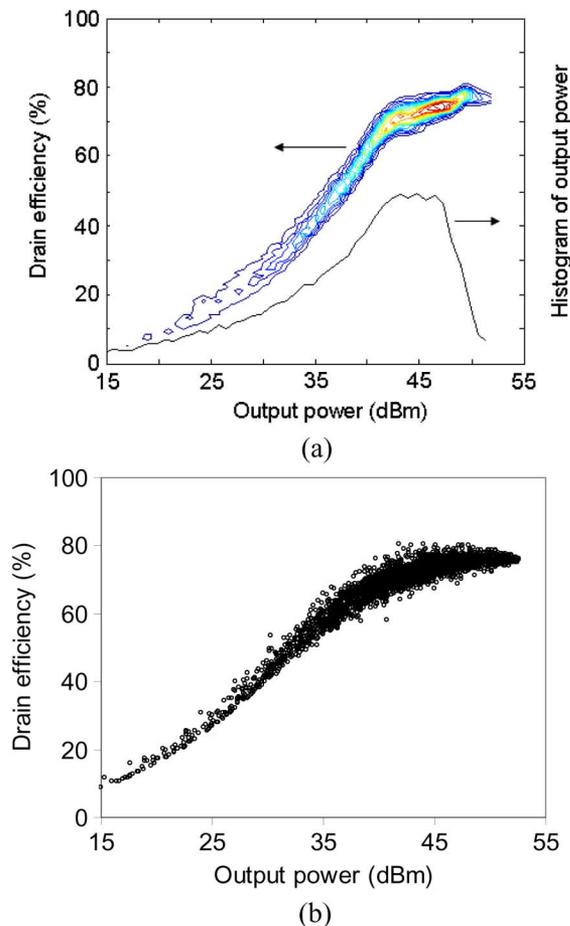


Fig. 13. (a) Contours of measured instantaneous DE of RF power amplifier as a function of output power. Also shown is a histogram of the output power for the WCDMA signal. (b) Simulated instantaneous DE of RF power amplifier as a function of output power.

values caused by the displacement current of drain capacitors. It was found that the drain impedance of the RF power amplifier is around 4.45Ω in the high drain bias range.

The measured instantaneous DE of the RF amplifier is shown in Fig. 13(a) as a function of output power. A histogram of output power for the WCDMA signal is also included. The efficiency is presented as a contour plot since the measured instantaneous values of dc and RF input power were not single-valued functions of the output power. The DE reached a maximum above 80% (as expected for a class J/E operation), and remained above 70% over a 10-dB power range, as expected from the use of ET. These measurements were carried out for an average output power of 21.6 W, for which the DE of the RF amplifier, averaged over the W-CDMA output, was calculated to be 71.2%, and corresponding PAE was 64.4%.

To further analyze the experimental results, a simulation of the ET amplifier similar to the one reported in Section II-B, including realistic estimates of the matching circuits, was used to provide the fundamental load impedance of $0.44 + j1.14 \Omega$. The simulation was found to predict the amplifier characteristics quite well, as shown in Fig. 13(b). There is some discrepancy in the simulated DE at low output power. We believe this occurred because, at the low drain biases involved, the device

model may have been inaccurate (since the model was extracted from pulsed I - V measurements at a quiescent drain voltage of 20 V and output capacitance was assumed constant with respect to drain voltage.) The simulation shows the output power of 28.8 W with DE of 73.7% PAE of 68.6%.

The dissipated power within the envelope amplifier and RF amplifier are calculated to be 16.8 and 10.8 W, respectively. For constant drain operation, the power dissipation inside the RF amplifier can be calculated to be 57.8 W from the given data in Section II-B. Therefore, the total transistor power dissipation is reduced dramatically resulting from: 1) the high-efficiency operation of the ET amplifier and 2) the fact that the generated heat is distributed between the envelope amplifier and RF amplifier. The reduced junction temperature of GaN FET is expected to improve its performance in terms of output power, as well as reliability and longevity.

IV. SUMMARY AND CONCLUSIONS

In this paper, a W-CDMA base-station power amplifier using GaN HFETs on Si substrates was presented with very high average efficiency of 50.7%, together with average output power of 37.2 W and gain of 10.0 dB. The amplifier also showed good linearity corresponding to EVM of 1.74% and good ACLR. This high efficiency and excellent linearity is attributed to the high performance of both the GaN HFET power amplifier and the envelope amplifier. Detailed waveform analysis showed that a class J/E amplifier could provide linear and high-efficiency performance for the high-power GaN device. By combining a wide-band linear stage and a high-efficiency switch stage, the envelope amplifier provided high efficiency with good signal integrity. This study has demonstrated that ET power amplifiers using GaN HFETs are promising candidates for next-generation wireless communications.

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Sandro Lanfranco, photograph and biography not available at time of publication

Walter Nagy, photograph and biography not available at time of publication

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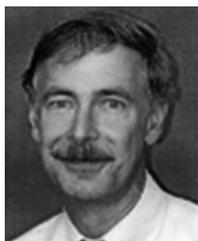
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