A High Average-Efficiency SiGe HBT Power Amplifier for WCDMA Handset Applications

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***Abstract*—The linearity of a silicon–germanium (SiGe) HBT power amplifier (PA) is analyzed with the help of a power-dependent coefficient Volterra technique. The effect of emitter inductance is included and the dominant sources of nonlinearity are identified. A dynamic current biasing technique is developed to improve the average power efficiency for wide-band code-division multiple-access (WCDMA) PAs. The average power efficiency is improved by more than a factor of two compared to a typical class-AB operation, while the power gain keeps roughly constant. The measured adjacent channel power ratio with 5- and 10-MHz offsets at 23.9-dBm average channel output power are −33 and −58.8 dBc, respectively, and satisfies the Third-Generation Partnership Project WCDMA specifications. The output power at the 1-dB compression point is 25.9 dBm.**

***Index Terms*—Average power efficiency, dynamic biasing, HBTs, intermodulation distortion, linearity, power amplifiers (PAs), Volterra series, wide-band code division multiple access (WCDMA).**

I. Introduction

In RECENT years, silicon–germanium (SiGe) has become a competitive candidate for the development of cellular handset power amplifiers (PAs) of third-generation (3G) wireless communication systems since SiGe exhibits good linearity, low-cost, and compatibility with BiCMOS technology [1]–[3], even though the SiGe HBT has a lower breakdown voltage and efficiency than its GaAs counterpart and is also affected by thermal runaway. The specifications of 3G wide-band code-division multiple-access (WCDMA) PAs are listed in Table I. To accommodate more users and maximize the usage of the spectrum in WCDMA systems, PAs have stringent limitations on linearity. PAs are also significant contributors to power consumption within mobile phones. Therefore, linearity and efficiency are the most critical parameters in the design of WCDMA handset PAs.

The linearity of RF amplifiers is usually analyzed using Volterra series. Besides providing insights into the nonlinearity mechanism, Volterra series can handle memory elements typical in the high-power amplifier [5]–[8]. To keep the analysis tractable while maintaining accuracy, Volterra series is often truncated to third order to analyze weakly nonlinear RF amplifiers operating in the class-A mode [6], [7]. On the other hand, high-efficiency code-division multiple-access (CDMA) PAs typically operate in the class-AB mode and exhibit strong nonlinearities. This renders the traditional Volterra analysis truncated to third-order inadequate and necessitates the inclusion of higher order terms, vastly increasing the complexity of the analysis. To keep the analysis tractable, and accurately predict the intermodulation distortion, we use a power-dependent coefficient Volterra technique [8]. Our analysis includes the effect of emitter bond-wire inductance, which is crucial to accurately predict the intermodulation distortion of PAs. With the help of the power-dependent coefficient Volterra technique, the dominant sources of nonlinearity in SiGe HBT PAs are highlighted.

TABLE I
3GPP WCDMA PA Specifications [4]

Specification	Value
Operating Frequency	1.92 – 1.98 GHz
Maximum Output Power	+23 dBm – +35 dBm
PAE @ Maximum Output Power	~ 30%
ACPR (3.84 MHz measured main channel)	–33 dBc @ 5 MHz offset –43 dBc @ 10 MHz offset

Average power efficiency (over the full range of output powers), instead of peak power-added efficiency (PAE), is the key factor determining the talk time and battery life for portable wireless applications [9]. Previous efforts using dynamic biasing techniques [10]–[12] achieved improved average power efficiency, but their power gains changed drastically when switched from the high-power region into the low-power region. This can create problems in the operation of the power control loop for a CDMA handset. Besides satisfying the specifications in Table I, our approach [13] substantially increases the average power efficiency, while keeping the power gain roughly constant.

In Section II, the linearity of SiGe HBT PAs is analyzed using a power-dependent coefficient Volterra technique. In Section III, we describe our dynamic current biasing (DCB) technique used in improving the average power efficiency of the WCDMA PA.

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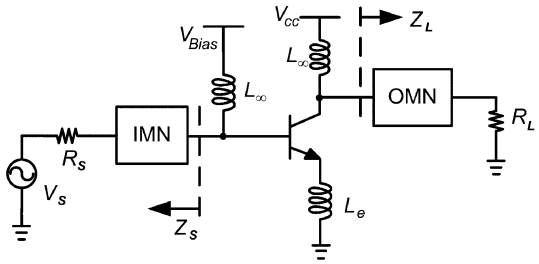

Fig. 1. Simplified schematic of a typical SiGe HBT PA.

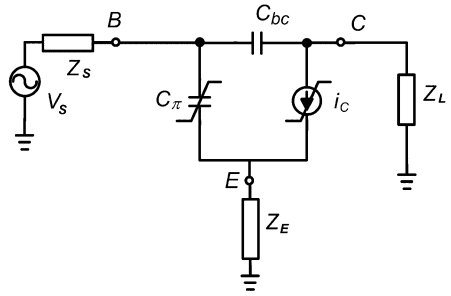

Fig. 2. Equivalent HBT nonlinear circuit for Volterra-series calculation.

In Section IV, measurement results are discussed. The conclusions are summarized in Section V.

II. Linearity Analysis of SiGe HBT PAs

A. Power-Dependent Coefficient Volterra Analysis

A simplified schematic of a typical SiGe HBT PA is shown in Fig. 1, and its equivalent nonlinear circuit for Volterra series calculation is shown in Fig. 2, where Z_S represents the source impedance, including the effects of the input matching network, bias network, and base resistance of transistors, Z_L represents the load impedance, including the effects of the output matching network (OMN), output capacitance, and conductance of transistors, and Z_E represents the emitter impedance, including the bond-wire inductance and ballasting resistance.

In our analysis, C_π and i_C are the main sources of nonlinearity, and the remaining elements are assumed linear. Our simulations show that this is an adequate model to predict the nonlinearities in our PA. Note that the nonlinear elements depend on both the quiescent bias point and RF signal power. Therefore, their values have to be determined under large-signal conditions.

For C_π, the stored charge in the base can be expressed as

$$Q_\pi = C_1 v_{\rm be} + K_{2C_\pi} v_{\rm be}^2 + K_{3C_\pi} v_{\rm be}^3. \tag{1}$$

The RF input signal determines the excursion range of the base–emitter voltage and this, together with the quiescent bias condition, determines the coefficients $C_1, K_{2C\pi}$, and $K_{3C\pi}$. The effects of the base–collector capacitance $C_{\rm bc}$ and base resistance r_b are removed in calculating these coefficients.

Similarly, the nonlinear collector current i_C can be expressed as

$$i_C = g_m v_{\rm be} + K_{2g_m} v_{\rm be}^2 + K_{3g_m} v_{\rm be}^3 \tag{2}$$

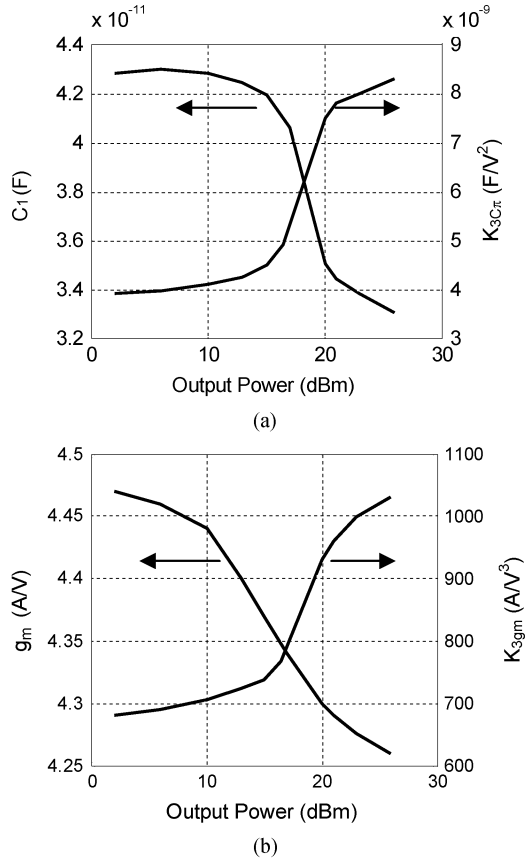

Fig. 3. Simulated nonlinearity coefficients: (a) C_1 and $K_{3C\pi}$ and (b) g_m and K_{3gm} versus output power. $I_{CQ} = 110$ mA.

where g_m, K_{2gm}, and K_{3gm} can be determined from the excursion of the base–emitter voltage together with the quiescent bias condition. The effects of capacitances and collector voltage variation are removed in calculating these coefficients.

The resulting nonlinearity coefficients $C_1, K_{3C\pi}, g_m$, and K_{3gm} are plotted in Fig. 3 for output power ranging from 0 to +26 dBm. As shown in Fig. 4, $Z_S = 0$ at even-order harmonic frequencies (including $\omega_1 - \omega_2$ and $2\omega_1$) is achieved through use of a quarter-wave stub. With this additional simplification, the nonlinear transfer function can be derived using the method of nonlinear currents described in [14] and [15] by combining (1) and (2). With the assumption, $\omega_1 \cong \omega_2$ and $\omega_1, \omega_2 \gg \omega_1 - \omega_2$, the third-order intermodulation ratio can be expressed as

$$\begin{aligned}{\rm IMR}_3 \cong{}& \frac{3}{4} A_{v{\rm be}}^2(\omega_1) A_{v{\rm be}}(-\omega_2) \\ &\times \Big\{ K_{3C_\pi} \left[j\omega_1 Z_E + j\omega_1 Z_S + \omega_1^2 C_{\rm bc} Z_S / g_m \right] \\ &\quad - K_{3g_m}/g_m \left[1 + j\omega_1 C_1 Z_E \right. \\ &\qquad \left. + j\omega_1 (C_1 + C_{\rm bc}) Z_S \right] \Big\} \cdot v_S^2 \end{aligned} \tag{3}$$

where $A_{v{\rm be}}(\omega_1)$ and $A_{v{\rm be}}(-\omega_2)$ are the matching network voltage gains from the source to the base–emitter at frequencies ω_1 and $-\omega_2$, respectively. Detailed derivations of the expressions for $A_{v{\rm be}}(\omega_1)$, $A_{v{\rm be}}(-\omega_2)$ and ${\rm IMR}_3$ are described in the Appendix.

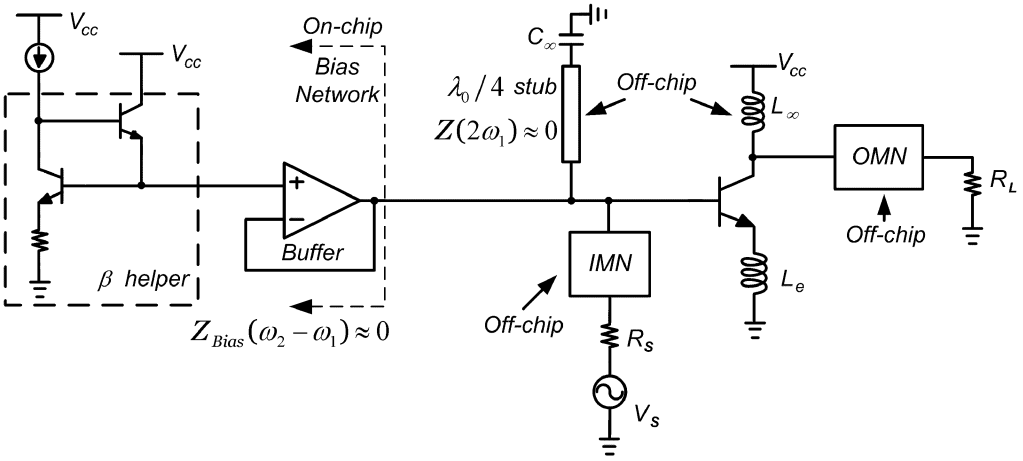

Fig. 4. Schematic of circuit used for experimental verification of linearity analysis.

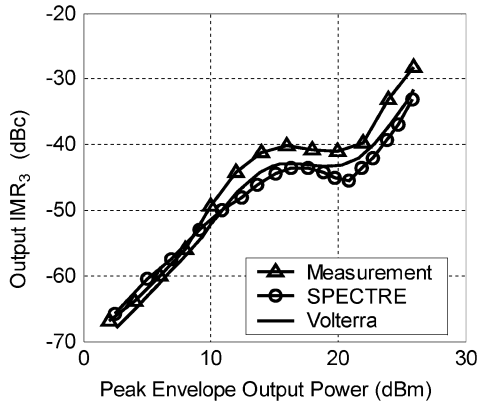

Fig. 5. IMR_3 comparison between SPECTRE simulation, Volterra calculation, and measurement for the circuit of Fig. 4.

B. Experimental Verification of Analysis

The single-stage PA shown in Fig. 4 was fabricated in a 0.25-μm SiGe BiCMOS process.[1] The main bipolar transistors in the PA are composed of 100 devices, each with an emitter area of 48 $\mu\mathrm{m} \times 0.44$ μm. The devices were packaged in the Amkor micro-lead-frame (MLF) package. The chip was mounted on a Rogers20 printed circuit board (PCB). The quiescent bias current at the collector is 110 mA.

A comparison of IMR_3 obtained from experimental measurements with our Volterra expression in (3) shows good agreement throughout the entire range of output powers from 0 to +26 dBm (Fig. 5). In addition, the excellent agreement of IMR_3 between SPECTRE simulations and our Volterra expression validates the completeness of our model shown in Fig. 2 and the corresponding extraction methodology described in Section II-A.

Our analysis not only accurately predicts the IMR_3, but also provides insight into the individual contributions from the main nonlinear sources. Fig. 6 displays the calculated amplitude and phase of IMR_3 in the following three cases.

Case 1) With the effect of the nonlinearity of C_π only $(K_{3gm} = 0)$.

[1]IBM 6HP BiCMOS Process. [Online]. Available: http://www-3.ibm.com/chips/techlib/techlib.nsf/products/BiCMOS_6HP

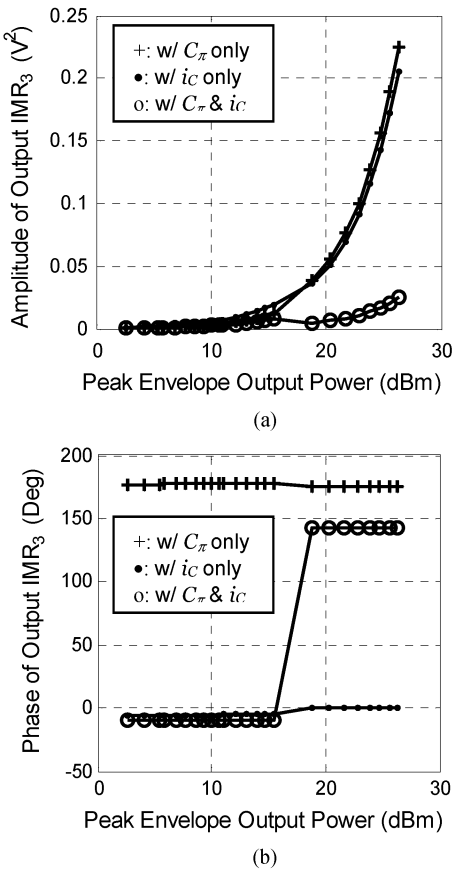

Fig. 6. Individual contributions to amplitude and phase of output IMR_3. Note that the jump in the phase of output IMR_3 comes from the fact that, at low input powers, the nonlinearity of i_C dominates the phase of output IMR_3, whereas at high input powers, the C_π nonlinearity dominates the phase of output IMR_3: (a) amplitude of IMR_3 and (b) phase of IMR_3

Case 2) With the effect of the nonlinearity of i_C only $(K_{3C\pi} = 0)$.

Case 3) With the effects of the nonlinearities of C_π and i_C together.

We observed that the nonlinearity of C_π and nonlinearity of i_C are quite large over the whole power range, but they are opposite in phase, resulting in the well-known intermodulation cancellation effect [16]. At low input powers, the nonlinearity of i_C

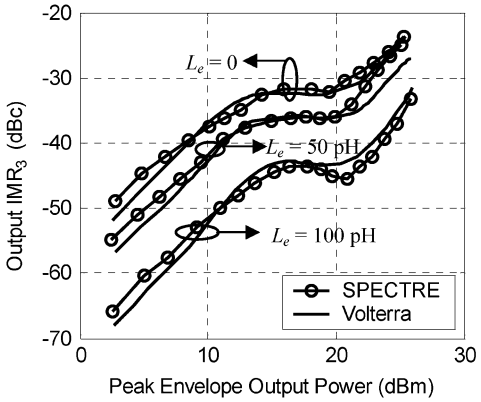

Fig. 7. IMR_3 with different values of L_e, $I_{CQ} = 110$ mA.

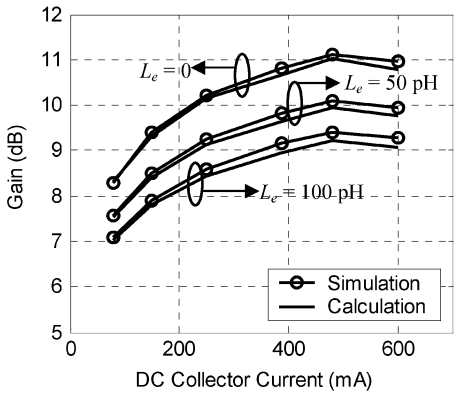

Fig. 8. Comparison of simulated and calculated power gains with different values of L_e.

dominates the magnitude and the phase of output IMR_3. The C_π nonlinearity dominates at high input powers so that the output IMR_3 is determined by the C_π nonlinearity.

The overall linearity of the SiGe HBT PA depends on the degree to which this cancellation is achieved [17]. Furthermore, the linearity is also limited due to considerations of power gain and efficiency.

C. Effect of Emitter Bond-Wire Inductance

The effect of bond wires connected to the emitter of the PA is critical in the design of the PA. Without considering its effect, the power gain and linearity cannot be accurately predicted. Therefore, it is necessary to include its effect in our linearity analysis.

Expression (3) was compared to SPECTRE simulations for different values of the bond-wire inductance, as shown in Fig. 7. From this figure, we observed that the linearity of the PA is improved with the increase of the bond-wire inductance L_e. Obviously, it may not be possible to pursue the best linearity by continuously increasing the value of L_e due to the reductions in gain and PAE.

The effect of L_e on power gain is demonstrated in Fig. 8, where three different values of L_e are compared. Calculation results are based on (4), which is the complete expression for power gain of the amplifier (including the effects of source

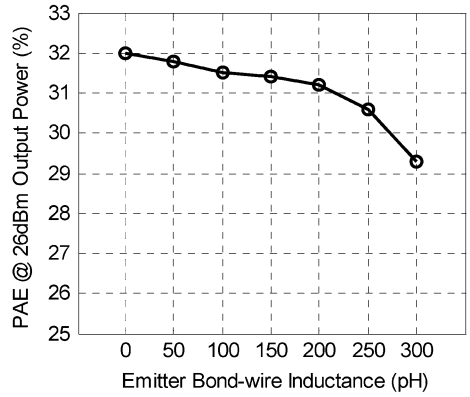

Fig. 9. Simulated PAEs at 26-dBm output power with different values of L_e.

impedance Z_L, load impedance Z_s, and bond-wire inductance L_e)

$$G_p \cong \frac{4Z_S Z_L}{\omega^2\left(L_e + \dfrac{Z_S}{\omega_T} + Z_S C_{\mathrm{bc}} Z_L\right)^2 + \omega^4 L_e^2 C_{\mathrm{bc}}^2 Z_S^2} \tag{4}$$

where the base resistance r_b is included in Z_S, $g_m = \omega_T \cdot C_\pi$, in which ω_T is the unity current gain radian frequency, C_π is the total capacitance between the base and emitter, and C_{bc} is the base–collector capacitance. All circuit parameters used in (4) are extracted at the corresponding bias point from SPECTRE simulation. Note that the power gain is very sensitive to the effect of L_e.

The effect of L_e on PAE is illustrated in Fig. 9, where PAEs at 26-dBm output power are compared with different values of L_e. The effect of emitter inductance on PAE is not as significant as its effect on power gain, but we can still observe that, with an increase of L_e, the power gain decreases and, thus, so does the PAE. This can be seen from the following definition of PAE [18]:

$$\mathrm{PAE} = \frac{P_{\mathrm{out}} - P_{\mathrm{in}}}{P_{\mathrm{dc}}} = \frac{P_{\mathrm{out}}}{P_{\mathrm{dc}}}\left(1 - \frac{1}{G}\right). \tag{5}$$

For WCDMA PAs, it is always desirable to have the power gain and PAE as high as possible, while satisfying the linearity requirement. For our PA, we found that 80 pH is the optimum value for bond-wire inductance L_e, considering the tradeoff between gain, linearity, and efficiency.

III. Efficiency Enhancement Technique

A. Average Power Efficiency

The average power efficiency is a measure of the ratio of the total energy transmitted to the total energy drawn from the battery [9], i.e.,

$$\langle \eta \rangle = \frac{\langle P_{\mathrm{out}} \rangle}{\langle P_{\mathrm{dc}} \rangle} = \frac{\int P_{\mathrm{out}} p(P_{\mathrm{out}}) dP_{\mathrm{out}}}{\int \dfrac{P_{\mathrm{out}} p(P_{\mathrm{out}}) dP_{\mathrm{out}}}{\eta(P_{\mathrm{out}})}} \tag{6}$$

where P_{out} is the output power, $p(P_{\mathrm{out}})$ is the probability of a certain output power P_{out}, and $\eta(P_{\mathrm{out}})$ is the PAE at P_{out}.

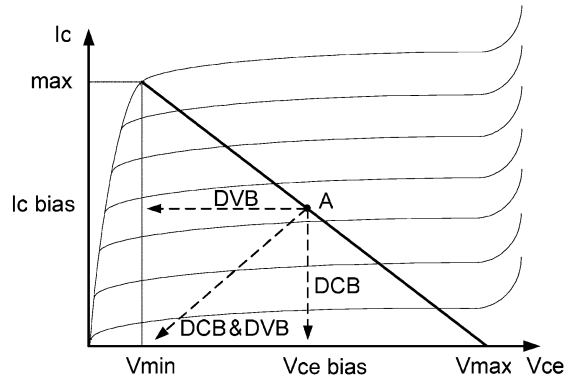

Fig. 10. Bipolar junction transistor (BJT) current versus voltage, demonstrating different dynamic biasing strategies (DCB/DVB).

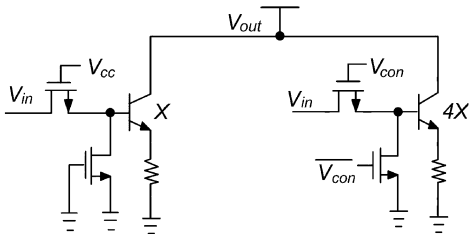

Fig. 11. Output stage transistors with DCB. HBTs are biased "on" or "off" in response to output power requirements.

The average output power of a CDMA handset is well below the peak output power, where efficiency is a maximum, so it is very desirable to improve the PAEs of the amplifier at lower output powers. For class-A PAs, the average power efficiency (over representative CDMA conditions) is roughly 1.3% [19]. Therefore, improving average power efficiency is one of the key objectives for future PAs.

B. DCB

The typical approaches for reducing dc power consumption at lower output powers are reducing either dc-bias current through DCB or dc bias voltage (DVB) or both, as shown in Fig. 10.

Power amplifiers with DCB have been proposed [10], [11], but their power gain changes by more than 8 dB with the change in dc-bias current. With the decrease of input power, the current swing at the output also becomes smaller and the total bias current can be reduced. However, the current density of each transistor drops, resulting in a reduction of power gain for the whole PA. With $L_e = 0$, the power gain of the PA can be simplified as

$$G_p \cong \frac{4}{Z_S} \cdot \left(\frac{\omega_T}{\omega}\right)^2 \cdot \frac{Z_L}{(1+\omega_T Z_L C_{\rm bc})^2}. \tag{7}$$

From (7), it is clear that, in order to maintain a constant power gain, we need to operate the transistor at a constant f_T. Therefore, the transistor should operate at a constant current density.

To lower the collector current and keep the power gain roughly constant, we utilize low-loss MOS switches at the bases of the transistors and dynamically bias the SiGe HBTs either fully "on" or fully "off" [20], as depicted in Fig. 11.

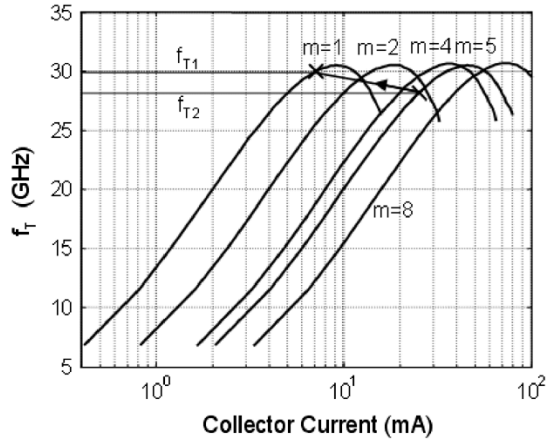

Fig. 12. Simulated HBT cutoff frequency versus collector current with differing device sizes (single device: 25 μm^2; m represents the number of devices in parallel).

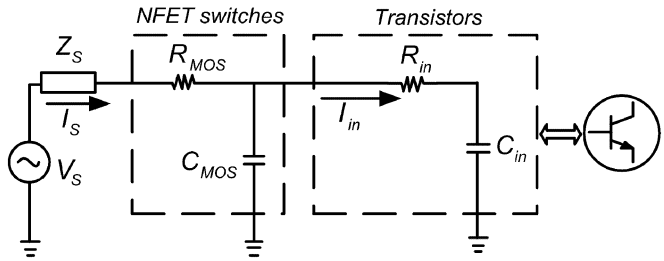

Fig. 13. Equivalent input circuit including NFET switches. For 100 parallel devices, $R_{\rm MOS} = 0.3\ \Omega$, $C_{\rm MOS} = 3.26$ pF, $R_{\rm in} = 1\ \Omega$, and $C_{\rm in} = 204$ pF.

The number of "on" transistors is adjusted in response to changes in the desired output power; the collector current density is increased slightly at the low-power region so as to keep the power gain constant. As shown in Fig. 12, the PA is operated at a slightly higher transition frequency (f_{T1}) in the low power mode than in the higher power mode (f_{T2}). Operating the transistor at this higher f_{T1} enables us to keep the gain relatively constant by overcoming the effects of the extra parasitics in the low power mode.

C. Design Considerations

Ideally, for each output power, the dc-bias current could be adjusted to achieve maximum power efficiency. However, it is simpler to vary the current in discrete finite steps. Simulation results show that a single step variation in dc bias provides the best tradeoff of average power efficiency and circuit complexity. In our case, the high-power mode consisted of 100 parallel devices, and the low-power mode consisted of 20 devices. Each device consists of a bipolar transistor with an emitter area 48 μm $\times$ 0.44 μm.

The simplified equivalent input circuit is shown in Fig. 13. There are two sources of power loss due to the n-type field-effect transistor (NFET) switches—resistance loss (ΔGain_$R_{\rm MOS}$) and capacitance loss (ΔGain_$C_{\rm MOS}$). The gain loss can be expressed as

$$\Delta{\rm Gain} \cong \Delta{\rm Gain\_}R_{\rm MOS} + \Delta{\rm Gain\_}C_{\rm MOS} \tag{8a}$$

$$\approx 10\log\frac{R_{\rm in}^2}{(R_{\rm MOS}+R_{\rm in})^2}. \tag{8b}$$

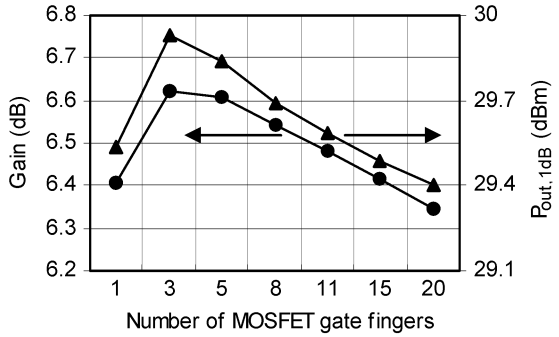

Fig. 14. Effects of gate finger on gain and 1-dB compression. Each finger is 15 μm $\times$ 0.25 μm finger and the HBT is 48 μm $\times$ 0.44 μm.

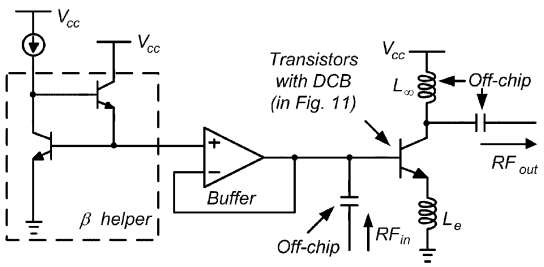

Fig. 15. PA schematic. An op-amp-based dc-bias circuit provides a low impedance at the baseband frequency.

Based on calculation using parameters extracted from simulation (in Fig. 13), capacitance loss (ΔGain_$C_{\rm MOS}$) is insignificant compared to resistance loss (ΔGain_$R_{\rm MOS}$).

The effects of the NFET switch size on both the power gain and 1-dB compression point of the PA were simulated. The results are shown in Fig. 14. Based on the simulation results that match the expression in (8b), an optimum MOS switch size of 3 finger $\times$ 15 μm $\times$ 0.26 μm was chosen. The corresponding gain loss at 1.95 GHz was 2.5 dB.

The bias network consists of a β helper and a low-impedance buffer, as shown in Fig. 15. This topology provides a *CV* biasing to the base of the PA and also terminates the sub-harmonic ($\Delta\omega$) frequency at the input to improve the overall linearity [21]. In order to effectively terminate the sub-harmonic component, the buffer needs to satisfy certain bandwidth requirement. For WCDMA handset PAs, the channel bandwidth is 3.84 MHz, thus, the minimum bandwidth of the bias network has to be larger than 3.84 MHz. Simulations show $Z_{\rm bias}(\Delta\omega) \approx 0$ for $\Delta\omega \leq 5$ MHz. The even-order harmonics are terminated by using a quarter-wave stub connected to the base of transistors on the testing PCB board, which, for simplicity, is not shown in Fig. 15.

IV. Experimental Results and Discussions

For WCDMA PAs, a two-stage topology is normally needed. In this study, we focus on the output stage, which is the key bottleneck in designing high-efficiency PAs. The first stage can be designed in a straightforward way.

The single-stage PA with DCB for WCDMA handset applications was fabricated in the 0.25-μm SiGe BiCMOS process used for the circuit of Fig. 4. The chip size, including the bias network, is 0.9 mm $\times$ 1.2 mm. The die photograph is shown in Fig. 16. The devices were tested in MLF (MLF12) packages. The OMN is implemented off-chip to achieve high Q for optimum PAE.

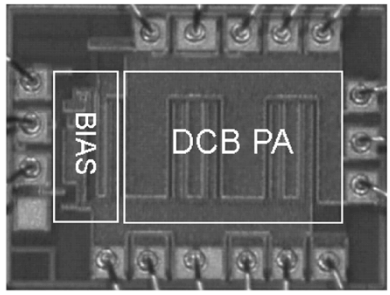

Fig. 16. DCB SiGe HBT PA.

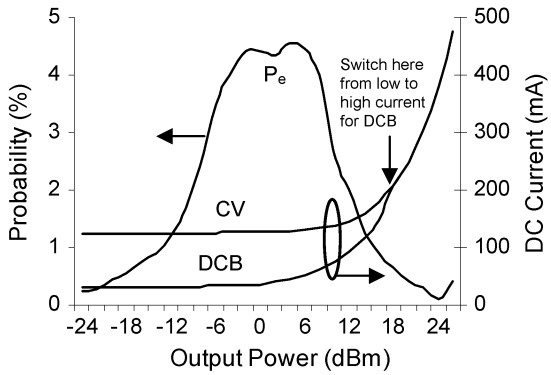

Fig. 17. Output power probability distribution P_e and measured dc current for different biasing techniques. The switch point from 100 devices to 20 devices occurs at $P_{\rm out} = 18$ dBm. $V_{CC} = 3$ V.

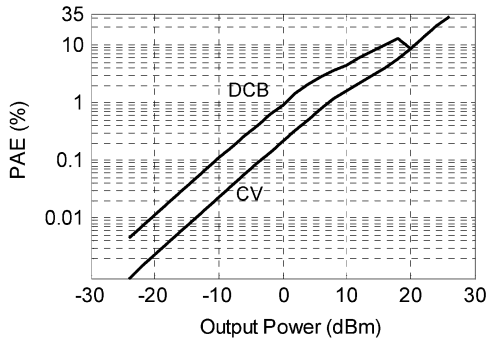

Fig. 18. Measured PAEs with *CV* with fixed area (*CV*) and DCB with varied area (DCB) PAs.

Fig. 17 compares the measured dc currents for different biasing approaches for a single-stage WCDMA PA, superimposed on a typical probability distribution function for the output power [19]. These approaches include constant base voltage (*CV*) biasing with a fixed number of parallel transistors and DCB with a fixed base voltage. Using (6), average power efficiencies are calculated as 2.5% for *CV* biasing and 8.0% for DCB—a substantial improvement with the new approach.

Fig. 18 shows measured PAEs with DCB and *CV* approaches. The peak PAE is not as high as other III–V WCDMA amplifiers reported [22], but the average power efficiency is improved. Table II is a summary of average power efficiencies for different reported dynamic biasing techniques, including this study.

TABLE II
AVERAGE POWER-EFFICIENCY COMPARISON OF REPORTED DYNAMIC BIASING TECHNIQUES

Techniques	Fixed biasing efficiency	Dynamic biasing efficiency
GaAs MESFET PA with DVB[1] [12]	3.89%	6.38%
AlGaAs/InGaAs MESFET PA with DVB [23][2]	2.2%	11.4%
LDMOS PA with DVB [24][2]	1.53%	6.78%
GaAs HBT PA with DCB[3] [11]	2.50%	4.03%
SiGe HBT PA with DCB in this work	**2.50%**	**8.08%**

[1]Dynamic voltage biasing
[2]Output power distribution probability function used in [23] and [24] is different from that used in this work
[3]Dynamic current biasing

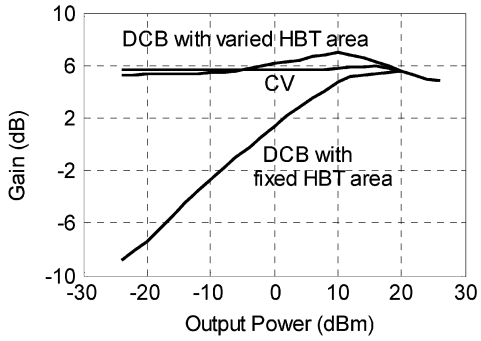

Fig. 19. Measured power gains with *CV* with constant area (*CV*), DCB with varied HBT area, and DCB with fixed HBT area PAs.

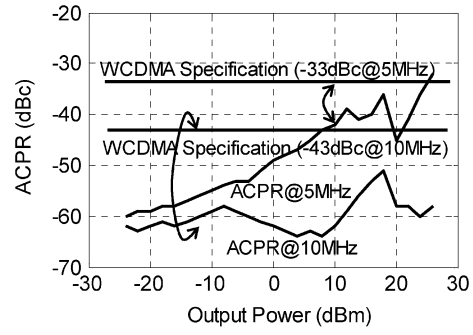

Fig. 20. Measured ACPRs of DCB SiGe HBT PA.

Fig. 19 compares the measured gain variation between a DCB with a varied HBT area, a DCB with a fixed HBT area, and *CV* with a fixed HBT area. The gain change for a DCB with a varied HBT area is less than 2 dB, and is much more constant than a DCB with a fixed HBT area [10], [11].

The linearity of the DCB amplifier is measured under adjacent channel power ratio (ACPR) testing with a WCDMA signal. The corresponding simulated ACPR curve is not compared here because the simulation of the ACPR in the Cadence design environment is very time consuming and the ACPR may be easily derived from IMR_3 [25], [26]. As shown in Fig. 20, the circuit satisfies the 3GPP class-3 WCDMA ACPR specification with 23.9-dBm channel output power.

V. CONCLUSION

This paper has used a power-dependent coefficient Volterra technique to analyze the linearity of SiGe HBT PAs. The analyzed model has taken into account the effect of emitter bondwire inductance. The comparison of IMR_3 between analysis, simulation, and measurement data has validated this approach. The main sources of nonlinearity in SiGe HBT PAs have been highlighted. The authors have also developed a DCB technique to improve the average power efficiency for PAs. A prototype chip with a DCB for WCDMA applications has been fabricated and measured. The measured 1-dB compression point is 25.9 dBm, and the peak PAE is 31%. The average power efficiency has been improved from 2.5% to 8.0% by more than a factor of two using the DCB technique, while the power gain has been kept almost constant. The PA has also satisfied the ACPR specification for linearity.

APPENDIX

Here, we derive (3) in detail using the method of nonlinear currents described in [14] and [15].

The fundamental responses of the collector voltage and base–emitter voltage are found to be

$$v_C(\omega_1) = \frac{(-g_m + j\omega_1 C_{\mathrm{bc}} - j\omega_1^3 C_1 C_{\mathrm{bc}} L_e) Z_L}{\det(\omega_1)} v_S \tag{9a}$$

$$\cong \frac{-g_m Z_L}{\det(\omega_1)} v_S \tag{9b}$$

$$v_{\mathrm{be}}(\omega_1) = \frac{1 + j\omega_1 C_{\mathrm{bc}} Z_L}{\det(\omega_1)} v_S \tag{10a}$$

$$= A_{v\mathrm{be}}(\omega_1) \cdot v_S \tag{10b}$$

where

$$\begin{aligned}\det(\omega_1) &= 1 - \omega_1^2 (C_1 C_{\mathrm{bc}} Z_E Z_L + C_1 C_{\mathrm{bc}} Z_E Z_S + C_1 C_{\mathrm{bc}} Z_L Z_S) \\ &\quad + g_m Z_E + j\omega_1 [C_1 Z_E + C_{\mathrm{bc}} Z_L + C_1 Z_S + C_{\mathrm{bc}} Z_S \\ &\qquad + C_{\mathrm{bc}} g_m Z_E Z_L + C_{\mathrm{bc}} g_m Z_E Z_S \\ &\qquad + C_{\mathrm{bc}} g_m Z_L Z_S]\end{aligned} \tag{11}$$

in which Z_E, Z_S, and Z_L are evaluated at the frequency ω_1.

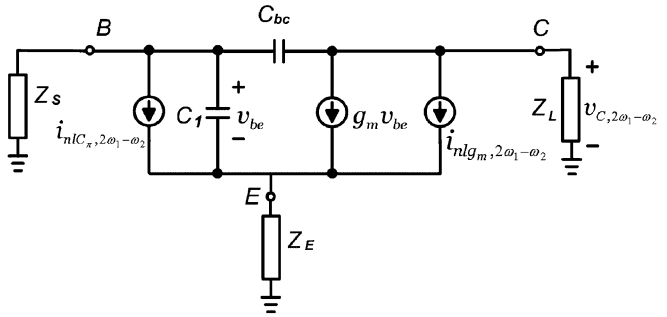

Fig. 21. Equivalent circuit for the computation of the third-order intermodulation product $2\omega_1 - \omega_2$.

The response of the base–emitter voltage at ω_2 is given by

$$v_{\rm be}(-\omega_2) = v_{\rm be}^*(\omega_2) = \frac{1 - j\omega_2 C_{\rm bc} Z_L^*}{\det^*(\omega_2)} v_S \tag{12a}$$

$$= A_{v\rm be}(-\omega_2) \cdot v_S \tag{12b}$$

in which Z_E, Z_S, and Z_L are evaluated at the frequency ω_2.

Since $Z_S = 0$ at even-order harmonic frequencies (including $\omega_1 - \omega_2$ and $2\omega_1$), there is no need to compute the second-order responses.

Now we can calculate the third-order intermodulation product at $2\omega_1 - \omega_2$. The equivalent circuit for its computation is shown in Fig. 21.

From [15], we find

$$i_{nlC_\pi,2\omega_1-\omega_2} = j(2\omega_1 - \omega_2) \cdot \frac{3}{4} K_{3C_\pi} v_{\rm be}^2(\omega_1) v_{\rm be}(-\omega_2) \tag{13a}$$

$$\cong j\omega_1 \cdot \frac{3}{4} K_{3C_\pi} A_{v\rm be}^2(\omega_1) A_{v\rm be}(-\omega_2) \cdot v_S^3 \tag{13b}$$

$$i_{nlg_m,2\omega_1-\omega_2} = \frac{3}{4} K_{3g_m} v_{\rm be}^2(\omega_1) v_{\rm be}(-\omega_2) \tag{14a}$$

$$= \frac{3}{4} K_{3g_m} A_{v\rm be}^2(\omega_1) A_{v\rm be}(-\omega_2) \cdot v_S^3 \tag{14b}$$

By applying Kirchoff's law in the circuit of Fig. 21, we find that

$$v_C(2\omega_1 - \omega_2) = \frac{Z_L}{\det(2\omega_1 - \omega_2)} \times \Big\{ i_{nlC_\pi,2\omega_1-\omega_2} \big[-j(2\omega_1 - \omega_2) C_{\rm bc} Z_S + g_m(Z_E + Z_S) \big] - i_{nlg_m,2\omega_1-\omega_2} \big[1 + j(2\omega_1 - \omega_2) C_{\rm bc} Z_S + j(2\omega_1 - \omega_2) C_1 (Z_E + Z_S) \big] \Big\} \tag{15}$$

in which Z_E, Z_S, and Z_L are evaluated at the frequency $2\omega_1 - \omega_2$.

Since $\omega_1 \gg \omega_1 - \omega_2$ and $2\omega_1 - \omega_2 \cong \omega_1$, Z_E, Z_S, and Z_L evaluated at the frequency $2\omega_1 - \omega_2$ are approximately equal to Z_E, Z_S, and Z_L evaluated at the frequency ω_1, respectively. Then $\det(2\omega_1 - \omega_2) \cong \det(\omega_1)$.

Substituting the expressions of the nonlinear currents (13b) and (14b) into (15) yields the final intermodulation product

$$v_C(2\omega_1 - \omega_2) \cong \frac{Z_L}{\det(\omega_1)} \frac{3}{4} A_{v\rm be}^2(\omega_1) A_{v\rm be}(-\omega_2) \times \Big\{ j\omega_1 K_{3C_\pi} \big[-j\omega_1 C_{\rm bc} Z_S + g_m(Z_E + Z_S) \big] - K_{3g_m} \big[1 + j\omega_1 C_{\rm bc} Z_S + j\omega_1 C_1 (Z_E + Z_S) \big] \Big\} \cdot v_S^3. \tag{16}$$

The ratio of the third-order intermodulation product and the fundamental at the collector is then found to be

$$\mathrm{IMR}_3 = \frac{v_C(2\omega_1 - \omega_2)}{v_C(\omega_1)} \cong \frac{3}{4} A_{v\rm be}^2(\omega_1) A_{v\rm be}(-\omega_2) \times \Big\{ K_{3C_\pi} \big[j\omega_1 Z_E + j\omega_1 Z_S + \omega_1^2 C_{\rm bc} Z_S / g_m \big] - K_{3g_m}/g_m \big[1 + j\omega_1 C_1 Z_E + j\omega_1 (C_1 + C_{\rm bc}) Z_S \big] \Big\} \cdot v_S^2. \tag{17}$$

Since the OMN is a linear passive network, (17) is also valid for the ratio of the third-order intermodulation product and the fundamental at the output load.

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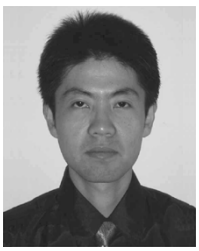

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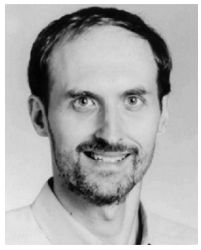

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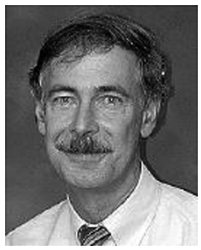

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