Modified Derivative Superposition Method for Linearizing FET Low-Noise Amplifiers

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***Abstract*—Intermodulation distortion in field-effect transistors (FETs) at RF frequencies is analyzed using the Volterra-series analysis. The degrading effect of the circuit reactances on the maximum IIP_3 in the conventional derivative-superposition (DS) method is explained. The noise performance of this method is also analyzed and the effect of the subthreshold biasing of one of the FETs on the noise figure (NF) is shown. A modified DS method is proposed to increase the maximum IIP_3 at RF. It was used in a 0.25-μm Si CMOS low-noise amplifier (LNA) designed for cellular code-division multiple-access receivers. The LNA achieved $+22$-dBm IIP_3 with 15.5-dB gain, 1.65-dB NF, and 9.3 mA@2.6-V power consumption.**

***Index Terms*—Amplifier noise, intermodulation distortion, MOSFET amplifiers, nonlinearities, Volterra series.**

I. Introduction

THE SINGLE-TONE desensitization requirement for code-division multiple-access (CDMA) phones demands a very high linearity of the low-noise amplifier (LNA) to reduce its cross-modulation distortion of a single-tone jammer in the presence of a transmitted signal leakage [1]. The high linearity should be achieved in combination with a low noise figure (NF), high gain, and low current consumption. The LNA linearity is usually specified as an input-referred third-order intercept point (IIP_3). For example, a typical cellular CDMA LNA must have $\mathrm{IIP}_3 \geq +8$ dBm, a nominal NF of 1.6 dB, and power gain of 16 dB with the power consumption less than 30 mW. This design challenge requires the use of linearization techniques.

As was shown in [2], the linearity of an Si bipolar junction transistor (BJT) or an SiGe HBT can be reliably improved using a simple technique based on low-frequency low-impedance base termination without degrading gain or NF. However, this technique is not effective for linearizing field-effect transistor (FET) amplifiers. In [3], feed-forward distortion cancellation was proposed to achieve a very high IIP_3 of a CMOS LNA. This technique relies on accurate scaling between the input signals of the main and auxiliary gain stages and their transfer functions. The results demonstrated in [3] were measured using a coaxial assembly to split and attenuate the input signal for the main and auxiliary gain stages; thus, the feasibility of this approach for practical applications is questionable.

An FET can also be linearized by biasing at a gate–source voltage (V_{GS}) at which the third-order derivative of its dc transfer characteristic is zero [4]–[7]. The resulting IIP_3 peaks in a very narrow range of V_{GS} making this technique sensitive to bias variations. To reduce the IIP_3 sensitivity to the bias, the derivative superposition (DS) method was proposed in [8]. It uses two or more parallel FETs of different widths and gate biases to achieve a composite dc transfer characteristic with an extended V_{GS} range in which the third-order derivative is close to zero. However, the IIP_3 improvement in this method is only modest at RF (3 dB, as reported in [9]). Reducing the source degeneration inductance and drain load impedance at the second harmonic frequency of the composite input transistor allowed the authors of [10] to boost IIP_3 in the DS method by as much as 10 dB. However, a small degeneration inductance prevents a simultaneous noise-power input match leading to a higher NF. This NF increase comes in addition to an intrinsically higher NF of a composite FET in comparison with a single FET (higher by 0.6 dB, as reported in [10]). This NF increase due to replacing a single FET by a composite FET in the DS method is not predicted by simulations using BSIM3v3 models.

Here, we explain the poor IIP_3 performance of the conventional DS method at RF based on the Volterra-series analysis. We also explain the higher NF resulting from the use of this method. We propose a modified DS method to achieve a very high IIP_3 at RF. Its principle of operation is explained based on the Volterra-series analysis. A cellular CDMA 0.25-μm CMOS LNA using this method is described. The measured data is presented to confirm the analytical results.

II. DC Theory of DS Method

Consider a common-source FET biased in saturation. Its small-signal output current can be expanded into the following power series in terms of the small-signal gate–source voltage v_{gs} around the bias point

$$i_d(v_{\mathrm{gs}}) = g_1 v_{\mathrm{gs}} + g_2 v_{\mathrm{gs}}^2 + g_3 v_{\mathrm{gs}}^3 + \cdots \tag{1}$$

where g_1 is the small-signal transconductance and the higher order coefficients (g_2, g_3, etc.) define the strengths of the corresponding nonlinearities. Among these coefficients, g_3 is particularly important because it controls the third-order intermodulation distortion (IMD_3) at low signal levels and, thus, determines IIP_3. The input tone amplitude at the intercept point is given by [16]

$$A_{\mathrm{IP3}} = \sqrt{\frac{4}{3}\left|\frac{g_1}{g_3}\right|}. \tag{2}$$

The power series coefficients generally depend on the dc gate–source and drain–source voltages V_{GS} and V_{DS}. However,

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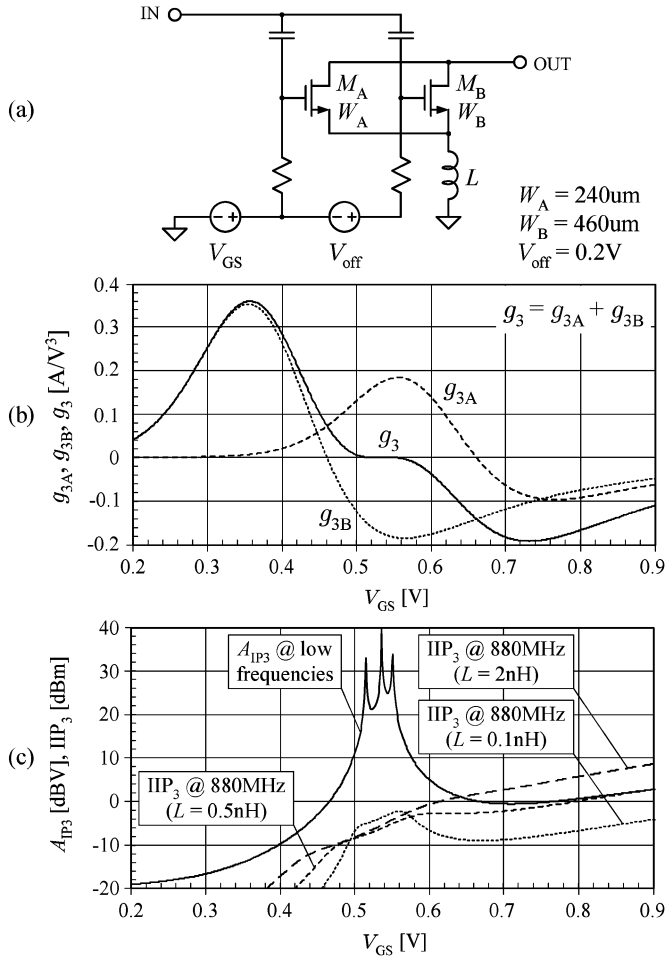

Fig. 1. DS method. (a) Composite FET. (b) Third-order power series coefficients. (c) Theoretical A_{IP3} at dc and IIP_3 at 880 MHz. Note that the bondwire inductance reduces the improvement in IIP_3 at the optimum gate biases at high frequencies.

the dependence on V_{DS} for an FET in saturation can be neglected. The coefficients of (1) can then be found as

$$g_1 = \frac{\partial I_D}{\partial V_{\mathrm{GS}}} \quad g_2 = \frac{1}{2}\frac{\partial^2 I_D}{\partial V_{\mathrm{GS}}} \quad g_3 = \frac{1}{6}\frac{\partial^3 I_D}{\partial V_{\mathrm{GS}}}. \tag{3}$$

The dependence of g_3 on V_{GS} is such that g_3 changes from positive to negative when V_{GS} transitions from the weak and moderate inversion regions to the strong inversion (SI) region [7]. If a positive g_3 with a certain $g_3(V_{\mathrm{GS}})$ curvature of one FET is aligned with a negative g_3 with a similar, but mirror-image curvature of another FET by offsetting their gate biases, and the g_3 magnitudes are equalized through a relative FET scaling, the resulting composite g_3 will be close to zero and the theoretical A_{IP3} will be significantly improved in a wide range of the gate biases, as shown in Fig. 1. At the optimum gate biases, FET M_A operates in the weak inversion (WI) region near the peak in its positive g_3 and FET M_B operates in the SI region near the dip in its negative g_3. The achieved A_{IP3} improvement due to zero composite g_3 happens only at very low frequencies at which the effect of circuit reactances is negligible.

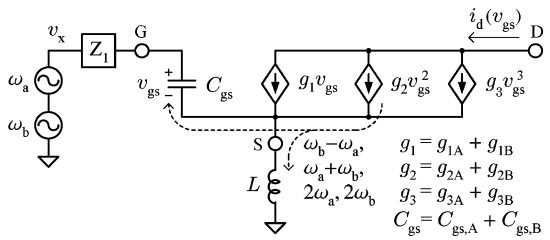

Fig. 2. Small-signal nonlinear equivalent circuit of the composite FET in Fig. 1(a).

III. RF Theory of DS Method

Consider a small-signal nonlinear equivalent circuit shown in Fig. 2 for a composite FET $(M_A + M_B)$ in Fig. 1(a). The signal generator is modeled by a Thevenin equivalent circuit with an open-circuit voltage v_x and a transformed output impedance Z_1. L is the source degeneration inductance. Here, we made the following assumptions.

1) The body effect is negligible i.e., $g_{mb} \approx 0$.
2) All capacitances are zero, except for the composite C_{gs}.
3) The composite C_{gs} is bias independent, i.e., linear.
4) The FET gate and source series resistances and the dc resistance of the degeneration inductor are zero.
5) The FET output conductance is infinite, i.e., there is no channel length modulation.
6) The input signal is very weak such that the $i_d(v_{\mathrm{gs}})$ nonlinearities of the order higher than three are negligible. This assumption is typical for LNAs because they operate far below their 1-dB compression point.

In this *weakly nonlinear* case with the neglected C_{gd}, IMD_3 would be generated entirely by the $g_3 v_{\mathrm{gs}}^3$ component of the drain current if L was zero. The source degeneration inductance creates a feedback path for the drain current to v_{gs}. This feedback is particularly strong for high-frequency spectral components of i_d. For example, the second harmonics $2\omega_a$ and $2\omega_b$ generated by $g_2 v_{\mathrm{gs}}^2$ are fed back across the gate and source adding to the fundamental components of v_{gs}. These spectral components are then mixed in $g_2 v_{\mathrm{gs}}^2$ to produce the responses at $2\omega_a \pm \omega_b$ and $2\omega_b \pm \omega_a$. Thus, the second-order nonlinearity of i_d also contributes to IMD_3.

Assuming that $\Delta\omega (= \omega_b - \omega_a)$ is much smaller than ω_a and ω_b such that $j\Delta\omega L \approx 0$ and the signal generator is conjugately matched to the FET input at $\omega (\omega \approx \omega_a \approx \omega_b)$, we can derive the following expression for IIP_3 [7]:

$$\mathrm{IIP}_3 = \frac{4 g_1^2 \omega^2 L C_{\mathrm{gs}}}{3|\varepsilon|} \tag{4}$$

where

$$\varepsilon = g_3 - \frac{2 g_2^2/3}{g_1 + \dfrac{1}{j2\omega L} + j2\omega C_{\mathrm{gs}} + Z_1(2\omega)\dfrac{C_{\mathrm{gs}}}{L}}. \tag{5}$$

As can be seen from (4) and (5), making the composite g_3 zero does not result in an infinite IIP_3 as it does at low frequencies due to the second term in (5). This term represents the contribution of the second-order nonlinearity to IMD_3. As expected, this contribution depends on the degeneration inductance L.

Fig. 1(c) shows IIP_3 calculated at 880 MHz using (4) and (5) for the composite FET in Fig. 1(a) with an input matching circuit consisting of a series capacitor and shunt inductor. As can be seen, the source degeneration inductance significantly suppresses the high-frequency IIP_3 peaking at V_{GS} where g_3 is close to zero. In fact, for realistic values of L, which are limited by the downbond inductance ($\geq$0.5 nH), the conventional DS method provides no IIP_3 improvement at all.

Replacing a common-source configuration with a symmetrically driven differential pair does not eliminate the second-order contribution to IMD_3 because the second harmonic currents generated by the FET pair are in-phase and create a common-mode voltage at the common source if the impedance from this node to ground is not zero at the second harmonic frequency. As a result, the gate–source voltages of both FETs contain nonzero second harmonic responses, which are mixed with the differential fundamental responses by the second-order nonlinearities of the FETs producing the differential IMD_3 responses in the drain currents.

According to (5), to minimize the second-order contribution to IMD_3 of a common-source FET with a nonzero source-degeneration inductance, $Z_1(2\omega)$ must be increased. However, the feedback through the neglected C_{gd} then becomes significant, which also leads to the second-order contribution to IMD_3. To completely eliminate this contribution and achieve a significant IIP_3 improvement in the DS method, the gate and drain terminations of the composite FET at the second harmonic frequency must be optimized. Our analysis shows that one of these terminations must have a negative real part, which would result in potential instability of the amplifier. The authors of [10] achieved a noticeable IIP_3 improvement using the conventional DS method by simply minimizing the source degeneration inductance and the drain load impedance. However, with a very small L, it is difficult to simultaneously achieve a good voltage standing-wave ratio (VSWR) and NF. The gain and NF of the LNA in [10] are only 10 and 2.85 dB, respectively, at 900 MHz.

IV. Noise Issues in DS Method

The DS method in general uses two FETs one of which is biased in the WI region [M_A in Fig. 1(a)] and the other in the SI region [M_B in Fig. 1(a)]. Intuitively, the overall NF of the composite FET should be dominated by the FET in SI since it draws 20–40 times more current than the FET in WI. This assumption is confirmed by simulations using BSIM3v3 models. However, it disagrees with our measured data.

The most significant MOSFET noise sources at RF are the drain current noise and the induced gate noise. These noise sources for the composite FET in the DS method are shown in Fig. 3, where the dc blocking capacitors and the bias resistors are neglected for simplicity. As can be seen, the drain and induced gate noise currents of the two FETs appear in parallel. These noise currents are given by [11]

$$\overline{i_{nd,X}^2} = 4kT\Delta f \gamma_X g_{d0,X} \tag{6}$$

$$\overline{i_{ng,X}^2} = 4kT\Delta f \delta_X g_{g,X} \tag{7}$$

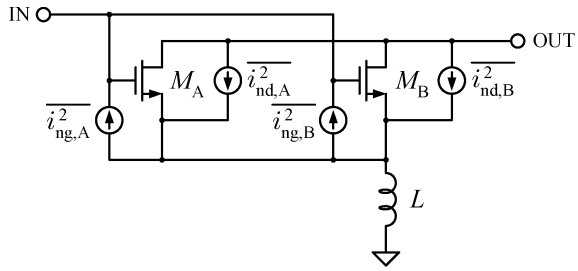

Fig. 3. Schematic of the DS method with major noise sources. The dc blocking capacitors and the bias resistors are neglected for simplicity.

where

$$g_{g,X} = \frac{4\omega^2 (C_{\mathrm{ox}} W_X L_{\mathrm{eff}})^2}{45 g_{d0,X}} \tag{8}$$

where k is the Boltzmann's constant, T is the absolute temperature, γ_X and δ_X are the bias-dependent noise coefficients, $g_{d0,X}$ is the drain–source conductance at zero V_{DS}, C_{ox} is the gate–oxide capacitance per unit area, W_X is the channel width, and L_{eff} is the channel length assumed to be the same for both FETs. The subscript X in the above notations denotes either A or B. The two noise currents are partially correlated, with a correlation coefficient defined as

$$c_X = \frac{\overline{i_{ng,X} \cdot i_{nd,X}^*}}{\sqrt{\overline{i_{ng,X}^2} \cdot \overline{i_{nd,X}^2}}}. \tag{9}$$

For simplicity, we will neglect the short-channel effects here. According to van der Ziel [11] if M_B is a saturated long-channel FET biased in SI, $\gamma_B = 2/3, \delta_B = 4/3, c_B = j0.395$, and

$$g_{d0,B} = \sqrt{2\mu C_{\mathrm{ox}} \frac{W_B}{L_{\mathrm{eff}}} I_{D,B}} \tag{10}$$

where μ is the electron mobility and $I_{D,B}$ is the drain saturation current of M_B. The van der Ziel noise model can also be extended for an FET in WI. As shown in Appendix A, if M_A is a saturated long-channel FET biased in WI, $\gamma_A = 1/2, \delta_A = 45/16, c_A = j0.707$, and

$$g_{d0,A} = \frac{I_{D,A}}{\phi_t} \tag{11}$$

where $I_{D,A}$ is the drain saturation current of M_A and ϕ_t is the thermal voltage kT/q. Substituting (11) into (8) and the latter into (7), we can make an interesting observation. While M_A draws a negligible drain current, its induced gate noise is inversely proportional to the drain current and, thus, can be quite significant. It adds to the induced gate noise current of M_B, degrading the overall NF in the DS method. Simulations using BSIM3v3 models do not predict this NF degradation because they do not take into account the induced gate noise.

To quantitatively estimate the NF degradation in the DS method due to the WI operation of M_A, we will reuse the result for the minimum noise factor of a common-source amplifier without degeneration from [14], but we will rewrite it in a more general way as follows:

$$F_{\min} = 1 + \frac{2}{g_m} \sqrt{\gamma g_{d0} \delta g_g \left(1 - |c|^2\right)}. \tag{12}$$

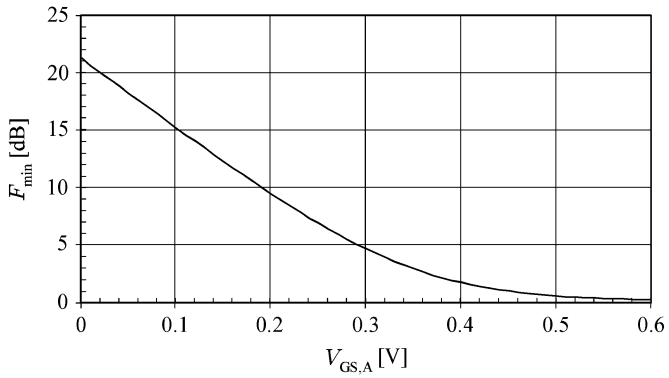

Fig. 4. Theoretical $F_{\min}$ of the circuit in Fig. 1(a) with $L = 0$ versus the gate bias of M_A. The gate bias of M_B is kept constant.

We will neglect the drain noise current of M_A due to the fact that $I_{D,A} \ll I_{D,B}$. We can then write

$$g_m \approx g_{m,B} \tag{13a}$$

$$g_{d0} \approx g_{d0,B} \tag{13b}$$

$$\gamma \approx \gamma_B. \tag{13c}$$

The induced gate noise of M_A increases the portion of the total induced gate noise current that is uncorrelated to $i_{nd,B}$. This uncorrelated portion is given by

$$\begin{aligned}\overline{i_{ngu}^2} &= 4kT\Delta f\delta g_g\left(1-|c|^2\right)\\ &= 4kT\Delta f\delta_A g_{g,A} + 4kT\Delta f\delta_B g_{g,B}\left(1-|c_B|^2\right).\end{aligned} \tag{14}$$

From the last equation, we get

$$\delta g_g(1-|c|^2) = \delta_A g_{g,A} + \delta_B g_{g,B}\left(1-|c_B|^2\right). \tag{15}$$

Substituting (15) and (13) into (12), we get

$$F_{\min} \approx 1 + \frac{2}{g_{m,B}}\sqrt{\gamma_B g_{d0,B}\left[\delta_A g_{g,A} + \delta_B g_{g,B}\left(1-|c_B|^2\right)\right]}. \tag{16}$$

The plot of $F_{\min}$ of the circuit in Fig. 1(a) with $L = 0$ computed using (16) versus the gate bias of M_A is shown in Fig. 4 (the gate bias of M_B is kept constant). As can be seen, $F_{\min}$ rapidly increases with $V_{\mathrm{GS},A}$ falling below the threshold voltage (in this process, 0.58 V) due to the increasing contribution of the induced gate noise of M_A. It should be noted that (16) was derived using the van der Ziel's first-order approximation of the induced gate noise and, therefore, it may correctly show the trend of $F_{\min}$ versus gate bias, but it may not be accurate for predicting the absolute values of $F_{\min}$ [15].

V. Modified DS Method

For the DS method to significantly boost IIP_3 at RF, it is not necessary to completely eliminate the second-order contribution to IMD_3. It is enough to make it the same magnitude and opposite phase with the third-order contribution. Instead of optimally scaling and rotating the second-order contribution by tuning the second harmonic terminations of the composite FET, here we propose a method shown in Fig. 5, which is similar to the conventional DS method, but uses two source-degeneration inductors in series. The FET sources are connected to different nodes of the inductor chain to adjust the magnitude and phase of the composite third-order contribution. M_A is biased in WI with a positive g_{3A} and M_B is biased in SI with a negative g_{3B}. It can be shown that the contributions of g_{1A} and g_{2A} to the overall response are negligible. The purpose of connecting the M_A source to the common node of the two inductors is to change the magnitude and phase of its g_{3A} contribution to IMD_3 relative to the g_{2B} and g_{3B} contributions of M_B.

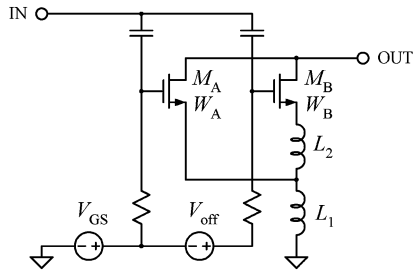

Fig. 5. Modified DS method.

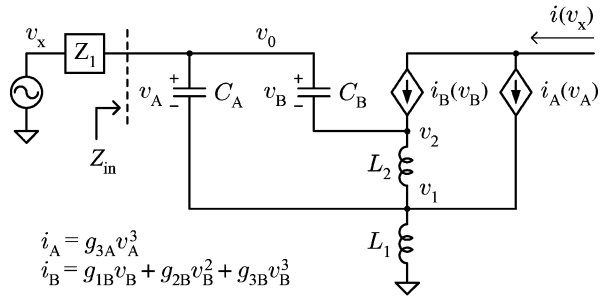

Fig. 6. Simplified equivalent circuit of the composite FET in Fig. 5.

To explain how the composite FET in Fig. 5 achieves high IIP_3 at RF, we will analyze its simplified equivalent circuit shown in Fig. 6, where the signal generator is modeled by a Thevenin equivalent circuit with an open-circuit voltage v_x and a transformed output impedance Z_1 as before, C_A and C_B are the gate–source capacitances of M_A and M_B, respectively, v_A and v_B are the small-signal gate–source voltages of M_A and M_B, respectively, and i_A and i_B are the small-signal drain currents of M_A and M_B, respectively. Here, we used the same assumptions as those made for the equivalent circuit in Fig. 2. To simplify derivations further, we also neglected the linear and second-order responses of M_A, i.e., assumed that $g_{1A} \approx 0$ and $g_{2A} \approx 0$.

The combined output current can be represented as the following truncated Volterra series in terms of the excitation voltage v_x in the time domain:

$$i(v_x) = C_1(s) \circ v_x + C_2(s_1, s_2) \circ v_x^2 + C_3(s_1, s_2, s_3) \circ v_x^3 \tag{17}$$

where $C_n(s_1, s_2, \ldots, s_n)$ is the Laplace transform of the nth-order Volterra kernel, also often called the nth-order nonlinear transfer function, $s(= j\omega)$ is the Laplace variable, and the operator "$\circ$" means that the magnitude and phase of each spectral component of v_x^n is to be changed by the magnitude

and phase of $C_n(s_1, s_2, \ldots, s_n)$ where the frequency of the component is $\omega_1 + \omega_2 + \cdots + \omega_n$. For a two-tone excitation

$$v_x = A\big[\cos(\omega_a t) + \cos(\omega_b t)\big] \tag{18}$$

the input tone amplitude at the intercept point of the IMD_3 response at $2\omega_b - \omega_a$ with the fundamental response at ω_a is given by [16]

$$A_{\mathrm{IP3}}(2\omega_b - \omega_a) = \sqrt{\frac{4}{3}\left|\frac{C_1(s_a)}{C_3(s_b, s_b, -s_a)}\right|}. \tag{19}$$

We will treat IIP_3 as the available power of the signal generator at the third-order intercept point. It is given by [17]

$$\begin{aligned}\mathrm{IIP}_3(2\omega_b - \omega_a) &= \frac{A_{\mathrm{IP3}}(2\omega_b - \omega_a)^2}{8\Re\big(Z_1(s_a)\big)} \\ &= \frac{1}{6\Re\big(Z_1(s_a)\big)}\left|\frac{C_1(s_a)}{C_3(s_b, s_b, -s_a)}\right|. \end{aligned} \tag{20}$$

To find the transfer functions of (17), we will use the *harmonic input* method [17]. This method is based on probing the circuit with a multitone excitation and solving the Kirchhoff's law equations in the frequency domain at the sum of all input frequencies. The number of incommensurable frequencies in v_x is equal to the order of the nonlinear transfer function to be found. The procedure starts with a single-tone excitation to determine the linear transfer function and is continued to higher order functions by adding one more input tone at each step. The derivations of $C_1(s_a)$ and $C_3(s_b, s_b, -s_a)$ for a narrow tone separation, the conjugate input match at the fundamental frequency, and a low-impedance input termination at the second harmonic frequency are shown in Appendix B. Substituting (47a) and (65) into (20) and taking into account (66), we get

$$\mathrm{IIP}_3 \approx \frac{4g_{1B}^2\omega^2\big[L_1(C_A + C_B) + L_2C_B\big]}{3|\varepsilon|} \tag{21}$$

where

$$\begin{aligned}\varepsilon = {} & g_{3A}(1 + j\omega L_2 g_{1B})\big[1 + (\omega L_2 g_{1B})^2\big] \\ & \cdot\left[1 + \frac{L_2C_B}{L_1(C_A + C_B) + L_2C_B}\right] \\ & + g_{3B} - \frac{2g_{2B}^2}{3g_{1B}}\frac{1}{1 + \dfrac{1}{j2\omega(L_1 + L_2)g_{1B}}} \end{aligned} \tag{22}$$

and $\omega \approx \omega_a \approx \omega_b$. The above expression does not show IIP_3 dependence on the intermodulation frequency (i.e., $2\omega_b - \omega_a$ versus $2\omega_a - \omega_b$) because the contribution of the difference-frequency mixing terms to IMD_3 is negligible at small $\Delta\omega(= \omega_b - \omega_a)$ due to the absence of a dc source resistance in the analyzed circuit (see Fig. 6).

Parameter ε shows how different nonlinearities of the circuit in Fig. 6 contribute to IMD_3. The first two terms in (22) represent the contributions of the third-order nonlinearities of M_A and M_B, respectively, and the last term represents the contribution of the second-order nonlinearity of M_B. The phase of the composite third-order contribution of M_A and M_B is dependent on L_2. If L_2 were zero, the imaginary part of the first term in (22) would be zero and the vector of the composite third-order contribution described by the first two terms could never be made collinear with the vector of the second-order contribution described by the last term since the latter has a nonzero imaginary part. Therefore, the distortion cancellation would not be possible, as in the case of the conventional DS method. Graphically, this is explained by the vector diagram in Fig. 7(a).

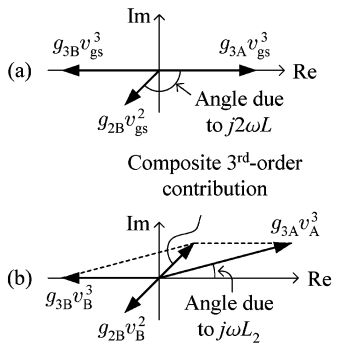

Fig. 7. Vector diagram for the IMD_3 components. (a) Conventional DS method. (b) Modified DS method.

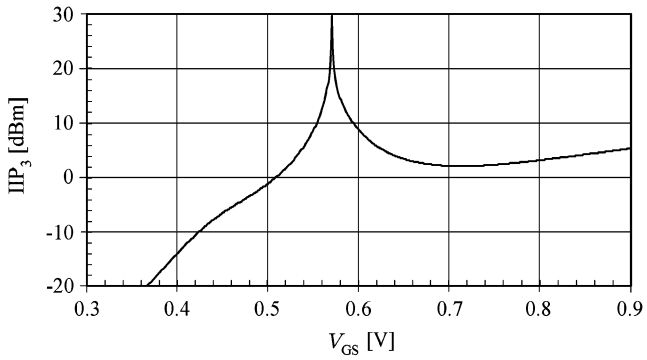

Fig. 8. Theoretical IIP_3 at 880 MHz of the circuit in Fig. 5 ($W_A = 240\ \mu$m, $W_B = 460\ \mu$m, $L_1 = 0.83$ nH, $L_2 = 0.61$ nH, $V_{\mathrm{off}} = 0.2$ V).

The idea of the modified DS method is to use the L_2 portion of the total degeneration inductance to rotate the phase of the g_{3A} contribution to IMD_3 relative to that of the g_{3B} contribution such that their sum is out-of-phase with the second-order contribution. Graphically, this is explained by the vector diagram in Fig. 7(b). In order for IMD_3 to be zero, both the real and imaginary parts of ε must be zero. The equations $\Re(\varepsilon) = 0$ and $\Im(\varepsilon) = 0$ can be solved for L_1 and L_2. Using the FET sizes and bias offset from Fig. 1(a) as an example, the solutions at $V_{\mathrm{GS}} = 0.57$ V are $L_1 = 0.83$ nH and $L_2 = 0.61$ nH. The plot of IIP_3 at 880 MHz computed using (21) versus V_{GS} is shown in Fig. 8. As can be seen, with the total degeneration inductance of 1.44 nH, a significant IIP_3 improvement is achieved at optimum gate biases in comparison with the conventional DS method used at the same frequency [see Fig. 1(c)]. The fact that the proposed modified DS method does not require the degeneration inductance to be minimized as in [10] makes the simultaneous noise-power match possible.

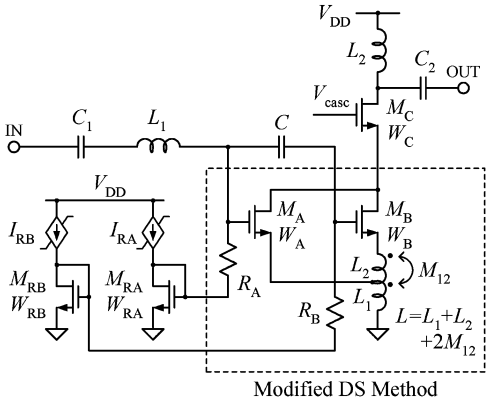

Fig. 9. Simplified schematic diagram of LNA using modified DS method.

VI. LNA Design and Measured Results

The proposed modified DS method was used in the cellular-band CDMA LNA whose schematic is shown in Fig. 9. Instead of two degeneration inductors in series, the LNA uses a single tapped inductor to save the die area. The input FETs M_A and M_B are interdigitated for better mutual matching and to reduce their combined drain–bulk capacitance and, thus, the noise contribution of the cascode FET M_C. FET M_A is biased in WI and FET M_B is biased in SI. Their gate bias voltages are generated by the diode-connected FETs M_{RA} and M_{RB}, respectively, whose drain currents I_{RA} and I_{RB} are independently programmable. We used the current-derived bias because it results in less $\mathrm{IIP_3}$ variations from part to part than a voltage-derived bias. A constant-gm bias circuit was used to minimize the gain and $\mathrm{IIP_3}$ variations over temperature. The ratios $W_B/W_A, I_{RB}/I_{RA}$, and L_2/L_1 were optimized for the highest $\mathrm{IIP_3}$ using a commercial circuit simulator. Due to the interdigitation of M_A and M_B, the evaluated values of W_B/W_A were limited to ratios of small integers, i.e., 1/1, 2/1, 3/2, etc. The evaluated values of I_{RB}/I_{RA} were also limited to the ratios of integers whose sum was kept constant (equal to 40) to ensure a constant total dc current. At each optimization step, the total degeneration inductance was adjusted to keep the LNA gain constant. We found that the optimum ratios were $W_B/W_A = 3/2, I_{RB}/I_{RA} = 39/1$ and $L_2/L_1 = 0.85$ with the total degeneration inductance L of 2.7 nH including the bondwire.

The LNA was manufactured in a 0.25-μm Si CMOS technology as part of a cellular-band CDMA zero-IF receiver and packaged in a 32-pin quad flat no-lead (QFN) package. Its measured power gain and NF are 15.5 and 1.65 dB, respectively, with the current consumption of 9.3 mA from 2.6 V excluding the bias circuit. The input and output return losses are lower than -11 dB. The LNA $\mathrm{IIP_3}$ was tested with two tones at 880 and 880.5 MHz and was found to be insensitive to the tone separation. The measured output powers of the fundamental and $\mathrm{IMD_3}$ responses as functions of the input power per tone are plotted in Fig. 10. In the single-tone desensitization scenario of an IS-98 mobile receiver, the combined power of the single-tone jammer and the transmitted signal leakage can be as high as -27 dBm. Therefore, it is important that the LNA exhibits a high linearity below this input power. As can be seen from Fig. 10, below

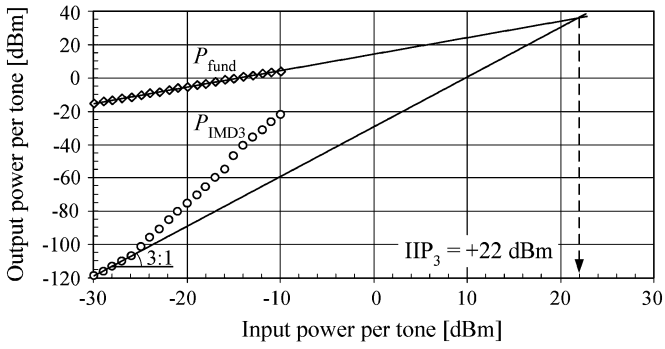

Fig. 10. Measured CMOS LNA two-tone transfer characteristics.

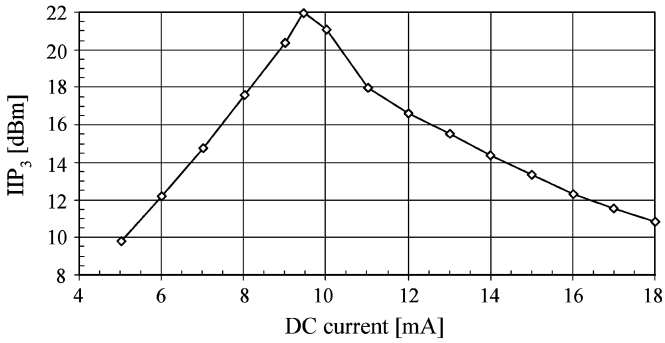

Fig. 11. Measured $\mathrm{IIP_3}$ at $P_{\mathrm{in}} = -30$ dBm as a function of the combined dc current of the input FETs. The ratio I_{RB}/I_{RA} is kept constant.

P_{in} of -25 dBm per tone, the $P_{\mathrm{IMD3}}(P_{\mathrm{in}})$ curve rises with a slope 3 : 1 and $\mathrm{IIP_3} = +22$ dBm. At higher input power levels, the slope is steeper than 3 : 1 indicating that $\mathrm{IMD_3}$ is dominated by the fifth-order and higher odd-order nonlinearities. If the third-order nonlinearity was completely cancelled, the slope 3 : 1 would not exist and $\mathrm{IIP_3}$ would be meaningless. In this case, the fifth-order or higher order intercept points could be used to estimate the distortion levels at particular input power levels. We also measured $\mathrm{IIP_3}$ for different values of the master reference current with the ratio I_{RB}/I_{RA} kept constant. Fig. 11 shows that the LNA maintains high $\mathrm{IIP_3}$ in a wide range of the dc current through the composite FET. The achieved $\mathrm{IIP_3}$ was found to be insensitive to the input and output harmonic terminations.

To investigate the effect of the gate bias of M_A on the LNA performance, we measured the LNA $\mathrm{IIP_3}$, gain, NF, and dc current as functions of $V_{\mathrm{GS},A}$ with $V_{\mathrm{GS},B}$ kept constant. The results are presented in Fig. 12. As can be seen, the peak in $\mathrm{IIP_3}$ is fairly broad and centered around $V_{\mathrm{GS},A} = 0.55$ V. As predicted by the theory, reducing $V_{\mathrm{GS},A}$ increases the LNA NF due to the increasing induced gate noise current of M_A. The rate at which the NF increases with the dropping $V_{\mathrm{GS},A}$ is much lower than the theoretical one shown in Fig. 4 indicating the deficiency of the van der Ziel's first-order approximation of the induced gate noise at subthreshold biases (see also [15]).

We also manufactured an LNA with a single-input FET. It achieved 16-dB gain, +2-dBm $\mathrm{IIP_3}$, and 1.4-dB NF with 9-mA dc current. Thus, the proposed modified DS method boosted $\mathrm{IIP_3}$ by approximately 20 dB, but degraded the NF by 0.25 dB due to the induced gate noise of the FET biased in WI (M_A in Fig. 9).

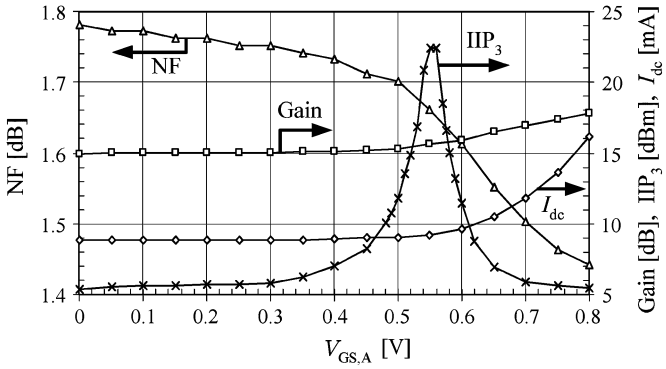

Fig. 12. Measured IIP_3, gain, NF, and combined dc current versus the gate bias voltage of M_A. The gate bias of M_B is kept constant ($V_{\mathrm{GS},B} \approx 0.75$ V).

TABLE I
COMPARISON OF STATE-OF-THE-ART LINEAR FET LNAS

Work	Technology	Freq GHz	S21 dB	NF dB	IIP_3 dBm	P_{dc} mA@V	FOM
This work	0.25μm Si CMOS	0.9	15.5	1.65	+22	9.3@2.6	503
[7]	0.25μm Si CMOS	0.9	14.6	1.8	+10.5	2@2.7	117
[19]	0.6μm GaAs MESFET	0.9	17	1.6	+8.5	4.7@2.7	62.8
[20]	0.25μm Si CMOS	2.2	14.9	3	+16.1	9.4@2.5	53.8
[10]	0.35μm Si CMOS	0.9	10	2.8	+15.6	7.8@2.7	19
[3]	0.35μm Si CMOS	0.9	2.5	2.8	+18	15@3	3

To compare the designed high-linearity CMOS LNA with other state-of-the-art FET LNAs, we will use the dynamic-range figure-of-merit (FOM) defined as [18]

$$\mathrm{FOM} = \frac{\mathrm{OIP}_3}{(F-1)P_{\mathrm{dc}}} \tag{23}$$

where OIP_3 is the output referred third-order intercept point ($\mathrm{OIP}_3 = \text{Power Gain} \cdot \mathrm{IIP}_3$), F is the noise factor ($F = 10^{\mathrm{NF}/10}$), and P_{dc} is the dc power consumption. Table I summarizes the performances of our and other state-of-the-art FET LNAs. As can be seen, our LNA using the modified DS method has the highest FOM. To our knowledge, this FOM is also the highest among LNAs using bipolar transistors.

VII. CONCLUSION

We have shown that the conventional DS method does not provide a significant IIP_3 improvement at RF due to the contribution of the second-order nonlinearity to IMD_3. In general, the vector of this contribution is not collinear with the vector of the third-order contribution and, therefore, they cannot cancel each other. To give these contributions opposite phases, we proposed a modified DS method that uses two inductors in series (or a tapped inductor) for source degeneration of the composite FET. This method boosted IIP_3 of the designed CMOS LNA by 20 dB. This LNA has the highest dynamic range FOM among known FET LNAs. We also explained the reason why the composite FET in the DS method exhibits a higher NF than a single FET. Our analysis showed that the FET biased in the subthreshold region is responsible for this NF degradation due to its high induced gate noise, which is inversely proportional to the drain current. We found that the van der Ziel noise theory overestimates this NF degradation, which indicates the deficiency of its first-order approximation of the induced gate noise at subthreshold biases.

APPENDIX A

Here, we derive the drain and induced gate noise coefficients for a saturated long-channel MOSFET biased in WI (M_A in Fig. 3) following the approach outlined by van der Ziel in [11]. For simplicity, we omit the letter A in the subscripts of notations here.

To find the drain noise current, we will start with an expression for the drain current caused by the noise voltage Δv_{x0} across the channel section between x_0 and $x_0 + \Delta x_0$ [11] as follows:

$$\Delta i_{nd} = \frac{g(V_0)}{L_{\mathrm{eff}}} \Delta v_{x0} \tag{24}$$

where $g(V_0)$ is the channel conductance per unit length at x_0, and V_0 is the dc potential at x_0. In the WI region, the drain current mechanism is due to diffusion. According to [12],

$$g(V_0) = g_0 e^{-\frac{V_0}{\phi_t}} \tag{25}$$

where g_0 is the channel conductance per unit length at the source terminal ($V_0 = 0$) and ϕ_t is the thermal voltage kT/q.

The mean-square value of Δi_{nd} is given by

$$\overline{\Delta i_{nd}^2} = \frac{g^2(V_0)}{L_{\mathrm{eff}}^2} \overline{\Delta v_{x0}^2} \tag{26}$$

where

$$\overline{\Delta v_{x0}^2} = 4kT\Delta f \frac{\Delta x_0}{g(V_0)} = 4kT\Delta f \frac{\Delta V_0}{I_D}. \tag{27}$$

The total drain noise current can be found as follows:

$$\overline{i_{nd}^2} = \int_0^{L_{\mathrm{eff}}} \frac{d\left(\overline{\Delta i_{nd}^2}\right)}{dx}\, dx = \frac{4kT\Delta f}{L_{\mathrm{eff}}^2 I_D} \int_0^{V_D} g^2(V_0)\, dV_0 \tag{28}$$

where V_D is the dc drain potential (the source is assumed grounded). The last equation was first derived by Klaassen and Prins [13]. Substituting (25) into (28) and simplifying the result for $V_D \gg \phi_t$, we get

$$\overline{i_{nd}^2} \approx 2kT\Delta f \frac{g_0^2 \phi_t}{L_{\mathrm{eff}}^2 I_D}. \tag{29}$$

We also know that

$$I_D = \frac{1}{L_{\mathrm{eff}}} \int_0^{V_D} g(V_0)\, dV_0. \tag{30}$$

Substituting (25) into (30), we get

$$I_D = \frac{g_0\phi_t}{L_{\text{eff}}}\left(1 - e^{-\frac{V_D}{\phi_t}}\right). \tag{31}$$

For $V_D \gg \phi_t$, the above expression simplifies to

$$I_D \approx \frac{g_0\phi_t}{L_{\text{eff}}}. \tag{32}$$

Solving for g_0 in (32) and substituting it to (29), we get

$$\overline{i_{nd}^2} = 2kT\Delta f\frac{I_D}{\phi_t} = 2qI_D\Delta f. \tag{33}$$

Using (31) and (32), we can also find

$$g_{d0} = \left.\frac{\partial I_D}{\partial V_D}\right|_{V_D=0} = \frac{g_0}{L_{\text{eff}}} \approx \frac{I_D}{\phi_t} \tag{34}$$

and, thus,

$$\overline{i_{nd}^2} = 2kT\Delta f g_{d0}. \tag{35}$$

A comparison of (35) with (6) yields $\gamma = 1/2$.

In the first-order approximation, the gate current caused by the noise voltage Δv_{x0} is given by [11]

$$\Delta i_{ng} = j\omega C_{\text{ox}}W g(V_0)\Delta v_{x0}\left[\int_{V_0}^{V_D}\frac{dx}{g(V)} - \int_0^{V_D}\frac{xdx}{L_{\text{eff}}g(V)}\right]. \tag{36}$$

We know that [11]

$$dx = \frac{g(V)dV}{I_D} \tag{37}$$

and, therefore,

$$x = \int_0^V \frac{g(u)du}{I_D} = \frac{g_0\phi_t}{I_D}\left(1 - e^{-\frac{V}{\phi_t}}\right). \tag{38}$$

Substituting (37), (38), and (25) into (36) and simplifying the result for $V_D \gg \phi_t$, we get

$$\Delta i_{ng} \approx \frac{j\omega C_{\text{ox}}W g(V_0)\Delta v_{x0}}{I_D}(\phi_t - V_0). \tag{39}$$

The total induced gate noise current is

$$\begin{aligned}\overline{i_{ng}^2} &= \int_0^{L_{\text{eff}}}\frac{d\left(\overline{\Delta i_{ng}^2}\right)}{dx}dx \\ &= 4kT\Delta f\frac{\omega^2C_{\text{ox}}^2W^2}{I_D^3}\int_0^{V_D} g^2(V_0)(\phi_t - V_0)^2dV_0 \\ &\approx kT\Delta f\omega^2C_{\text{ox}}^2W^2L_{\text{eff}}^2\frac{\phi_t}{I_D}.\end{aligned} \tag{40}$$

Taking into account (34), we can write

$$\overline{i_{ng}^2} = kT\Delta f\frac{\omega^2(C_{\text{ox}}WL_{\text{eff}})^2}{g_{d0}}. \tag{41}$$

A comparison of (41) with (7) yields $\delta = 45/16$.

To find the correlation coefficient between i_{ng} and i_{nd}, we need the following cross-correlation:

$$\overline{i_{ng}i_{nd}^*} = \int_0^{L_{\text{eff}}}\frac{d\left(\overline{\Delta i_{ng}\Delta i_{nd}^*}\right)}{dx}dx. \tag{42}$$

Substituting (39) and (24) into (42) and taking into account (27), we get

$$\begin{aligned}\overline{i_{ng}i_{nd}^*} &= 4kT\Delta f\frac{j\omega C_{\text{ox}}W}{I_D^2L_{\text{eff}}}\int_0^{V_D} g^2(V_0)(\phi_t - V_0)dV_0 \\ &\approx kT\Delta f j\omega C_{\text{ox}}WL_{\text{eff}}.\end{aligned} \tag{43}$$

Finally, the correlation coefficient

$$c = \frac{\overline{i_{ng}\cdot i_{nd}^*}}{\sqrt{i_{ng}^2\cdot i_{nd}^2}} = \frac{j}{\sqrt{2}}. \tag{44}$$

APPENDIX B

Here, the first- and third-order coefficients of the Volterra series (17) are derived using the harmonic input method.

First, we will establish the relationship between the combined output current i and the gate–source voltages v_A and v_B. From Fig. 6,

$$i_A = g_{3A}v_A^3 \tag{45a}$$

$$i_B = g_{1B}v_B + g_{2B}v_B^2 + g_{3B}v_B^3 \tag{45b}$$

$$i = i_A + i_B = g_{3A}v_A^3 + g_{1B}v_B + g_{2B}v_B^2 + g_{3B}v_B^3. \tag{45c}$$

The gate–source voltages can be modeled by the following truncated Volterra series in terms of the excitation voltage v_x:

$$v_A = A_1(s)\circ v_x + A_2(s_1,s_2)\circ v_x^2 + A_3(s_1,s_2,s_3)\circ v_x^3 \tag{46a}$$

$$v_B = B_1(s)\circ v_x + B_2(s_1,s_2)\circ v_x^2 + B_3(s_1,s_2,s_3)\circ v_x^3. \tag{46b}$$

Substituting (46) into (45c) and comparing the resulting expression with (17), we can write

$$C_1(s) = g_{1B}B_1(s), \tag{47a}$$

$$\begin{aligned}C_3(s_1,s_2,s_3) = {} & g_{3A}A_1(s_1)A_1(s_2)A_1(s_3) \\ & + g_{1B}B_3(s_1,s_2,s_3) \\ & + 2g_{2B}\overline{B_1(s_1)B_2(s_2,s_3)} \\ & + g_{3B}B_1(s_1)B_1(s_2)B_1(s_3)\end{aligned} \tag{47b}$$

where the bar indicates the symmetrization (averaging) of the corresponding transfer function over all possible permutations of the Laplace variables, i.e.,

$$\overline{B_1(s_1)B_2(s_2,s_3)} = \frac{1}{3}\big[B_1(s_1)B_2(s_2,s_3) + B_1(s_2)B_2(s_1,s_3) + B_1(s_3)B_2(s_1,s_2)\big]. \quad (47c)$$

Therefore, to find $C_1(s)$ and $C_3(s_1,s_2,s_3)$, we first need to find $A_1(s), B_1(s), B_2(s_1,s_2)$, and $B_3(s_1,s_2,s_3)$.

The Kirchhoff's current law equations for each node of the circuit in Fig. 6 are

$$\frac{v_x - v_0}{Z_1(s)} + (v_1 - v_0)sC_A + (v_2 - v_0)sC_B = 0 \quad (48a)$$

$$(v_0 - v_1)sC_A + i_A + \frac{v_2 - v_1}{sL_2} - \frac{v_1}{sL_1} = 0 \quad (48b)$$

$$(v_0 - v_2)sC_B + i_B + \frac{v_1 - v_2}{sL_2} = 0. \quad (48c)$$

Solving these equations for v_0, v_1, and v_2 and substituting the solutions into $v_A = v_0 - v_1$ and $v_B = v_0 - v_2$, we get

$$v_A = \frac{v_x a(s) - i_A a(s)b(s)l - i_B b(s)c(s)}{a(s)d(s) - c(s)} \quad (49a)$$

$$v_B = \frac{v_x - i_A b(s)l - i_B b(s)d(s)}{a(s)d(s) - c(s)} \quad (49b)$$

where

$$l = \frac{L_1}{L_2} \quad (49c)$$

$$a(s) = 1 + s^2 L_2 C_B \quad (49d)$$

$$b(s) = sL_2 \quad (49e)$$

$$c(s) = l - sC_B Z_1(s) \quad (49f)$$

$$d(s) = 1 + l + sC_A\big(Z_1(s) + sL_1\big). \quad (49g)$$

Equation (49a)–(49c) is the starting point for derivations of the transfer functions of (46a) and (46b). The idea of the harmonic input method is that these equations must hold separately for the first-order (i.e., linear) terms, as well as the second- and third-order intermodulation products. To find the linear transfer functions $A_1(s)$ and $B_1(s)$, we will excite the circuit with a single tone $v_x = e^{st}$. Substituting (45a), (45b), and (46a) and (46b) into (49a) and (49b), equating the coefficients of e^{st} on both sides of (49a)–(49g), and solving for $A_1(s)$ and $B_1(s)$, we get

$$A_1(s) = n(s)B_1(s) \quad (50a)$$

$$B_1(s) = \frac{1}{a(s)d(s) - c(s) + g_{1B}b(s)d(s)} \quad (50b)$$

where

$$n(s) = a(s) + g_{1B}b(s). \quad (51)$$

To find the second-order transfer function $B_2(s_1,s_2)$, we will excite the circuit with two tones $v_x = e^{s_1 t} + e^{s_2 t}$. Substituting (45a), (45b), and (46a) and (46b) into (49a) and (49b), equating the coefficients of $e^{(s_1+s_2)t}$ on both sides of (49a)–(49g) and solving for $B_2(s_1,s_2)$, we get

$$B_2(s_1,s_2) = -g_{2B}b(s_1+s_2)d(s_1+s_2) \cdot B_1(s_1+s_2)B_1(s_1)B_1(s_2). \quad (52)$$

Similarly, using a three-tone excitation, we can derive

$$\begin{aligned} &B_3(s_1,s_2,s_3) \\ &\quad = -b(s_1+s_2+s_3)B_1(s_1+s_2+s_3) \\ &\qquad \cdot \Big\{\big[g_{3B}B_1(s_1)B_1(s_2)B_1(s_3) \\ &\qquad\quad + 2g_{2B}\overline{B_1(s_1)B_2(s_2,s_3)}\big]d(s_1+s_2+s_3) \\ &\qquad\quad + lg_{3A}A_1(s_1)A_1(s_2)A_1(s_3)\Big\}. \end{aligned} \quad (53)$$

For the input excitation given by (18), IMD_3 at $2\omega_b - \omega_a$ is found by setting $s_1 = s_2 = s_b$ and $s_3 = -s_a$. Assuming closely spaced frequencies, i.e., $s_a \approx s_b \approx s$, we can simplify (53) and (47c) as follows:

$$\begin{aligned} B_3(s_b,s_b,-s_a) &= -b(s)B_1(s) \\ &\quad \cdot \Big\{d(s)\big[g_{3B}B_1(s)|B_1(s)|^2 \\ &\qquad + 2g_{2B}\overline{B_1(s_b)B_2(s_b,-s_a)}\big] \\ &\qquad + lg_{3A}A_1(s)|A_1(s)|^2\Big\} \end{aligned} \quad (54)$$

$$\overline{B_1(s_b)B_2(s_b,-s_a)} = \frac{1}{3}\big[2B_1(s_b)B_2(s_b,-s_a) + B_1(-s_a)B_2(s_b,s_b)\big]. \quad (55)$$

Substituting (52) into (55), we get

$$\begin{aligned} \overline{B_1(s_b)B_2(s_b,-s_a)} &= -\frac{g_{2B}B_1(s_b)^2B_1(-s_a)}{3} \\ &\quad \cdot \big[2b(\Delta s)d(\Delta s)B_1(\Delta s) \\ &\qquad + b(2s_b)d(2s_b)B_1(2s_b)\big] \end{aligned} \quad (56)$$

where $\Delta s = s_b - s_a$. From the assumption that $s_a \approx s_b$, it follows that $\Delta s \approx 0$ and $b(\Delta s) \approx 0$. Equation (56) then simplifies to

$$\overline{B_1(s_b)B_2(s_b,-s_a)} \approx -\frac{g_{2B}B_1(s)|B_1(s)|^2}{3} \cdot b(2s)d(2s)B_1(2s). \quad (57)$$

Substituting (57) and (50a) into (54), we get

$$\begin{aligned} &B_3(s_b,s_b,-s_a) \\ &\quad = -b(s)B_1(s)^2|B_1(s)|^2 \\ &\qquad \cdot \left\{d(s)\left[g_{3B} - \frac{2g_{2B}^2}{3}b(2s)d(2s)B_1(2s)\right]\right. \\ &\qquad\quad \left. + lg_{3A}n(s)|n(s)|^2\right\}. \end{aligned} \quad (58)$$

Substituting (58), (57), and (50a) into (47b), we get

$$\begin{aligned} C_3(s_b, s_b, -s_a) &= B_1(s)|B_1(s)|^2 \\ &\cdot \Big\{ g_{3A} n(s)|n(s)|^2 \big[1 - l g_{1B} b(s) B_1(s)\big] \\ &+ \big[1 - g_{1B} b(s) d(s) B_1(s)\big] \\ &\cdot \left[g_{3B} - \frac{2 g_{2B}^2}{3} b(2s) d(2s) B_1(2s) \right] \Big\}. \end{aligned} \tag{59}$$

To simplify (59), we will consider the case of the conjugately matched input at the fundamental frequency, i.e.,

$$Z_1(s) = Z_{\text{in}}(-s) \tag{60}$$

where $Z_{\text{in}}(s)$ is the input impedance of the circuit given by

$$Z_{\text{in}}(s) = sL_1 + \frac{1 + s(L_1 + L_2) g_{1B} + s^2 L_2 C_B}{s(C_A + C_B + sL_2 C_A g_{1B} + s^2 L_2 C_A C_B)}. \tag{61}$$

In this case,

$$1 - g_{1B} b(s) d(s) B_1(s) = 1/2. \tag{62}$$

We will further assume that

$$\omega^2 L_1 C_{\text{A}} \ll \frac{\omega}{\omega_{TB}} \tag{63a}$$

$$\omega^2 L_2 C_B \ll 1/4 \tag{63b}$$

$$\Re(Z_1(2s)) \ll (L_1 + L_2) \cdot \min\left(\omega_{TB}, \frac{g_{1B}}{C_A} \right) \tag{63c}$$

$$|\Im(Z_1(2s))| \ll \frac{1}{2\omega \cdot \max(C_A, C_B)} \tag{63d}$$

where $\omega_{TB} = g_{1B}/C_B$. The last two assumptions call for a relatively low impedance presented to the composite FET gate at the second harmonic frequency. They are not necessary for the proposed modified DS method to work and are only used here to simplify expressions for demonstration purposes. Using (63), we can write

$$n(s) \approx 1 + g_{1B} s L_2 \tag{64a}$$

$$1 - l g_{1B} b(s) B_1(s) \approx \frac{1}{2}\left[1 + \frac{L_2 C_B}{L_1(C_A + C_B) + L_2 C_B}\right] \tag{64b}$$

$$b(2s) d(2s) B_1(2s) \approx \frac{1}{g_{1B} + \frac{1}{2s(L_1 + L_2)}}. \tag{64c}$$

Substituting (62) and (64) into (59), we get

$$C_3(s_b, s_b, -s_a) = \frac{1}{2} B_1(s)|B_1(s)|^2 \varepsilon \tag{65a}$$

where

$$\begin{aligned} \varepsilon \approx\ & g_{3A}(1 + sL_2 g_{1B})\big[1 + (\omega L_2 g_{1B})^2\big] \\ &\cdot \left[1 + \frac{L_2 C_B}{L_1(C_A + C_B) + L_2 C_B}\right] \\ &+ g_{3B} - \frac{2 g_{2B}^2}{3 g_{1B}} \frac{1}{1 + \dfrac{1}{2s(L_1 + L_2) g_{1B}}}. \end{aligned} \tag{65b}$$

For IIP_3 derivations, the following quantity will also be needed:

$$\Re\big(Z_1(s)\big)|B_1(s)|^2 \approx \frac{1}{4 g_{1B} \omega^2 [L_1(C_A + C_B) + L_2 C_B]}. \tag{66}$$

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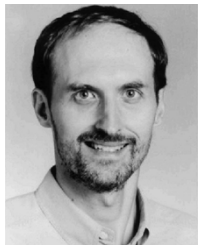

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