"Distortion-Free" Varactor Diode Topologies for RF Adaptivity

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***Abstract* — Varactor diode-based circuit topologies, which can act as high-Q "distortion-free" tunable capacitive elements, are presented. These diodes are implemented in a novel ultra low-loss silicon-on-glass technology, with resulting measured Q's of over 200 at 2 GHz. The measured IM3 improvement compared to traditional single varactor tuning techniques is greater than 30 dB.**

***Index Terms* — Distortion, impedance matching, losses, tunable filters, tuners, varactors.**

I. Introduction

Next-generation wireless systems will dramatically benefit from circuit techniques that allow for RF "adaptivity." Some examples of adaptive circuits include tunable power amplifier matching networks, tunable filters, and multi-band VCO's. Currently, PIN Diodes or PHEMT devices are used for implementing RF adaptivity. However, these solutions are considered to be too expensive, not technologically compatible, or simply too lossy or power hungry to be the final solution for adaptive matching networks. An ideal tunable element will provide extremely low loss, high linearity, ruggedness, wide tuning range, very low cost, low area usage, and be continuously tunable, with a high tuning speed.

This need has triggered an intensive search for alternatives that do not suffer from the drawbacks of traditional approaches. One example is the MEMS capacitor, which in its most popular implementation is able to switch between two fixed capacitance values. MEMS capacitors provide a very high Q at moderate capacitance values [1][2] but they require non-standard processing, expensive packaging techniques, high control voltages, and their reliability and switching speed are still poor compared to semiconductor-based solutions. Other proposed tuning techniques based on voltage-variable dielectrics exhibit similar drawbacks of manufacturability and performance [3].

In view of this urgent need, more simple tunable elements like varactor diodes would seem to be a logical choice for implementing RF adaptivity [4]. However, their inherently nonlinear behavior disqualifies them for use with modern communication standards characterized by high peak-to-average power ratios, and their related Q factors are usually too low at the microwave frequencies of interest.

In order to overcome these drawbacks, we present varactor diode-based circuit topologies, which for a given grading coefficient (n=0.5), can act as variable capacitors with extremely low or, in the special case of n=0.5, theoretically no distortion. These low distortion varactor stack (LDVS) components are, through their ease of implementation and inherently high performance, suitable for use in a variety of high-Q tunable circuits, including filters, switches, phase shifters and matching networks. To demonstrate their performance in terms of quality factor and linearity, a dedicated ultra-low-loss silicon-on-glass technology was developed, which has been utilized for the implementation of a tunable filter and adaptive matching network.

II. Low-distortion varactor stack (LDVS) circuits

The capacitance of a single varactor diode can usually be expressed as

$$C(V) = \frac{K}{(\phi + V)^n} \tag{1}$$

where ϕ is the built-in potential of the diode, V is the applied voltage, n is the power law exponent of the diode capacitance, and K is the capacitance constant. The power law exponent can exhibit wide variation in different situations, from a value of $n \approx 0.3$ for an implanted junction to $n \approx 0.5$ for a uniformly doped junction to $n \approx 1.5$ for a hyper-abrupt junction.

If the applied dc voltage is V_{DC}, then the incremental capacitance of a single varactor diode as a function of the incremental voltage v can be expressed as

$$C(v) = C_0 + C_1 v + C_2 v^2 + \ldots . \tag{2}$$

where the C_1 term in (2) gives rise to second-order distortion and the C_2 term gives rise to third-order distortion.

The diode configuration in Fig. 2(a) can be employed to realize a voltage variable capacitor with theoretically no distortion. For this purpose, we set the ratio of the diode areas D_B/D_A to be s. Evaluation of the topology of Fig. 1(a), yields expressions for the linear and nonlinear terms of the capacitance

$$C_0 = \frac{sK_A}{(1+s)(\phi + V_{DC})^n}, \tag{3}$$

$$C_1 = \frac{(1-s)nC_0}{(1+s)(\phi + V_{DC})} \tag{4}$$

and

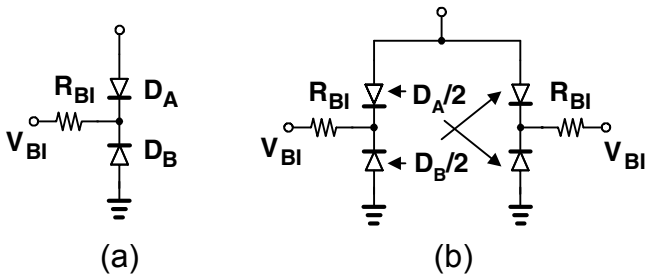

Fig. 1. (a) Anti-series connection of varactor diodes to minimize third-order distortion. The ratio of the areas of D_A and D_B follows form setting C_2 to zero, for n≥0.5. (b) Anti-series/anti-parallel connection of varactor diodes to minimize second *and* third-order distortion for grading coefficients >0.5. In this case, both C_1 and C_2 can be set to zero.

$$C_2 = \frac{C_0\left[\left(s^2+1\right)\left(n+1\right)-s\left(4n+1\right)\right]}{2\left(\phi+V_{DC}\right)^2\left(s+1\right)^2}. \qquad (5)$$

Note that C_2 of (5) can be made equal to zero by setting

$$s=\frac{4n+1+\sqrt{12n^2-3}}{2\left(n+1\right)} \qquad (6)$$

resulting in zero third-order distortion caused by the capacitance term C_2. The result of (6) demonstrates that cancellation can *only* occur for cases where the diode power-law exponent is equal or greater than 0.5. Also, as was pointed out in [5] a constant doping profile in the diode (the so-called "abrupt junction" case where *n=0.5*) results in a *value of s* of unity. This case is particularly attractive because – from (4) – this set of conditions (*n=0.5, s=1*), sets *both* C_2 *and* C_1 equal to zero. A more elaborate analysis shows that *all* higher order distortion terms vanish, yielding (in theory) a "distortion-free" operation for this unique case.

When dealing with process technologies where *n>0.5* the solution of (6) provides a direct means of calculating the required diode area ratio to minimize C_2. For example, in the case where *n=1*, the required area ratio is exactly two. In the case of *n=2*, which corresponds to the ideal hyper-abrupt junction, the required area ratio is 2.6. These values are straightforward to realize with high accuracy in any standard integrated circuit process that includes varactor diodes.

Although this approach can minimize C_2, it is clear from (4), that a value of s≠1 will result in a finite value of C_1. In this case, a relatively high third-order distortion product will unfortunately still arise, resulting from the secondary mixing of the fundamental with the second-order non-linearity C_1. Fortunately, this distortion contribution can be eliminated, by placing an identical varactor stack in *anti-parallel* configuration, as shown in Fig. 1(b). The linear capacitance of the circuits of Figs. 1(a) and 1(b) are identical, but the circuit of Fig. 1(b) now has $C_1=C_2=0$ when the proper area ratio is set. It should be noted that *all* the even-order coefficients are zero (C_1, C_3, C_5, …) in this topology, but the higher coefficients that create odd-order distortion (C_4, C_6, C_8, …) of Fig.1(b). are *not* zero, although the IM3 contributions due to the 5th and higher order nonlinearities are very small

The implications of this analysis can be summarized as follows:

- *The classical configuration of Fig. 1(a) provides theoretically a "distortion-free" varactor stack (DFVS) when n=0.5, corresponding to a uniform doping profile of the varactors.*
- *The more generalized configuration of Fig. 1(b) provides an ultra-low distortion varactor stack for <u>any</u> value n>0.5, by setting the proper ratio of the diode areas, which sets C_1 and C_2* to zero. *This topology provides more freedom for use in different process technologies and facilitates linear operation with a higher C_{max}/C_{min} ratio than the n=0.5 case. For this reason we will refer to this topology as the high tuning range varactor stack (HTRVS) configuration.*

It should also be noted that each of the circuits in Fig. 1 requires a very high center-tap impedance (R_{BI}) for proper operation, this will be further discussed in the next section.

III. Linearity Performance of Varactor Stack Configurations

Since the capacitance of a varactor is a function of applied voltage rather then applied power, its linearity is best described as a function of the input voltage. For this reason we consider the circuits of Fig. 2, which provide the testing conditions for the single varactor, the DFVS, the HTRVS, and the DFVS with an anti-parallel diode to raise the center tap impedance. The effective zero bias capacitance of all circuits is chosen to be 10 pF.

For a given center tap bias voltage, the fundamental and IM3 components of the AC varactor current can be evaluated as function of the RF source voltage (Fig. 3.). As expected the single varactor has the worst linearity performance, and its eventual forward biasing by the RF signal results in a dramatic loss of linearity. The DFVS (n=0.5) has virtually no distortion through its near-perfect cancellation of all nonlinear coefficients and its IM2 and IM3 levels are outside the plotting range.

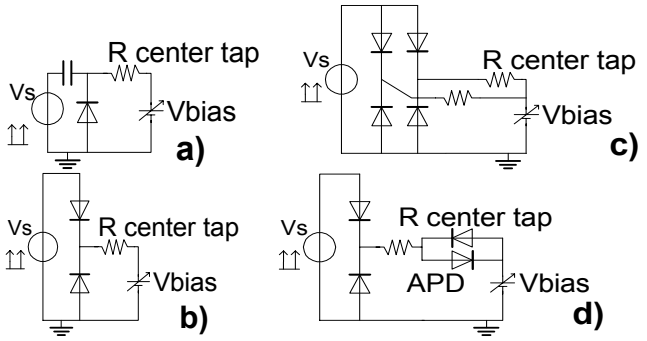

Fig. 2. Two-tone test conditions for a voltage driven, a) single varactor diode, b) DFVS, c) HTRVS, and d) a DFVS with modified center contact.

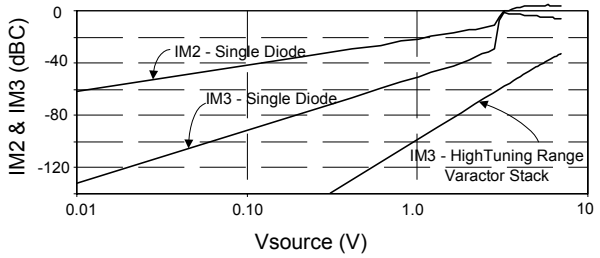

Fig. 3. Simulated $|i|_{IM2}$ and $|i|_{IM3}$ for a two-tone voltage driven single diode and High Tuning Range Varactor Stack (HTRVS) (n=1) (f_0=2GHz, Δf=100MHz). The bias voltage is 5V. Note that the Distortion Free Varactor Stack (DFVS) IM2 and IM3 distortion is not shown due to its extremely low level. The IM3 of the HTRVS is now limited by fifth-order distortion due to complete cancellation of the third-order products.

The high center tap impedance is the reason that forward biasing of one of the diodes by the RF signal has only limited impact on the DFVS and HTRVS linearity. When considering the HTRVS (n=1) we find a 1:5 slope dependence for the IM3 components, confirming the elimination of the C_1 and C_2 contributions. The intercept points of the varactor configurations are a function of the control voltage. They can be expressed analytically and are shown in Table I.

TABLE 1 THEORETICAL VOLTAGE INTERCEPT POINTS

	IP2	IP3	IP4
Single diode	$-\frac{\phi+V_{DC}}{n}$	$\sqrt{\frac{(\phi+V_{DC})^2}{2n(n+1)}}$	$2\left(\frac{-(\phi+V_{DC})}{n(n^2+3n+2)}\right)^{\frac{1}{3}}$
Distortion Free Varactor Stack	∞	∞	∞
High Tuning Range Varactor Stack	∞	∞ ,IM3 limited by 5th order	∞

A. The Influence of Center Tap Impedance on Linearity

Until now we have assumed that the biasing network of the center tap has no effect on the RF operation of the varactor stack (VS) configuration. However, in practical situations the shunting impedance of the center contact must be maximized to avoid linearity degradation. This degradation occurs when the AC current through the bias network for the various harmonic components becomes significant compared to the desired AC current through the diodes (Fig. 2). In this situation, the conditions for distortion cancellation are violated.

It is for this reason that the control voltage must be connected by a high impedance to the center contact of the VS. The most difficult conditions in this respect are found at base-band frequencies (created by the second-order distortion of the individual diodes), where the impedance of the biasing network needs to be higher than the already high impedance offered by the VS capacitance at these low frequencies. This is illustrated in Fig. 4, where the IM3 in dBc is plotted as function of tone spacing, for a 1GHz two-tone voltage driven single varactor and a DFVS with varying center tap resistances.

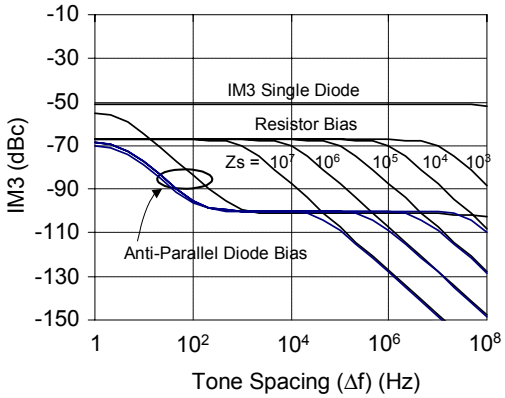

Fig. 4. Simulated IM2 and IM3 for a single varactor and a voltage driven DFVS under two-tone test as function of the tone spacing and center tap loading (f_c=1GHz, c_{eff}=10pF, Vcenter tap =5V).

Fig. 4 shows that the DFVS outperforms the single varactor in terms of linearity; however, the best results are obtained when the cut-off frequency of the dc bias network is much lower than the frequency of the envelope variation. An effective way to implement the high impedance while keeping the RC time limited for the control signal is the anti-parallel diode pair depicted in Fig 2. This is quite effective for most applications in order to meet high linearity requirements.

In addition to the requirement for a high center tap impedance, the varactor diodes should not become forward biased or exceed the diode voltage-breakdown conditions during the RF signal cycle.

IV. VARACTOR TECHNOLOGY

Since we aim for high performance adaptive matching networks and tunable filters, extreme demands are set on Q factor (>100), linearity and power handling of the varactors. In order to fulfill these requirements, a dedicated silicon-on-glass varactor technology was developed at the Delft University of Technology. This technology provides a low-loss substrate and patterning of both the front and back sides of the wafer so the intrinsic varactor can be directly contacted by thick metal on both sides. This eliminates the need for a buried layer or finger structures, as would be the case in conventional integrated varactor implementations. The cross section of a typical silicon-on-glass varactor stack is given in Fig. 5.

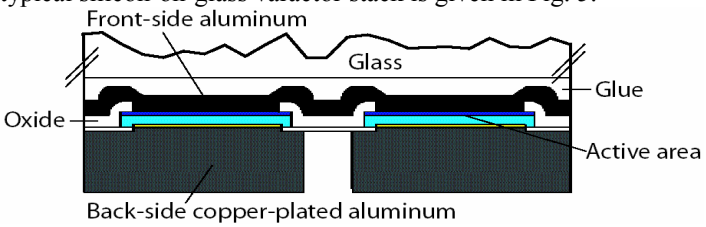

Fig. 5. Cross-section of the silicon-on-glass varactor stack.

V. EXPERIMENTAL RESULTS

The distortion-free varactor stacks (DFVS) (n=0.5) have been implemented in the technology described in the previous Section. The measured uniformity of the doping is illustrated in Fig. 6, which gives $1/C^2$ versus bias voltage. Note that a straight line for this quantity corresponds to a uniform doping, and the x-axis intercept yields the built-in potential.

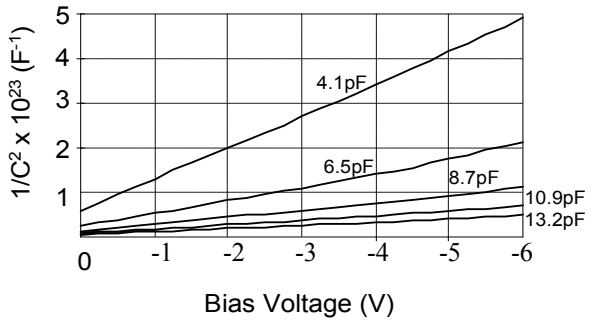

Fig. 6. Measured $1/C^2$ versus bias voltage for different capacitances. Perfectly straight lines correspond with a uniform varactor doping.

Q measurements: The realized DFVS have been measured for their Q factor and linearity at 2GHz, using a LRM calibration with Cascade Infinity probes (pitch 100 and 200μm). Since device simulations predicted a very high Q for the structure, the calibration has been extensively verified with various reference structures. In order to avoid any confusion, we only correct for the series inductance and not for the losses (series resistance) of the connecting lines. The series-inductances were found from the self-resonance of the different varactor structures. The resulting "deembedded" capacitance versus frequency behavior exhibits the desired frequency independent behavior of the capacitance. The resulting Q-factor for various DFVS structures at 2 GHz is given in Fig. 7, with typical values between 100 and 300.

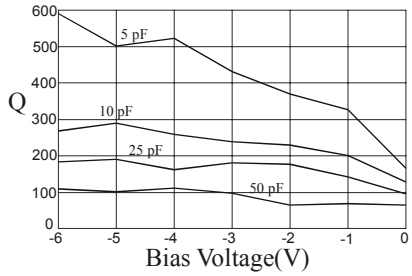

Fig. 7. Measured Q factor versus center-tap control voltage (f=2GHz), for copper-plated silicon-on-glass DFVS devices of 5, 10, 25, and 50pF with a breakdown voltage of 12V.

Large signal characterization: A two–tone test (f_c=2.14 GHz) was performed on a single varactor and a DFVS using a 50Ω terminated two-port configuration. For the calibrated power measurement of all frequency components of interest we have used the system of [6]. Fig. 8 gives the measured and simulated IM3 components as function of power for different tone-spacing (Δf=100kHz and Δf=10 MHz) using a center-tap impedance of 47kΩ and a reversed center-tap bias of 2V. These results match the theory presented earlier very well. There is a substantial improvement in linearity using the DFVS configuration over a single varactor diode.

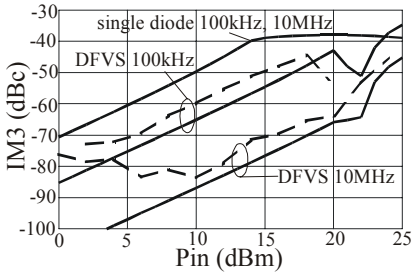

Fig. 8. Measured and simulated (solid lines) IM3 components for a single varactor and a DFVS (f_c=2.14GHz) as function of power for Δf=100kHz and 10MHz.

VI. CONCLUSIONS

Ultra low distortion varactor topologies have been presented for realizing RF adaptivity functionality in future wireless applications. A custom silicon-on-glass technology was developed for the low-loss implementation of these "distortion-free" varactor stacks, resulting in high Q's even for large capacitance values. The high performance of these structures in terms of linearity, tuning range, speed, and low costs, makes them an attractive option for the implementation of tunable filters, switches and adaptive matching networks.

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