Low-Distortion, Low-Loss Varactor-Based Adaptive Matching Networks, Implemented in a Silicon-on-Glass Technology

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Abstract — **A low-loss, low-distortion continuously tunable matching network, is demonstrated at 2 GHz in a silicon-on-glass varactor IC technology. The tuner uses an optimized varactor configuration to minimize distortion, and exhibits less than 0.5 dB loss and IM3 < -50 dBc at 27 dBm output power, and tunes with a VSWR > 250:1 to 1:1.**

Index Terms — **Adaptive systems, distortion, impedance matching, losses, nonlinearities, tuners, varactors.**

I. Introduction

Low-loss adaptive matching networks promise to solve a number of outstanding problems in the design of microwave and RF circuits. For example, they have the ability to tune the matching conditions for power amplifiers to dynamically optimize the load impedance, in order to provide the best performance at varying output powers and antenna conditions. Other uses of "adaptive" passive networks are for tunable filters, multi-band radios, and reconfigurable RF systems.

In this field, much progress has been made in adaptive matching using PHEMT [1], MEMS [2] and voltage-variable dielectric [3] technologies. Although very promising, these technologies still suffer from performance, reliability and manufacturability concerns, limiting their usefulness to specialized applications.

As alternatives to the above techniques, we have recently demonstrated in [4] that varactor based tunable capacitors, can be implemented with a very high Q (>100 @ 2GHz) and extremely low-distortion in a low-cost silicon-based technology. In this paper we use these varactor based tuning elements for the implementation of two adaptive matching networks. The resulting networks are compact (< 3.5 mm2), continuously tunable, and meet the power and linearity requirements for a typical handset output stage.

In this paper we discuss the technology constraints for the implementation of these networks, their design and measured performance in terms of impedance tuning range, losses and linearity. All networks are implemented using an in-house customized silicon-on-glass technology [4].

II. "Distortion Free" Varactor Diodes

At lower power levels the use of varactor diodes for capacitance tuning is common practice in many RF circuits. Unfortunately, conventional varactor tuning has the drawback of a highly nonlinear operation, which disqualifies it for use in linear applications at higher power levels, like RF front-ends and adaptive matching networks. Meyer *et. al.* showed that uniformly doped varactor diodes with a capacitance voltage power-law coefficient ($n=0.5$), exhibit essentially no distortion when operated in the *anti-series* configuration [5]. Recall, that the C(V) of a single varactor diode is given by:

$$C(V) = \frac{K}{(\phi + V)^n} \qquad (1)$$

where, ϕ is the built-in potential of the diode, V is the applied voltage, n is the power law exponent of the diode capacitance, and K is the capacitance constant. The power law exponent n can exhibit wide variation in different situations, from a value of $n \bullet 0.3$ for an implanted junction to $n \bullet 0.5$ for a uniformly doped junction to $n \bullet 1.5$ for a hyper-abrupt junction.

In [4] a modified version of the anti-series diode configuration ($n=0.5$), with an improved center tap connection for higher linearity at low tone spacing was introduced. This modified topology, referred to as *distortion-free varactor stack* (DFVS) (see also Fig. 1), behaves as linear capacitor between the two end nodes while its value can be varied continuously by the applied voltage at the center-tap. In [4] additional combinations of properly scaled anti-series diodes are given, which provide very low distortion properties for varactors with higher grading coefficients ($n>0.5$). Since higher grading coefficients result in a higher tuning range of the capacitance, these later topologies provide more design flexibility, and are therefore extremely promising for many RF applications. In this work we employed uniformly doped varactors ($n=0.5$) in a DFVS configuration for our adaptive matching networks in order to achieve the highest linearity and the lowest sensitivity to process variation.

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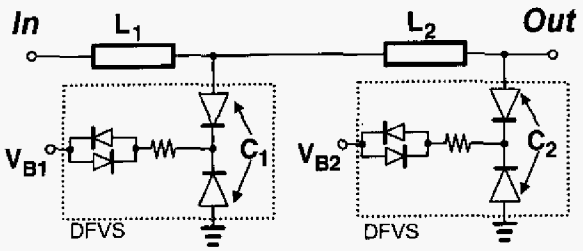


Fig. 1. Schematic diagram of varactor diode-based tuners. The two versions of the tuner are designed for a load impedance of either 50 Ω or 25 Ω. The element values for the tuner are given in Table I.

Element	25Ω structure	50Ω structure
L_1	612 μm	450 μm
C_1	43.5 pF	72.9 pF
L_2	2491 μm	2018 μm
C_2	32.5 pF	32.5 pF

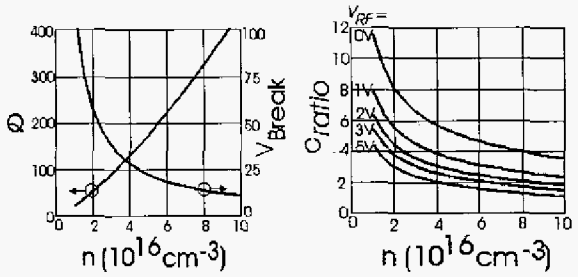
Table I: Component values of the integrated tuners, the other coplanar transmission line parameters are; $Width_{line}$=265μm, Gap_{line}=143 μm. The capacitance values are zero-bias values.

III. VARACTOR TECHNOLOGY CONSIDERATIONS

Integrated tuner design for linear high power applications is subject to many design constraints, due to the harsh signal conditions that occur with high impedance transformation ratios. These high ratios often translate into high Q conditions, which are accompanied by high voltages and currents. These conditions require ultra low loss, as well as high breakdown voltage of the network elements. In addition, we have to adjust our design so that forward biasing of the diodes by the RF signal is avoided, forward biasing of one of the diodes will eliminate the IM3 cancellation in the varactor stack, yielding high distortion. Consequently, the varactor diodes should not become forward biased nor exceed the diode voltage breakdown (V_{break}) conditions during the RF signal cycle. Since the RF voltage amplitude limits the "safe" linear operation region of the varactors, the effective tuning ratio of the varactor capacitance (c_{ratio}):

$$c_{ratio} = \frac{C(V_{cont\_min})}{C(V_{cont\_max})} \qquad (2)$$

is reduced. With C(V) given by (1), the control voltages are limited by $V_{cont\_min} = \hat{V}_{RF}/2$ and $V_{cont\_max} = V_{break} - \hat{V}_{RF}/2$, where $\hat{V}_{RF}$ is the voltage amplitude of the applied RF signal, where we assume that the RF voltage is divided equally between the two diodes. These considerations demonstrate that the effective tuning range can be improved by increasing the breakdown voltage of the diodes, by lowering the doping concentration of the epilayer and increasing its thickness. However, this will result in a higher series resistance – and lower Q – and the need for higher control voltages. Since both effects are undesired, it is important to limit the RF voltage swing on the DFVS in the matching network. To assess the influence of the RF voltage amplitude, Fig. 2 shows the calculated breakdown voltage, zero bias Q factor and the effective capacitance ratio for different RF voltage amplitudes as function of doping for a silicon based device. For our experimental work, based on the two-stage ladder-matching network of Fig. 1, we chose a doping level of 4.10^{16} cm^{-3} to obtain a good tradeoff between tuning range, varactor Q>100 @ 2GHz, and breakdown voltage (~30V).



a) b)

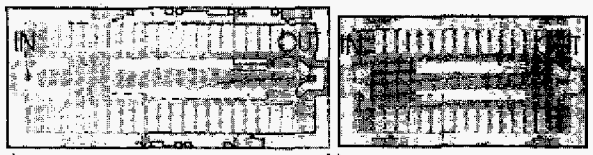
Fig. 2. a) Calculated varactor breakdown voltage and related zero bias Q factor of the intrinsic device. b) Effective c_{ratio} for different RF voltage amplitudes as function of doping.

IV. ADAPTIVE MATCHING NETWORK DESIGN

The tuner of Fig. 1 consists of low-loss coplanar transmission lines and varactor diode tuning to continuously vary the impedance transformation. This topology has been selected for its ease of implementation and the low Q it offers for the high input power/low input impedance condition (see Fig. 4.a). Furthermore, due to the shunt configuration of the varactor stack, it is less sensitive to varactor parasitics since these are also shunted to ground. There are only two control voltages and the total structure is very compact (< 3.5 mm^2). One of the nice features of this structure is that it provides an ohmic loading condition at its input port ranging from below one ohm to tens of ohms. Since the tuning speed can be very high, this also makes the network a potential candidate for use with dynamic load-line amplifier concepts [6]. Two

circuits based on the topology of Fig. 1, have been implemented with approximately the same power handling capabilities. One tuner is designed for a 50Ω output loading, and the other is designed for a 25Ω output loading (for more relaxed element values (see Table I)). Both tuners fulfill the following constraints:

- tuning range varactors (c_{max}/c_{min}): < 2.5
- design frequency: 2 GHz
- control voltages: < 18 V
- impedance transformation ratio: > 10
- no-forward biasing of one of the diodes by RF input powers up to 1 W.



a) b)

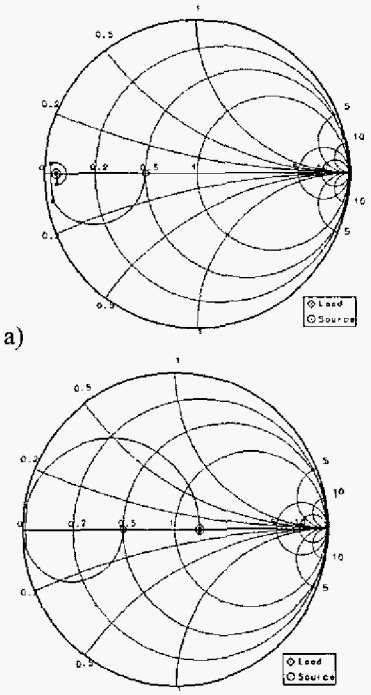
Fig. 3. Layout's of the tuners and filter: a) 25Ω structure, b) 50Ω structure.

V. Experimental Results

The tuner circuits of Fig. 1 were fabricated in the high performance silicon-on-glass technology described in [4]. This technology provides a low-loss substrate and accurate processing of both the front and backsides of the wafer so the intrinsic varactor can be directly contacted by thick metal on both sides. This eliminates the need for a buried layer or finger structures, as would be the case in conventional integrated varactor implementations. A 4μm copper layer has been plated on 1.4μm aluminum, to minimize the transmission line losses. The diodes were designed for a uniform doping profile – to realize a value of $n=0.5$ – but due to the limited availability of wafers at the time of processing, a grading coefficient of $n\approx0.6$ was used. The realized tuners circuits are given in Fig. 3.

The measured Q and $1/C^2$ versus voltage of a 19pF test DFVS are given in Fig. 5 The measured $1/C^2$ plot shows a deviation from the ideal straight line of the uniformly doped case. This is also reflected by the somewhat reduced zero bias quality factor of the varactors. This is expected to slightly degrade the linearity of the tuner; but fortunately the linearity of the anti-series configuration is quite insensitive to these deviations as will be shown by the following results.

Fig. 6 shows the measured values of s_{11} at 2 GHz for the two tuners. Note the close-to-ideal distribution of impedance points, which cover the ohmic control range of



a) b)

Fig. 4. Simulated Smith chart trajectory with variation in diode capacitance for the 25Ω structure; a) low input impedance (2Ω) mode, b) high input impedance (50Ω) mode. Note the high-Q (trajectory very close to the edge) in the 50Ω mode.

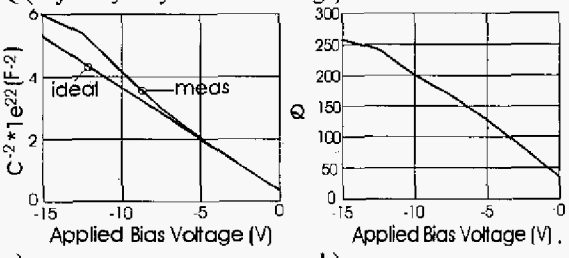


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Fig. 5. a) Measured $1/C^2$ and b) Q @ 2GHz of a 19pF DFVS element versus bias voltage. Note the slight deviation from the ideal straight line from 0 to -15V. Beyond -15V, the diode is "punched through" and there is little capacitance variation.

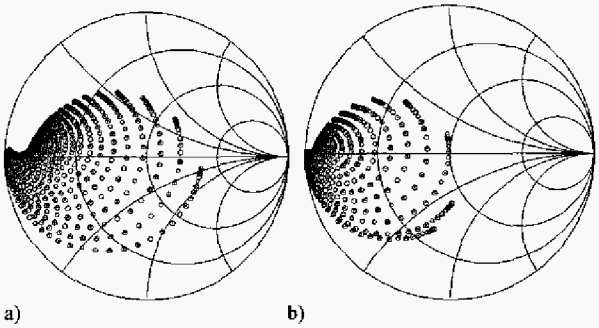

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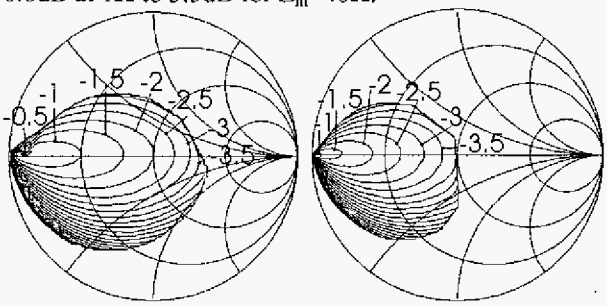
Fig. 6. Measured s_{11} at 2GHz for the integrated silicon-on-glass tuners; a) tuner designed for 25 ohm loading, b) tuner designed for 50 ohm output loading.

0.2 to 82 ohm and 0.2 to 49 ohm for the 25Ω tuner and 50Ω tuner respectively. From this data, we observe for both tuners a VSWR > 250:1.

One of the most important aspects of tuner design is to maximize the power gain (P_{out}/P_{in}) or minimizing the losses of the structure. The definition of this gain is:

$$G_p = \frac{|S_{21}|^2}{1-|\Gamma_{in}|^2}. \qquad (3)$$

Note that G_p is a more appropriate measure for this network than G_{max}, which assumes conjugate matching conditions at both input and output. (G_{max} for both structures was approximately 0.2 dB for all tuning values). Maximizing the Q of the varactor diodes and minimizing ohmic losses in the transmission lines results in the lowest losses. Fig. 7(a) plots the measured loss contours at all the different tuning points, for the 25Ω structure, the losses vary from 0.4dB at 3Ω to 2dB for Z_{in}=50Ω. The losses for the 50Ω tuner are plotted in Fig. 7(b) and range from 0.6dB at 1Ω to 3.5dB for Z_{in}=40Ω.



a) b)

Fig. 7. Measured loss contours (G_p in dB) at 2GHz for the integrated silicon-on-glass tuners; a) tuner designed for 25 ohm loading, b) tuner designed for 50 ohm output loading.

At first glance, it is somewhat surprising that the highest losses are found for the lowest impedance transformation ratios. This is a consequence of the applied optimization of these matching networks which was focused on achieving low Q conditions for high input power levels (low input impedances). As result high Q conditions arise for the low input power condition (high input impedances Fig. 4b). Other possible configurations can solve this limitation by using a low Q matching solution for all power levels.

The large-signal performance of the tuners has also been measured. Fig. 8 plots the IM3 versus output power for the 50Ω structure as function of output power at low (2Ω) and high (37Ω) input impedance conditions. The IM3 components are below 50dBc for both 27 dBm output power (2Ω input) as well 17 dBm (37Ω input), which represents the 10dB power back-off condition. This performance is compatible with the linearity constraints of most communication standards for handsets.

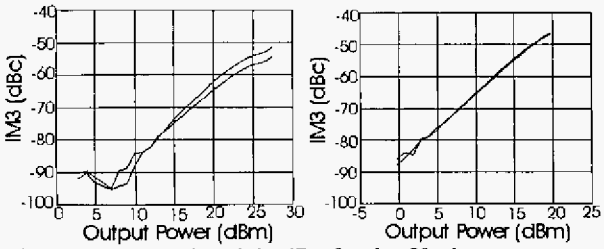


Fig. 8. Measured IM3 in dBc for the 50 ohm tuner structure f_c=2GHz Δf=20MHz; a) Z_{in}=2Ω, b) Z_{in}=37Ω.

VI. Conclusions

An ultra low distortion varactor configuration has been applied in combination with a novel, very low-loss, silicon-on-glass technology for the implementation of integrated tuners for adaptive matching. The measured close-to-ideal continuously variable tuning capabilities make these networks very suitable for providing optimum loading conditions to the output stage, under varying output power or antenna matching conditions. The achieved performance of these networks in terms of loss, size, cost, tuning range, power handling and linearity, makes them attractive candidates for a variety of future adaptive tuning applications.

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References

[1] C. McIntosh, et. al., "Novel MMIC source-impedance tuners for on-wafer microwave noise-parameter measurements", *IEEE Trans. MTT*, Vol. 47, Feb. 1999.

[2] J. Papapolymerou, et. al., "Reconfigurable double-stub tuners using MEMS switches for intelligent RF front-ends", *IEEE Trans. MTT*, vol.51, Jan. 2003, pp. 271- 278.

[3] P. Pamini et. al., "Realization of High Tunability Barium Strontium Titanate Thin Films by RF Magnetron Sputtering", *Applied Physics Letters*, Nov. 1999.

[4] K. Buisman, et. al., "'Distortion Free' varactor diode topologies for RF adaptivity", submitted to *2005 IEEE IMS*.

[5] R.G. Meyer et. al., "Distortion in Variable Capacitance Diodes", *IEEE JSSC*, vol. Sc-10, no.1 Feb. 1975.

[6] F. H. Raab, "High-Efficiency Linear Amplification by Dynamic Load Modulation", *IEEE IMS 2003*.