Improved Digital-IF Transmitter Architecture for Highly Integrated W-CDMA Mobile Terminals

Vincent W. Leung, *Member, IEEE*, Lawrence E. Larson, *Fellow, IEEE*, and Prasad S. Gudem

***Abstract*—An improved digital intermediate frequency (IF) transmitter architecture for wide-band code-division multiple-access (W-CDMA) mobile terminals is proposed. Based on the heterodyne design but without requiring any off-chip IF filter, the transmitter enjoys the advantages of a homodyne architecture (such as circuit simplicity, low power consumption, and a high level of integration) while avoiding the performance problems associated with direct upconversion. By implementing the quadrature modulation in the digital domain and requiring only a single path of analog baseband circuits, inherently perfect I/Q matching and good error vector magnitude (EVM) performance can be achieved. The IF is chosen to be a quarter of the clock rate for a very simple and low-power digital modulator design. The difficulties of on-chip IF filtering were greatly alleviated by 1) performing a careful frequency planning and 2) employing a special-purpose digital-to-analog converter to produce high-order $\sin(x)/x$ rolloff. System-level simulation demonstrates that spurious-emission requirements are met with virtually no dedicated reconstruction filter circuits. This architecture takes full advantage of complimentary metal–oxide–semiconductor technology scaling by employing digital processing to ease analog complexities.**

***Index Terms*—Digital intermediate frequency (IF), digital-to-analog conversion, error vector magnitude, frequency allocation, heterodyne, high-order hold, mobile radio, quadrature modulation, radio transmitters, wide-band code-division multiple access (W-CDMA).**

I. Introduction

THE expansion of the mobile communication market has been remarkable. From originally providing voice service, the wireless industry has gradually evolved to enable high-bit-rate multimedia communications such as electronic mail (e-mail), Internet access, and image and video transfers. Within the third-generation (3G) framework, the wide-band code-division multiple-access (W-CDMA) system has emerged as a standard and early deployment has already begun.

There is enormous pressure to reduce the size, cost, and power consumption of mobile phones. While the digital circuits have experienced tremendous power saving and enhanced functionalities with the progress of deep submicrometer processes, the analog/radio-frequency (RF) sections remain the bottleneck. In this paper, we focus on an improved W-CDMA transmitter IC (TxIC) architecture for handset applications.

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The authors are with the Department of Electrical and Computer Engineering, University of California at San Diego, La Jolla, CA 92093 USA (e-mail: vleung@ece.ucsd.edu).

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Existing TxIC solutions commonly require external filters at the intermediate frequency (IF) for rejection of spurious components [4]–[6]. While being a time-proven approach, those off-chip components (for instance, IF SAW and LC tank) are bulky and expensive; they substantially increase the feature size and cost of the final cell phone product.

TxIC solutions that are available today tend to be power-hungry and complicated. This is mainly due to the heterodyne architecture, which demands two pairs of analog/RF mixers and synthesizers. Furthermore, the power consumption can be substantially driven up if an active IF filter is integrated.

A highly integrated, simple, and low-power W-CDMA TxIC solution for mobile station applications is proposed. This is achieved through a novel architecture that alleviates some of the analog circuit complexities by high-speed digital signal processing. We believe that this is an appealing technological direction because the resulting TxIC solution can then take full advantage of the rapid advancement of fine-geometry IC technologies.

This paper is organized as follows. Section II reviews the existing TxIC solutions developed by both the industry and academia. This is to illustrate the issues faced by W-CDMA transmitter architecture design. Section III presents the improved transmitter architecture based on the digital IF scheme. The design innovations developed to enhance the level of integration and to reduce circuit complexity will be discussed in detail. System-level simulations on the spurious emission are presented in Section IV and concluding remarks are made in Section V.

II. Survey of TxIC Architectures for W-CDMA Mobile Phones

Table I presents a list of published W-CDMA handset transmitter designs in the literature [1]–[10]. Almost all W-CDMA TxICs are heterodyne [1]–[8], performing upconversion in two steps similar to that shown in Fig. 1. Baseband data are first upconverted by quadrature modulation to the intermediate frequency, typically at hundreds of megahertz. The in-phase (I) and quadrature-phase (Q) signals are then summed and further upconverted to the desired transmit channel by a single-sideband (SSB) mixer.

Among the heterodyne TxICs listed in Table I, different levels of transmitter functions are integrated. The designs of [1]–[3] include the IF quadrature modulator only, while the chips of [4]–[8] have *both* the IF and RF upconversion sections integrated. External RF SAW filters (following the RF upconversion) are required in the TxICs of [4] and [5] as no on-chip inductance–capacitance LC filtering [6] or SSB mixer [7] are

TABLE I
COMPARISON OF W-CDMA TXIC ARCHITECTURE

Company/ Institution [ref.]	Architecture	Ext. RF SAW needed?	Ext. IF filter needed?	Num. of analog mix/ syn. needed?	EVM performance under:		Dynamic range
					I/Q mismatch	LO leakage	
Infineon [1]	Heterodyne	N/A (No RF section)	Yes	2 / 2	Good	Good	70 dB
IME Singapore [2]	Heterodyne		Yes	2 / 2	Good	Good	68 dB
Mitsubishi [3]	Heterodyne		Yes	2 / 2	Good	Good	90 dB
Mitsubishi [4]	Heterodyne	Yes	Yes	2 / 2	Good	Good	100 dB
IBM [5]	Heterodyne	Yes	Yes	2 / 2	Good	Good	95 dB
TI [6]	Heterodyne	No	Yes	2 / 2	Good	Good	90 dB
Philips [7]	Hetero. var. IF	No	No	1 / 2	Fair	Good	81 dB
IBM [8]	Hetero. var. IF	No	No	1 / 2	Fair	Good	115 dB
Swiss Inst. Tech. [9]	Homodyne	No	No	1 / 1	Bad	Bad	78 dB
Seoul Nat. U. [10]	Homodyne	No	No	1 / 1	Bad	Good	50 dB
This work	Hetero. dig. IF	No	No	1 / 1	Ideal	Good	90 dB

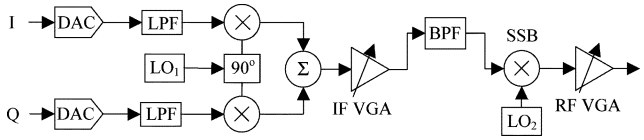

Fig. 1. Block diagram of a conventional heterodyne transmitter.

featured. Some of the TxICs also distinguish themselves by integrating the synthesizer [1], [3], [6], [7] or the reconstruction filter for D/A conversion [1].

The heterodyne architecture offers many advantages. Since the frequencies of the local oscillators (LOs) are far from the final transmit signal, injection locking [11] (i.e., the LO shifts toward the frequency of the noise injected by the strong power amplifier output) can be avoided. Also, the somewhat inevitable LO leakage would not degrade the error vector magnitude (EVM) performance because it does not overlap with the transmit signal spectrum. I and Q matching is superior (if careful design and layout practices are employed) because quadrature modulation is performed at lower (intermediate) frequencies [12]. But most importantly, the very wide gain-control range of 76 dB mandated by the W-CDMA standard [13] can be readily implemented despite the limited substrate isolation. (In fact, to provide adequate design margin for process, supply, and temperature variations, it is not uncommon to find more than 90 dB of nominal dynamic range in TxIC solutions [4]–[6], [8].) This last point is explained later.

Signal isolation on a silicon substrate can be as low as 40–50 dB RFs [14], [15] and it is impossible for a variable gain amplifier (VGA) to attenuate beyond the level of isolation. For example, an RF VGA circuit may attenuate its input by, say, 60 dB. The input signal, however, can appear at the output (reduced only by 40 dB of isolation) directly through the substrate, thus inundating the desired output. Therefore, substrate isolation dictates the maximum achievable VGA attenuation. It is clear that the gain control mandated for W-CDMA transmitters cannot be carried out solely at RF.

The heterodyne architecture overcomes the substrate-isolation problem by effectively distributing the total gain range among two separate frequency bands (IF and RF). As such, the RF VGA can be designed to cover a much smaller gain-control range (so that substrate isolation is no longer an issue), while the rest of the gain control can be attributed to the IF VGA (which generally experiences a less severe signal coupling problem because of the lower frequency of operation).

However, the heterodyne architecture is not without drawbacks. It often demands external IF filters to remove the spurious responses. These off-chip components would substantially increase the size and cost of the chipset. They also pose reliability issues as high-frequency signals (in the hundreds of megahertz range) must now travel off-chip.

Two approaches have been attempted to eliminate these external passive components. The design of [7] employs an active IF poly-phase filter. As shown in Fig. 2(a), the IF section is fully complex. That is, the I and Q signals will not be summed until they have been upconverted to RF. We believe that this architecture is more vulnerable to mismatch issues than other conventional heterodyne implementations, because of the extended I/Q paths. Besides, the high-Q IF bandpass filter function demands ultrawide-band opamps (with open-loop gain bandwidth product of 11.3 GHz). The design is nontrivial and may noticeably increase the overall power budget.

On the other hand, the design of [8] eliminates the need of the off-chip IF filter by adopting a meticulous frequency-planning scheme, which is shown in Fig. 2(b). Local oscillator frequencies are carefully selected so that they do not have a direct harmonic or subharmonic relation to the RF output frequency. Together with good circuit linearity and quadrature balance, the co-

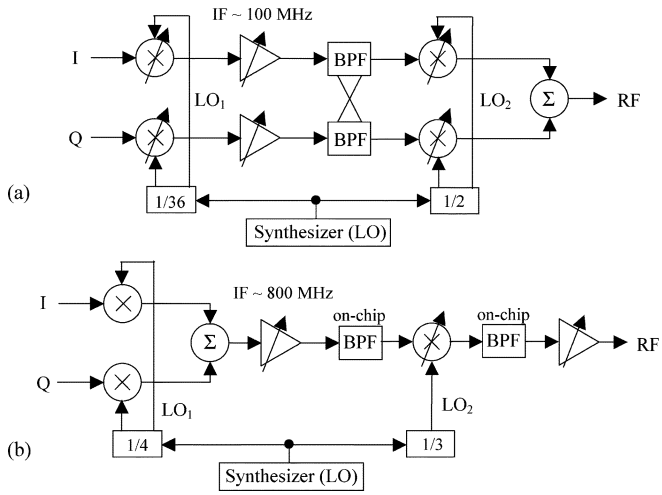

Fig. 2. Two variable-IF heterodyne architectures that eliminate the external IF filter by (a) implementing a complex-IF filter and (b) adopting a frequency-planning scheme.

pious spurs resulting from the IF and RF upconversions can pass the W-CDMA spurious specifications with very little amount of on-chip filtering (by, say, LC tanks). The final TxIC solution requires only an absolute minimum of external filtering (namely, one SAW filter between the TxIC and the power amplifier and an antenna duplexer filter). However, we believe that this architecture is also more susceptible to the I/Q mismatch problem, as will be discussed soon.

The second drawback of the conventional heterodyne architecture is that two synthesizers (IF and RF) are needed [4]–[6], resulting in relatively complicated and high power consumption designs. The "complex-IF" and "minimum-filtering" designs of [7], [8] both mitigate this problem by employing a "variable IF" architecture, in which both stages of upconversion mixers are driven by a common synthesizer. The mixer frequencies (i.e., LO_1 and LO_2 of Fig. 2) are harmonically related to some higher frequency local-oscillator input (LO), so that

$$\begin{aligned} k \cdot \mathrm{LO}_1 = l \cdot \mathrm{LO}_2 &= \mathrm{LO} \\ \mathrm{LO}_1 + \mathrm{LO}_2 &= f_{\mathrm{ch}} \end{aligned} \tag{1}$$

where parameters k and l are integers. As such, the mixer frequencies will move together as a different channel frequency (f_{ch}) is desired.

In the design of [7], parameters k and l are 36 and 2, respectively. As the W-CDMA transmit channel is between 1920–1950 MHz, the intermediate frequency (i.e., LO_1) would be around 100 MHz. This is considered a low frequency, for which the circuit design (in particular, the quadrature modulator design) is relatively simple. However, for [8], in order to satisfy the spurious requirements, the parameters are chosen to be 4 and 3, respectively. This moves the intermediate frequency in excess of 800 MHz. In comparison, the quadrature modulator is likely to be more sensitive to circuit parasitics and I/Q imbalances and would consume more power.

On the other hand, if the baseband I/Q signals are upconverted to the RF *directly*, the previously discussed problems (namely, the external SAW filter and multiple synthesizers) could be avoided. The so-called homodyne architecture is shown in Fig. 3. Obviously, it demands no IF filtering and requires only one synthesizer. Therefore, this architecture lends itself very efficiently for single-chip integration [9], [10]. To avoid LO-pulling by the power amplifier output, a classic problem in the direct-conversion transmitter, a divider circuit is employed [9].

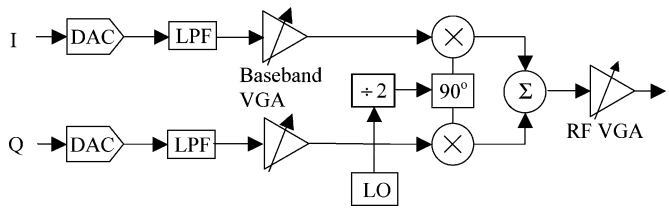

Fig. 3. Block diagram of a typical homodyne transmitter.

Nevertheless, the homodyne transmitter suffers serious performance issues (namely, the gain control I/Q matching and LO leakage) not experienced by its heterodyne counterpart, as will be explained later.

Notice that, due to the limited substrate isolation discussed before, most of the W-CDMA gain control must now be implemented at the baseband (dc) [12], as shown in Fig. 3. For instance, the design of [9] achieves its entire gain programmability at the baseband: 30 dB of dynamic range at the reconstruction (D/A) filter and 48 dB at the modulator (I-to-V) input. In the IC example of [10], the baseband VGA alone handles 35 dB of the 50-dB total transmitter dynamic range. Because of their much wider gain programmability, these baseband components often have more stringent linearity requirements than their heterodyne counterparts.

Since a substantial amount of gain control must now be applied separately to the I and Q (baseband) signals before they are summed and the quadrature modulator operates at much higher (radio) frequencies, I/Q mismatch is going to be nonnegligible. (In contrast, the heterodyne transmitter of Fig. 1 assumes a sum-before-gain approach at IF. Therefore, far less I/Q mismatch will be experienced.) The sideband rejection, or the related EVM[1] performance, is determined by the mismatch parameters according to [16]

$$\mathrm{EVM} \approx 20 \cdot \log_{10} \sqrt{\frac{\alpha^2 + \phi^2}{2}} \tag{2}$$

where α is the magnitude mismatch in percentage and ϕ denotes the phase mismatch in radians. We assume that ϕ can be as high as 2° at the RF quadrature modulator. Then, according to (2), a magnitude mismatch as small as 3% will degrade an otherwise ideal EVM to the unacceptable level of -30 dB (3.3%). Notice that for a gain of -40 dB, a 3% mismatch translates to a gain difference between 0.01 V/V to 0.0103 V/V. This matching accuracy is deemed difficult even with very good design and layout practice.

[1]The EVM performance is dominated by the noise floor, sideband suppression, and carrier-leakage characteristics of the I/Q modulator at low output power levels. The total EVM performance is specified to be less than 17.5% [13]. To allow a large margin to account for power amplifier distortion, it is important to ensure that the carrier leakage and sideband suppression of the TxIC should exceed 35 dBc [8].

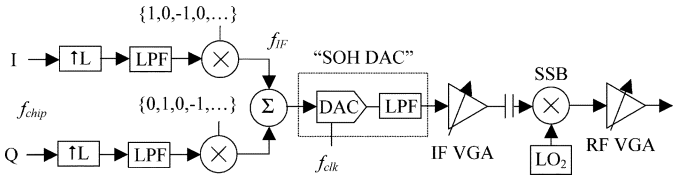

Fig. 4. Heterodyne transmitter with digital IF modulator.

LO leakage (to the RF port) is caused by direct substrate coupling or the baseband and modulator circuits dc offset. It is particularly troublesome for the homodyne transmitter because the LO always lies in the transmit band. It can severely degrade the EVM performance, especially if the baseband section is set into the low-gain mode. This performance issue is addressed in the design of [10]. For instance, assume that the baseband VGA attenuates the 1 V DAC output (by 40 dB) into 10 mV and the LO signal measures 200 mV. Substrate coupling as low as -50 dB (or, to the same effect, a dc offset as small as 0.6 mV) will degrade the otherwise ideal EVM to about -24 dB (or 6.3%), which is not acceptable. This simple example highlights the very challenging LO–RF isolation and circuit offset requirements.

In this work, we propose an improved heterodyne transmitter IC (TxIC) architecture that leverages the rapid technology advancement in CMOS by implementing the IF upconversion digitally. By means of a simple digital quadrature modulator, a careful frequency planning, and a second-order-hold D/A converter, our architecture: 1) eliminates the external IF filter; 2) demands only one synthesizer; 3) employs only one RF (single-sideband) mixer; and 4) achieves inherently perfect quadrature I/Q matching (for good EVM performance). In short, our TxIC inherits the advantages of the homodyne architecture without suffering the accompanying performance degradations.

III. Digital-IF Transmitter Architecture

A. Transmitter Architecture Overview

Fig. 4 shows the proposed architecture, which is a digital IF heterodyne transmitter. Digital data (with chip rate $f_{\rm chip}$ equals 3.84 MHz) are upsampled (interpolated), filtered, multiplied with the quadrature LOs, and then summed together before they reach the digital-to-analog converter (DAC). As such, the DAC should be designed to handle the (much faster) IF signal, although only one DAC is needed (instead of two; see Fig. 1).

Since the quadrature upconversion is performed digitally and there is no separate I and Q analog path, perfect I/Q matching and EVM performance can be achieved[17].[2] This desirable characteristic has found wide usage in wide-band orthogonal frequency-division multiplexing (OFDM) and base station transmitter design, where much tougher EVM performance is demanded.

In addition, alternating current (ac) coupling is possible because the analog signal is no longer centered at dc. As a result, the dc offset of the analog circuits before the SSB mixer is eliminated and, consequently, will not cause LO leakage.

To fully realize the potential of our architecture for the W-CDMA handset applications and to achieve the objectives that we stated earlier, we are proposing several innovative design ideas, which will be discussed next.

B. Digital Quadrature Modulator

In general, the digital modulator demands numerical oscillators and multipliers, resulting in a complicated and power-hungry design. However, it can be significantly simplified if we impose

$$f_{\rm IF} = \frac{f_{\rm clk}}{4}. \tag{3}$$

That is, if the intermediate frequency ($f_{\rm IF}$) is to be a quarter of the DAC clock rate ($f_{\rm clk}$), the LO signals can be completely represented by values of $+1$, 0, or -1. Therefore, the digital modulator is a trivial sign-bit-flipping logic,[3] thus eliminating the need for a direct digital synthesis (DDS) or a general digital multiplier. This idea has been known and practiced in the industry to considerably lower the power budget and design complexity of the modulator.

Under this scheme, we do not have freedom to choose the frequency (or the phase) of the LO signals once the DAC clock rate is determined. However, for the mobile phone applications, this is not an issue at all. This is because only one channel is transmitted per station at a time and the RF mixer with its variable LO (i.e., LO_2 of Fig. 4) will subsequently upconvert the IF signal to any desired channel frequency.

C. Problem of Reconstruction (IF) Filtering

In a digital-to-analog conversion system, repeating IF spectra would appear around the multiples of the clock frequency. These "digital images" would occupy frequencies of $f_{\rm clk} \pm f_{\rm IF}, 2f_{\rm clk} \pm f_{\rm IF}$, and $3f_{\rm clk} \pm f_{\rm IF}$, etc. To prevent them from interfering with other sensitive frequency bands and to meet the spurious emissions requirements, low-pass (reconstruction) filtering is required following the DAC.

Although the condition imposed in (3) allows easy digital modulator design, the reconstruction filtering can become difficult due to the low oversampling ratio (OSR $= (f_{\rm clk}/2)/f_{\rm IF} = 2$). The DAC digital images will appear very close in frequency to the desired signal. If they are to be sufficiently attenuated on-chip, a high-order linear-phase automatically tuned filter is necessary. To appreciate this problem in our W-CDMA mobile phone environment, where the transmit (Tx) band is between 1920–1980 MHz and the receive (Rx) band is 2110–2170 MHz, we consider two scenarios. The discussion will subsequently lead us to choosing an optimal IF (thus, the DAC clock speed and the interpolation factor L) for easy reconstruction filter design.

[2]In the SSB mixer, a 90° phase shifter will act on the single analog input and generate two quadrature signals. The inevitable I/Q mismatches of the circuit would result in a residual (imperfectly rejected) sideband. It would not, however, impact the EVM performance of the desired transmit channel.

[3]In fact, the quadrature LO signals can be equivalently represented by sequences of $\{+1, +1, -1, -1, +1, +1, \ldots\}$ and $\{-1, +1, +1, -1, -1, +1, \ldots\}$. Therefore, multiplication is simply accomplished by inverting the sign bits of every two consecutive input baseband data.

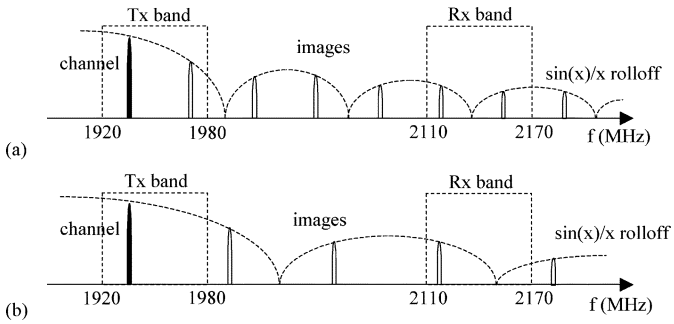

Fig. 5. Locations of digital images when (a) $L = 16$, and (b) $L = 32$. The "black" signal is the desired signal and the "white" are the digital images.

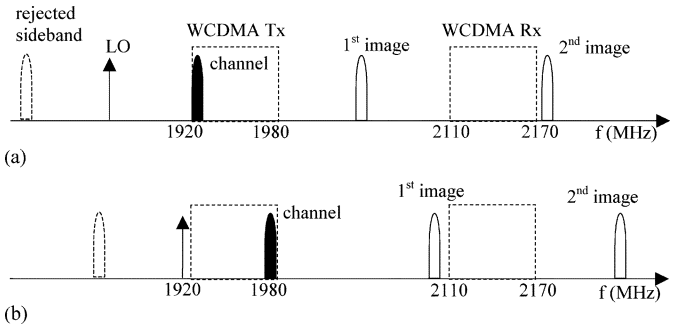

Fig. 6. Frequency planning: locations of images when the channel is at (a) the lower or (b) upper edge of the W-CDMA Tx band.

Case 1: If an interpolation factor of 16 ($L = 16$) is chosen, the DAC clock will be running at $3.84 \times 16 = 61.44$ MHz, giving an IF of 15.36 MHz. For a Tx channel located at, say, 1940 MHz, the first image will also appear in the Tx band. This is shown in Fig. 5(a). To ensure 55 dB of image attenuation at Tx band and a level of phase linearity yielding -42 dB EVM, a fifth-order Butterworth low-pass filter with a 18-MHz cutoff frequency is demanded. While such a design is not technically prohibitive, a fully monolithic version of the filter is certainly nontrivial and should be avoided if possible.

Case 2: If the interpolation factor is chosen to be 32, the DAC clock rate is 122.88 MHz and the intermediate frequency is 30.72 MHz. The Tx spectrum is shown in Fig. 5(b). Here, although no image falls into the Tx band, the image in the Rx band still needs to be sufficiently filtered. To achieve 61 dB of attenuation with -42 dB of EVM performance, a fourth-order Butterworth low-pass filter with 40-MHz cutoff frequency is required. Despite its lower order, this filter design is no simpler because of the higher cutoff frequency.

Recently, high-speed active filters have received a lot of research attention and very good results in terms of power consumption and performances have been reported [18]. In this work, however, we adopt an alternative design approach. Instead of building a sophisticated filter for reconstruction, we derive ways to make the task of reconstruction filtering much easier. This goal is to be achieved by: 1) performing optimized frequency planning and 2) employing a high-order-hold DAC. Both will be discussed later. We believe that our design paradigm is practical and has good potential for realizing an overall simple and low-power digital-IF upconverter solution.

D. Frequency-Planning Scheme

If the clock frequency is strategically selected so that the DAC images will appear out of the frequency bands of interest, the filter requirement could be substantially relaxed. Our goal is to make sure that no DAC images will land into the sensitive transmit and receive bands for all transmit channel locations. This can be met if the Rx band is always between the first and second images for all channel locations, as shown in Fig. 6. Notice that after RF upconversion, the first and second images are given by

$$\begin{aligned} f_{\text{imag1}} &= \frac{f_{\text{ch}} + f_{\text{clk}}}{2} \\ f_{\text{imag2}} &= f_{\text{ch}} + f_{\text{clk}} \end{aligned} \tag{4}$$

where f_{ch} denotes the channel location, which is between 1920–1980 MHz (Tx band). To ensure that the first image is always below the lower edge of the Rx band, we can write

$$\begin{aligned} f_{\text{ch}} + \frac{f_{\text{clk}}}{2} &< 2110 \\ f_{\text{clk}} &< (2110 - 1980) \times 2 \\ f_{\text{clk}} &< 260\ (\text{MHz}). \end{aligned} \tag{5}$$

Similarly, to ensure that the second image is always above the upper edge of the Rx band, we can write

$$\begin{aligned} f_{\text{ch}} + f_{\text{clk}} &> 2170 \\ f_{\text{clk}} &> 2170 - 1920 \\ f_{\text{clk}} &> 250\ (\text{MHz}). \end{aligned} \tag{6}$$

Combining the results found in (5) and (6), we arrive at

$$250 < f_{\text{clk}} < 260\ \text{MHz}. \tag{7}$$

In summary, if the clock rate is set to be between 250–260 MHz, no digital images will land into the Tx or Rx bands. This can be achieved by choosing an integer upsampling ratio (L) of 66. The DAC clock and the IF frequencies are 253.4 and 63.4 MHz, respectively. A second-order filter will be sufficient to reject the digital images and meet the spurious emission requirements.

This relaxed filter requirement is achieved at the expense of a high clock rate; the last stage of the baseband digital logic, as well as the DAC, are running in the excess of 250 MHz. The dynamic (digital) power consumption can be high. However, with the advancement of fine-geometry CMOS processes, this power consumption is being driven down very rapidly. Therefore, we believe it is a reasonable technology direction to trade off analog filter complexity with faster digital clock speed.

E. High-Order-Hold DAC

As the second part of our solution to address the reconstruction filter problem, we derive a DAC that "avoids" generating images in the first place.

A conventional DAC produces the analog waveform by converting the digital "sample" into an analog voltage and

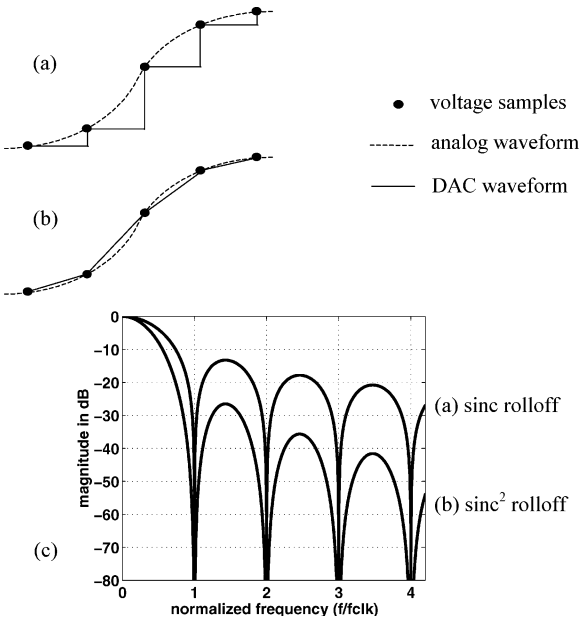

Fig. 7. Transient waveforms of (a) S/H DAC, (b) FOH DAC, and (c) their corresponding spectrum rolloffs.

"holding" it for one clock period until the next sampling instance. Such a sample-and-hold (S/H) waveform will exhibit repeating digital spectrum with the familiar $\sin(x)/x$ (sinc) rolloff, as shown in Fig. 7(a). This is also known as zero-order hold (ZOH) in the signal-processing literature.

The energy of images can be greatly reduced if the DAC output waveform is less abrupt than the staircase shown before. Instead of performing an S/H, the DAC could connect the voltage samples by straight lines such as a ramp, as shown in Fig. 7(b). It performs what is commonly known as "first-order-hold" (FOH) reconstruction. The DAC produces $(\sin(x)/x)^2$ (sinc squared) spectrum, where images roll off much faster, as shown in Fig. 7(c).

The circuit implementation of the FOH DAC is very straightforward. First, a current is generated that is proportional to the *difference* between two consecutive input digital codes (digital differentiation). Second, the current is pumped into a *capacitor* to perform the I-to-V conversion (analog integration). As such, the capacitor voltage will ramp up, effectively connecting one analog sample to the next. The implementation of a FOH DAC is, in fact, very comparable to that of a standard S/H current-steering DAC, as demonstrated in Table II.

Based on our intuitive understanding of the FOH DAC circuit implementation, we can represent its signal processing in Fig. 8(a), in which a digital differentiator $(1 - z^{-1})$ is followed by an analog integrator,[4] $(1/T) \int dt$ (where T is the clock period). Essentially, the cascade of the digital differentiator and analog integrator will turn the ZOH (square) pulse of $h_o(t)$ into

[4]The FOH DAC signal processing suffers a "singularity" at dc. Infinite attenuation of the differentiator is met by the infinite amplification of the integrator. However, this poses no problem to our application because the IF signal is bandpass in nature. We only need to avoid dc offset from saturating the integrator by performing a damped integration or a simple ac coupling.

TABLE II
COMPARSION BETWEEN THE CONVENTIONAL S/H DAC AND THE FOH DAC

	S/H DAC	**FOH DAC**
current (I) generation	Proportional to the input digital codes	Proportional to the *difference* between 2 input consecutive digital codes
Load	Resistor (R)	Capacitor (C)
Voltage output (V)	$V = I \cdot R$	$V = \frac{1}{C}\int (I)dt$
Waveform	Zero-order-hold	First-order-hold
Spectrum	$\sin(x)/x$ rolloff	$(\sin(x)/x)^2$ rolloff

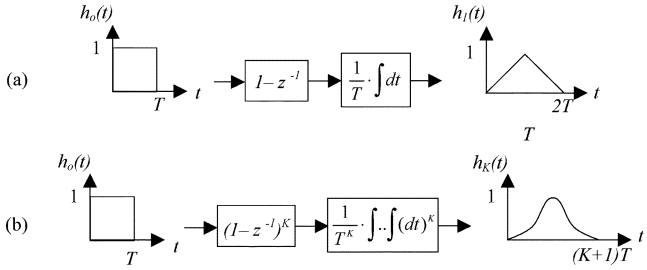

Fig. 8. Signal processing of (a) a FOH DAC and (b) a Kth-order hold DAC.

a FOH (triangular) pulse of $h_1(t)$. The Laplace transform of a square pulse $h_o(t)$ [19] is given by

$$H_o(\omega) = T \cdot \left[\frac{\sin\left(\frac{\omega T}{2}\right)}{\frac{\omega T}{2}}\right] \cdot e^{-j(\omega T/2)}. \tag{8}$$

Referring to Fig. 8(a), the Laplace transform of the triangular pulse $h_1(t)$ can be written as

$$\begin{aligned} H_1(\omega) &= \left(1 - e^{-j\omega T}\right) \cdot \frac{1}{j\omega T} \cdot H_o(\omega) \\ &= T \cdot \left[\frac{\sin\left(\frac{\omega T}{2}\right)}{\frac{\omega T}{2}}\right]^2 \cdot e^{-j\omega T}. \end{aligned} \tag{9}$$

As shown in (9), the final FOH DAC waveform will exhibit a spectrum with $(\sin(x)/x)^2$ rolloff.

The previous ZOH-to-FOH transformation can be generalized to realize any high-order-hold DAC. If we cascade K digital differentiators with K analog integrators, as shown in Fig. 8(b), we can turn a ZOH pulse into a Kth-order-hold pulse, i.e.,

$$\begin{aligned} H_K(\omega) &= \left(1 - e^{-j\omega T}\right)^K \cdot \frac{1}{T^K} \cdot \frac{1}{(j\omega)^K} \cdot H_o(\omega) \\ &= T \cdot \left[\frac{\sin\left(\frac{\omega T}{2}\right)}{\frac{\omega T}{2}}\right]^{K+1} \cdot e^{-j(K+1)\omega T/2}. \end{aligned} \tag{10}$$

Therefore, the Kth-order-hold DAC will exhibit $(\sin(x)/x)^{K+1}$ rolloff. To the extreme, when K is high, the digital images will be so small in the DAC output spectrum and the DAC time-domain waveform will resemble the "true" (very smooth) analog signal very well.

Fig. 9 illustrates how the output waveforms look for the ZOH, the FOH, and the second-order-hold (SOH, $K = 2$) DACs.

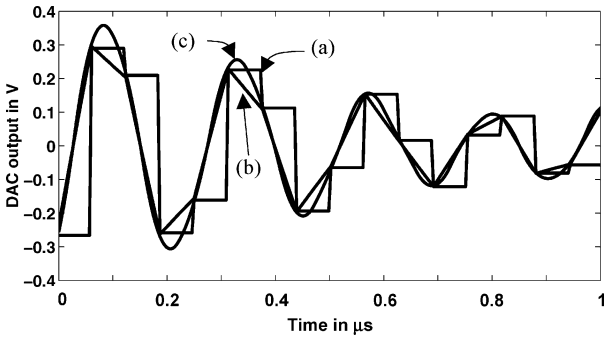

Fig. 9. Output waveforms of the (a) ZOH, (b) FOH, and (c) SOH DAC.

Notice that the three DACs produce the same voltages at the sampling instances (after proper time alignment, as they have different phase shifts). It is obvious that the higher the order, the smoother the DAC waveform. As will be illustrated shortly, a SOH DAC will be implemented in the digital-IF transmitter architecture to provide good spurious emission characteristics with a minimum hardware requirement.

Like any high-speed DAC designed for communication applications [20], the SOH DAC of this work should be designed for good dynamic performances. Interested readers are encouraged to consult [21] for the detailed circuit implementation and performances in the SiGe BiCMOS technology.

Also developed to yield a single-chip integration of wireless transmitters, an interpolation DAC has been recently reported in [22]. Employing skewed clocks generated by a voltage-control delay line, the DAC successfully realizes a linear interpolation (FOH) function. It handles wide-band baseband signal.[5] However, the DAC structure appears to be quite involved and it is not immediately obvious how the scheme can be extended to realize higher-order-hold responses.

F. Pulse Shaping and Interpolation Filters

As discussed in Section III-D, an optimal interpolation ratio (L) of 66 will be implemented to substantially alleviate the task of reconstruction filtering. This sample-rate conversion will be undertaken by three stages of integer-ratio upsamplers, namely: 1) a 2 × root-raised cosine (RRC) pulse-shaping filter; 2) a 3 × interpolator with comb filtering; and, finally, 3) a 11 × interpolator with comb filtering.

The W-CDMA standard specifies a RRC filter of 0.22 rolloff factor in the transmitter [13]. It shapes each pulse in the data sequence such that the overall response of the communication system (which includes another RRC filter at the receiver) at any given sampling instant is zero, except for the current symbol. This fulfills the Nyquist criterion, in which there would be no intersymbol interference [23]. An upsampling ratio of 2 is assumed, raising the chip rate of 3.84 MHz to the sample rate of 7.68 MHz. For practical purposes, a finite-time response is assumed for the RRC filter. By building the RRC filter using a 17-tap finite-impulse response (FIR) structure, it comfortably satisfies the spectrum-emission mask requirement, as will be demonstrated shortly. Simulation reveals that better than 40 dB (less than 1%) of EVM is achieved. This leaves ample safety margin for other circuit impairments to meet the overall EVM target of 17.5%.

[5]Notice that, in comparison, the high-order-hold DAC presented in our work could not handle baseband data. This is because the digital differentiators would annihilate any signal around dc. However, this is not a concern for the digital-IF application, because the DAC input signal is centered around IF. There is no signal component at dc.

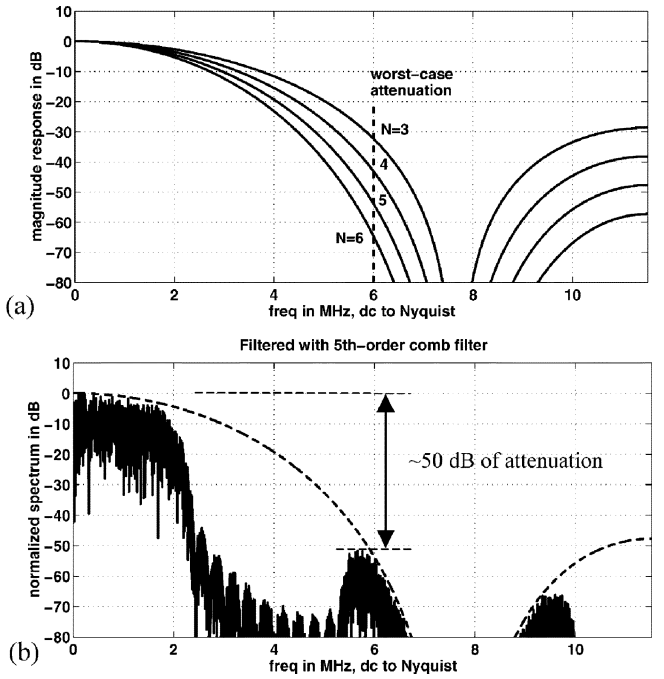

Fig. 10. (a) Magnitude responses of the comb filter of order 3–6 and (b) the filtered 3 × upsampled spectrum ($f_{\rm clk} = 23.04$ MHz).

The interpolation filter to be designed following the RRC filter will have the biggest impact on the adjacent-channel leakage power ratio (ACLR) performance. The standard calls for a minimum of 33 and 43 dB of ACLR at 5- and 10-MHz offset frequency from the carrier [13]. To achieve good rejection properties with the simplest hardware possible, the lower ratio (3 ×) upsampler, instead of the higher ratio (11 ×) one, will be implemented first. The data rate will be increased to 23.04 MHz, which still is a relatively low frequency, where digital operations can be accomplished with low power consumption and circuit complexity.

The 3 × upsampler inserts two zero-valued samples between two consecutive original samples, creating a copy of the original signal spectrum at 7.68 MHz (one-third of the final clock rate of 23.04 MHz). This replica needs to be sufficiently attenuated by a linear low-pass filter for meeting the ACLR requirements, which will be accomplished by a comb filter. The filter transfer function, in its general form, is given by

$$H(z) = \left(\frac{1 - z^{-L}}{1 - z^{-1}}\right)^N \tag{11}$$

where N and L are the filter order and upsampling ratio, respectively. The frequency response is found by substituting $z = e^{j\omega T}$. This filter is particularly efficient in rejecting the spectrum replica because of its zeroes locations

$$f_{\rm zero} = \frac{n}{L} \cdot f_{\rm clk}, \quad \text{where} \quad n = 1, 2, \ldots, L-1. \tag{12}$$

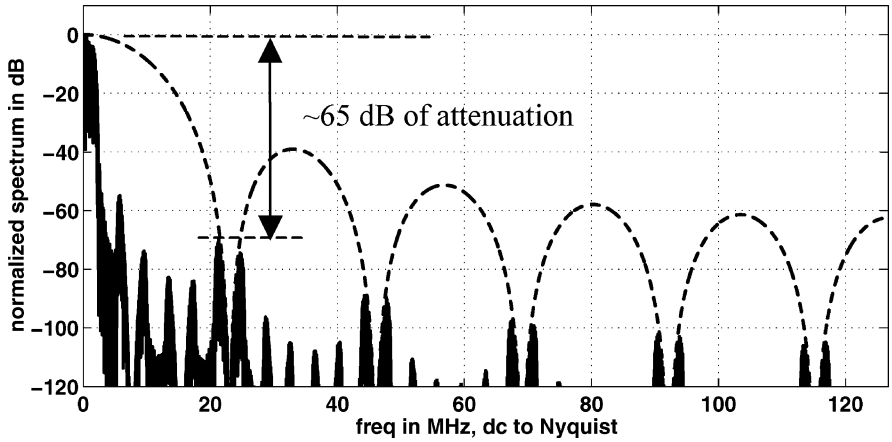

Fig. 11. Spectrum of the 11 × upsampled signal after the third-order comb filter ($f_{\text{clk}} = 253.44$ MHz).

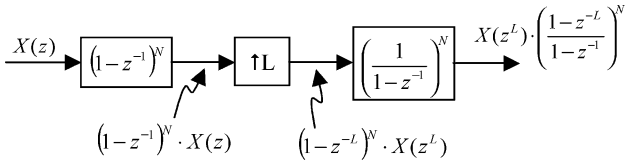

Fig. 12. Efficient implementation of a Nth-order comb low-pass filter for an L-times interpolation.

These zeroes appear exactly at frequencies where the spectrum repeats itself.

The transfer functions ($L = 3$, with $N = 3$–6) of the low-pass comb filter following the 3 × upsampling are shown in Fig. 10(a). Worst-case attenuation is located at about 6 MHz, which is found by subtracting the signal bandwidth ($(1 - 22\%) \cdot (f_{\text{chip}}/2) = 1.5$ MHz) from the replica frequency (7.68 MHz). We are to design a better than 15-dB margin to the minimum ACLR requirement mentioned before. The fifth-order filter function is chosen, which provides close to 50 dB of worst case attenuation. The filtered spectrum is shown in Fig. 10(b).

Following a similar analysis, the order of the comb filter following the 11 × interpolation is chosen to be three. This gives a worst case attenuation of about 65 dB. Fig. 11 displays the 11 × upsampled signal spectrum after the comb filter. The lower filter order is particularly advantageous from a power perspective, because the comb filter has to operate at the peak speed (i.e., 253.44 MHz) of the digital IF system.

The two comb filters (where $L = 3$ and 11 for the 3 × and 11 × interpolations, respectively) can be efficiently implemented as shown in Fig. 12. The differentiators ($1 - z^{-1}$) are implemented prior to the upsampler, which is then followed by the integrators ($1/(1 - z^{-1})$). The differentiator circuits can take advantage of the lower clock speed and consume less power.

The upsampled I and the Q baseband data at 253.44 MHz will be multiplied with running ±1s to perform the IF upconversion. (As discussed in Section III-B, this is equivalent to a sign-bit-flipping operation.) After the I and Q data summation, the digital IF signal is achieved. Fig. 13(a) displays the digital IF spectrum, while Fig. 13(b) overlaps it with the spectrum emission mask[6] requirement in dBc over the respective measurement bandwidth [13]. Adequate design margin is included to account for the distortions introduced by the subsequent analog/RF portion of the TxIC and the power amplifier.

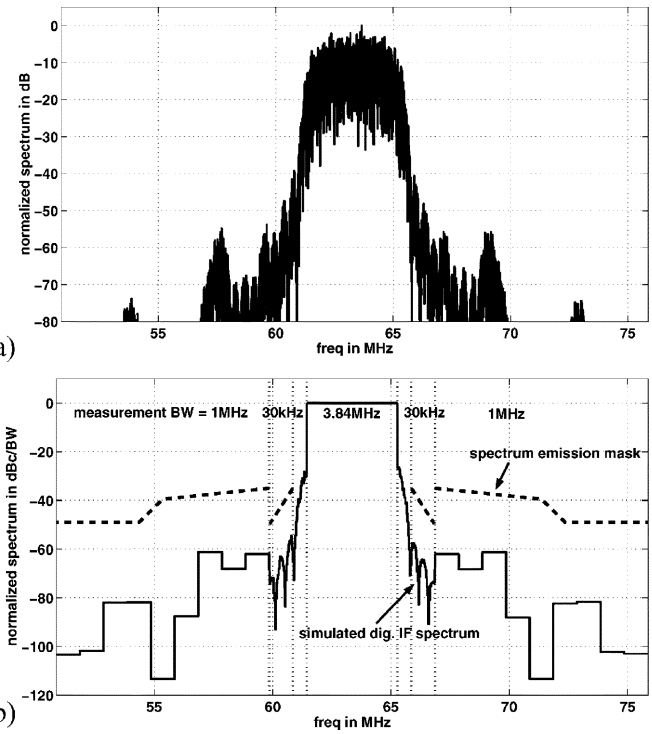

Fig. 13. (a) Spectrum of the digital-IF signal and (b) the corresponding spectrum expressed in dBc over the respective measurement bandwidth.

Finally, we will investigate the resolution requirement for the digital system. The signal-to-noise ratio (SNR) of an N-bit quantization is generally given by [24]

$$\text{SNR} = 6.02 \cdot N + 10 \cdot \log_{10}(3) - 10 \cdot \log_{10}(\text{PAR}) + 10 \cdot \log_{10}(\text{OSR}) \quad (13)$$

[6]The spectrum emission mask [13] applies to frequencies between 2.5–12.5 MHz away from the center carrier frequency (which translates to the IF of 63.36 MHz in the example of Fig. 13. The power of emission is measured in 30-kHz bandwidth if it is between 2.5–3.5 MHz offset frequency and 1 MHz in the 3.5–12.5-MHz region. The out-of-channel emission is specified relative to the channel power measured in a 3.84 MHz bandwidth.

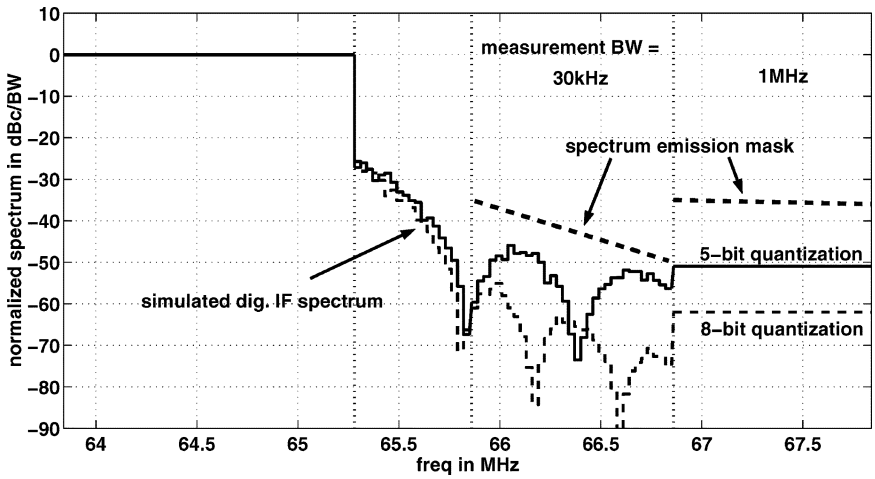

Fig. 14. Spectrum of the digital-IF signal in dBc over measurement bandwidth with 5 or 8 bit of resolution.

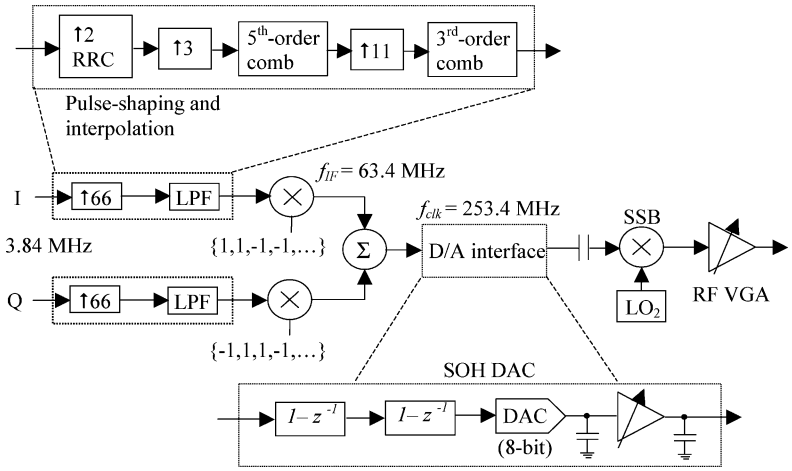

Fig. 15. Proposed transmitter architecture featuring a SOH DAC.

where PAR and OSR are the peak-to-average ratio and the oversampling ratio, respectively. W-CDMA signals can exhibit PAR as high as 4.5 (6.5 dB), while the OSR, which is given by the ratio of the Nyquist frequency (126.7 MHz) to the signal bandwidth (5 MHz) is approximately 25 in our system. To meet an EVM (i.e., SNR) of -40 dB, a mere 5-bit resolution would be sufficient according to (13).

On the other hand, the spectrum emission mask requirement poses a more limiting condition to determine the system resolution. Fig. 14 shows the spectrum resulting from 5-bit quantization. It is dangerously close to the spectrum mask around the 2.5–3.5-MHz offset frequencies (that is, from 65.86 to 66.86 MHz). The ACLR at the 5-MHz adjacent channel is only 37 dB, which is only 4 dB above the absolute minimum requirement. This imposes unrealistically high linearity requirement on the subsequent TxIC analog/RF components and the power amplifier. On the other hand, when 8 bits of resolution is used, as is the case shown in Figs. 13(b) and 14 (the broken line), the specification can be met with good margin. The ACLR at 5 MHz goes up to the more comfortable level of 48 dB or 15 dB above the requirement.

G. Summary of the Transmitter Architecture

Fig. 15 shows the block diagram of the final transmitter architecture with all the design parameters as described earlier. The SOH DAC is selected to provide a $(\sin(x)/x)^3$ spectrum for high image rolloff.[7] It is composed of two digital differentiators and two continuous-time integrators in cascade. The first continuous-time integrator is built as a FOH DAC, while the second is naturally incorporated into the IF VGA outputs. No dedicated reconstruction filter circuit, or precision automatic tuning, is needed. This scheme can be understood as performing digital pre-emphasis on the baseband signals to trivialize the task of analog filtering. Again, this follows the same technology direction discussed earlier. That is, to tradeoff analog complexities by implementing more functions in the digital domain.

[7]An inverse $(\sin(x)/x)^3$ digital filter (not shown in Fig. 15) is needed to compensate for the inchannel distortion of the baseband signals; otherwise, degraded EVM will result. While more complicated than a conventional inverse $(\sin(x)/x)$ filter, it is still straightforward to implement because the channel bandwidth (5 MHz) is narrow as compared to the clock rate (253.4 MHz).

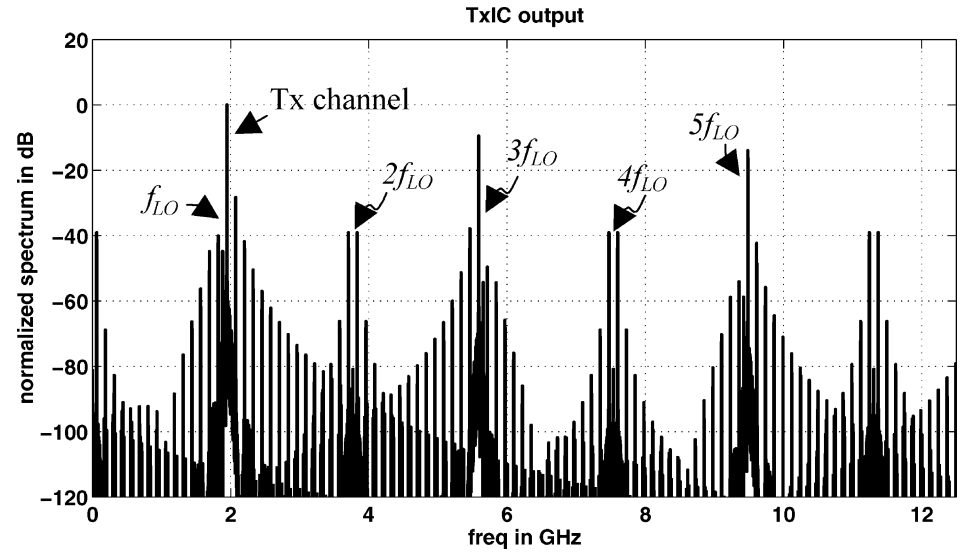

Fig. 16. Output spectrum of the TxIC from dc to 12.5 GHz.

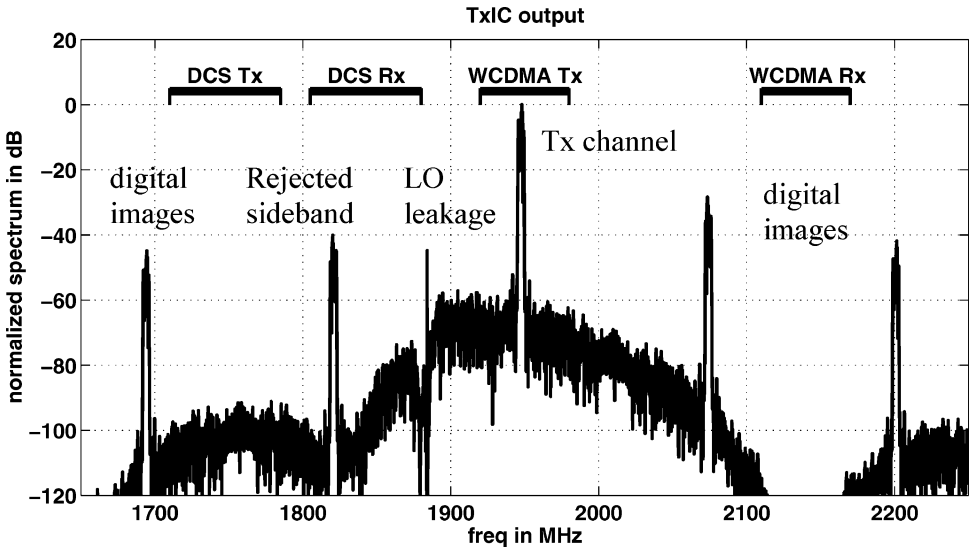

Fig. 17. Simulated output spectrum of the TxIC in the DCS and W-CDMA bands.

IV. Spurious Emissions Simulations

To establish the feasibility of our architecture illustrated in Fig. 15 (which does not require a sophisticated on-chip reconstruction filter or an external IF SAW filter), we present the system-level simulation results. In particular, we will observe if the transmitter satisfies the spurious emission requirement. Spurs are generated by harmonic emissions or frequency conversion products. They must be small enough so as not to degrade the sensitivity of the receiver or jam the nearby receivers operating at a different standard [8].

Fig. 16 shows the simulated wideband (dc to 12.5 GHz) output spectrum of the entire transmitter, which includes the digital IF upconversion, SOH D/A conversion, and the RF SSB upconversion. The IF spectrum [of Fig. 13(a)] is D/A converted and mixed with LO_2 (f_{LO}), which is a square pulse rich in odd-order harmonics ($3f_{\mathrm{LO}}, 5f_{\mathrm{LO}}$, etc). Here, we further assume a 1% mismatch between the rise and fall times of the LO signal so that even-order harmonics (at $2f_{\mathrm{LO}}, 4f_{\mathrm{LO}}$, etc.) are also present. This presents a pessimistic scenario from the spurious emission perspective. Since we have deliberately removed the reconstruction filter that conventionally follows the D/A conversion, the unfiltered digital images can now get downconverted with the LO harmonics. They will show up at frequencies

$$f_{\mathrm{spur}} = m \cdot f_{\mathrm{LO}} - (n \cdot f_{\mathrm{clk}} \pm f_{\mathrm{IF}}) \tag{14}$$

where m and n are integers indicating the number of the LO harmonics and the digital image locations, respectively. These spurs can potentially corrupt the transmit spectrum and nearby bands of interest. We will demonstrate that the hardware-efficient SOH DAC circuit, by providing a high-order $(\sin(x)/x)^3$ rolloff, would be sufficient to meet the spur requirements.

Fig. 17 presents a close-up of the TxIC output spectrum around the DCS and W-CDMA bands. A very clean transmit spectrum is observed. The noise floor in the W-CDMA Tx band is mainly dominated by the DAC quantization noise (at the 8-bit

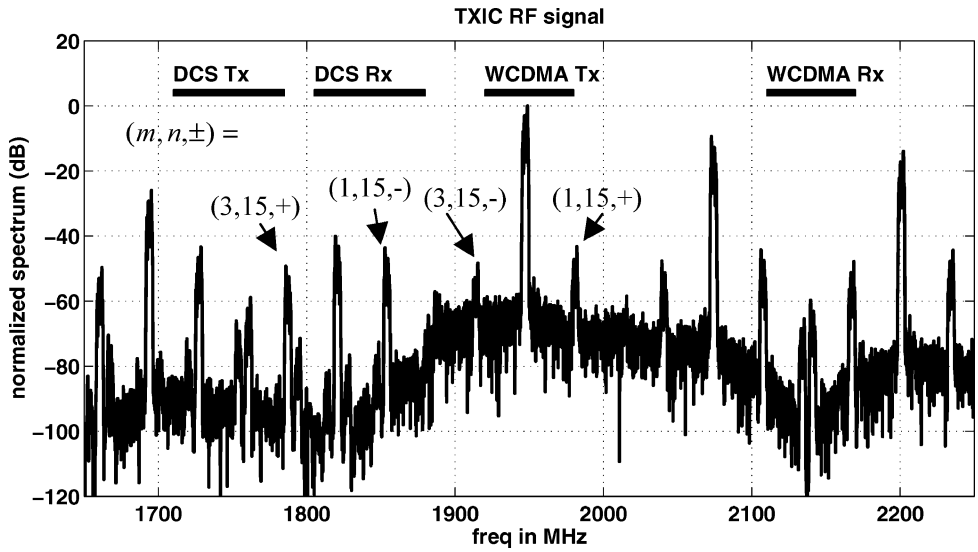

Fig. 18. Simulated output spectrum of the TxIC when the SOH DAC is replaced by a conventional ZOH DAC.

TABLE III
SPURIOUS EMISSION REQUIREMENTS FOR W-CDMA HANDSETS

	Frequency Bandwidth	Measurement Bandwidth	Minimum Requirement	Re-calculated* in dBc/5MHz
General spurious emissions [13]	9 - 150 kHz	1 kHz	-36 dBm	---
	0.15 - 30 MHz	10 kHz	-36 dBm	---
	30 - 1000 MHz	100 kHz	-36 dBm	-43
	1 - 12.75 GHz	1 MHz	-30 dBm	-47
Additional Spurious emissions [13]	1893.5 - 1919.6 MHz	300 kHz	-41 dBm	-53
	925 - 935 MHz	100 kHz	-67 dBm	-74
	935 - 960 MHz	100 kHz	-79 dBm	-86
	1805 - 1880 MHz	100 kHz	-71 dBm	-78
Others [8]	1920 - 1980 MHz	1 MHz	-25 dBm	-42
	2110 - 2170 MHz	3.84 MHz	-120 dBm	-143
	1710 - 1785 MHz	100 kHz	-49 dBm	-56

* assuming maximum (worst-case) transmitter output power of 24 dBm/5 MHz

level). Due to our choice of clock frequency, no digital images will land in the W-CDMA Rx band. Notice that the quantization noise of the DAC in the W-CDMA Rx band is heavily attenuated due to the notch of the $(\sin(x)/x)^3$ rolloff, which is rather advantageous. This model also assumes imperfect lower sideband rejection and LO leakage; they show up around the DCS receive (Rx) bands and will be further attenuated by the RF SAW and the duplexer filters before they get to the antenna.

The effectiveness of the SOH DAC becomes obvious if Fig. 17 is contrasted with a corresponding plot when a conventional (ZOH) DAC is employed (Fig. 18). The TxIC output spectrum becomes much more problematic. Numerous spurs show up at the sensitive Tx and Rx bands. This is because the digital images fail to roll off as rapidly as when the SOH DAC is used. Some of the spurs have been identified by their respective $(m, n, \pm)$ parameters [referring to (14)] to illustrate how they were generated.

The W-CDMA standard defines general and additional spurious emission requirements in terms of the output power (dBm) over certain measurement bandwidth; they are listed in Table III. For ease of graphical presentation, we will recalculate these powers over the 5-MHz W-CDMA channel bandwidth. Assuming the maximum (worst case) transmitter output power equals 24 dBm, we can represent the spurious emission specifications in the unit of dBc/5 MHz. Notice that other constraints are also adopted from [8].

Before the TxIC output signal shows up at the antenna, it will encounter two additional external filters, which are indispensable in the handset transmitter. They are, namely, the RF bandpass SAW filter and the duplexer filter. These two external filters will advantageously provide additional spurs removal. Based on data sheets available in the public domain, we can assume a combined filter attenuation profile, as shown in Fig. 19. We have intentionally underestimated the level of attenuation that

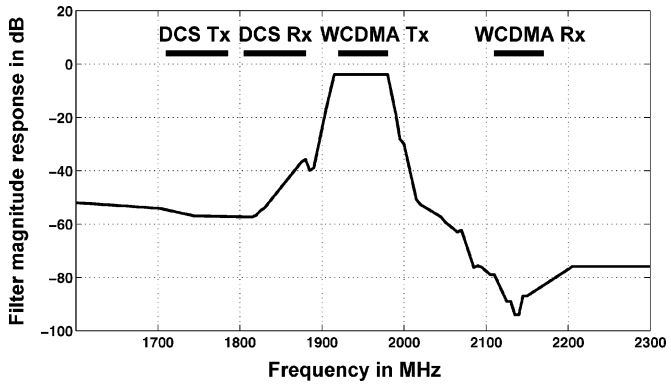

Fig. 19. Combined magnitude responses of the RF bandpass SAW filter and the duplexer filter.

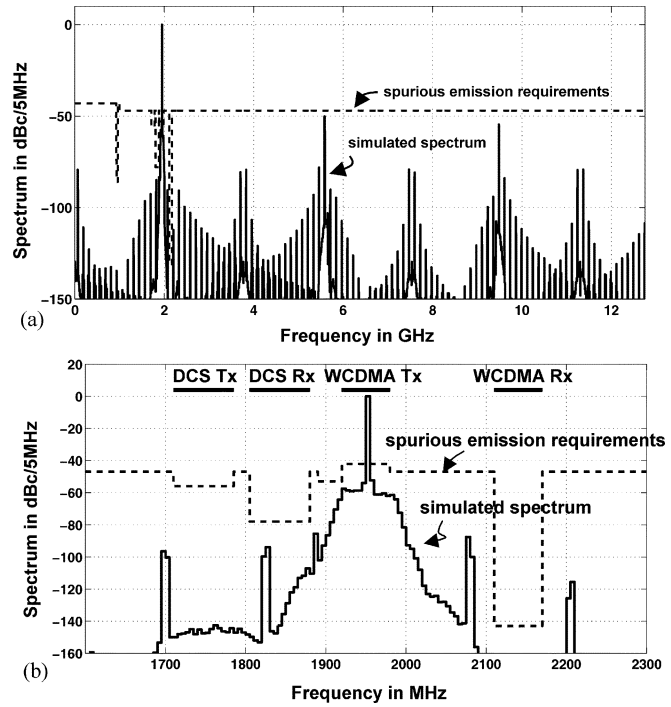

Fig. 20. Transmit signal spectrum at the antenna, expressed in dBc/5 MHz, (a) from DC to 12.5 GHz and (b) near the DCS/W-CDMA bands. Maximum (worst case) TxIC output power of 24 dBm is assumed.

they can provide, so that the spurious emission results to be illustrated next will represent the pessimistic scenario.

Displaying the TxIC spectrum of Fig. 17 in terms of dBc/5 MHz and taking the external filter attenuation into account, the final Tx spectrum at the antenna is computed. Fig. 20(a) shows the wide-band (dc to 12.5 GHz) spurious emission results, while Fig. 20(b) focuses on the DCS and W-CDMA bands. Spurious emission requirements are met. It was shown that, with the help of an effective frequency plan and an innovative SOH D/A conversion scheme, a functional W-CDMA transmitter can be built with virtually no dedicated IF (or reconstruction) filtering.

V. Conclusion

This research intends to accelerate and enhance the power and performance advantages as we move the digital/analog boundary closer to the antenna in the wireless handset transmitter architecture. A simple digital quadrature upconversion is proposed for perfect I/Q matching and EVM performance. The task of reconstruction filtering is greatly alleviated by: 1) careful frequency planning and 2) using a high-order-hold DAC circuit. Simulation reveals that the resulting transmitter could meet the W-CDMA spurious emission requirements with virtually no dedicated reconstruction filtering. This architecture is designed to benefit fully from the rapid advances of digital IC technology and is anticipated to be a good candidate for implementation of very low-power highly integrated transmitter IC for W-CDMA handset applications.

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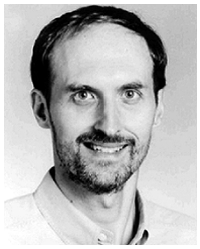
Vincent W. Leung (M'97) received the B.Eng. and M.Eng. degrees from McGill University, Montreal, QC, Canada, in 1995 and 1998, respectively, and the Ph.D. degree from the University of California at San Diego, La Jolla, in 2004, all in electrical engineering.

From 1997 to 2000, he was with Analog Devices, Somerset, NJ, where he engaged in the design of xDSL analog IC chips. He joined IBM T. J. Watson Research Center, Yorktown Heights, NY, in 2004. He is the coauthor of one book (on log-domain filters) and holds one U.S. patent.

Dr. Leung's doctoral research was awarded the Second Prize in Semiconductor Research Corporation's (SRC's) SiGe Design Contest.



Lawrence E. Larson (M'82–SM'90–F'00) received the B.S. degree in electrical engineering and the M.Eng. degree from Cornell University, Ithaca, NY, in 1979 and 1980, respectively, and received the Ph.D. degree in electrical engineering from the University of California, Los Angeles, in 1986.

He was with Hughes Research Laboratories, Malibu, CA, from 1980 to 1996, where he directed the development of high-frequency microelectronics in GaAs, InP and Si/SiGe, and MEMS technologies. He joined the Faculty at the University of California at San Diego (UCSD), La Jolla, in 1996, where he is the inaugural holder of the Communications Industry Chair. He currently is Director of the UCSD Center for Wireless Communications. During the 2000–2001 academic year, he was on leave with IBM Research, San Diego, CA, where he directed the development of RFICs for third-generation applications. He has published over 200 papers, coauthored three books, and received 27 U.S. patents.

Dr. Larson was the recipient of the 1995 Hughes Electronices Sector Patent Award for his work on RF MEMs and a co-recipient of the 1996 Lawrence A. Hyland Patent Award of Hughes Electronics for his work on low-noise millimeterwave HEMTs and of the 1999 IBM Microelectronics Excellence Award for his work in Si/SiGe HBT technology.

Prasad S. Gudem received the Ph.D. degree in electrical and computer engineering from the University of Waterloo, Waterloo, ON, Canada, in 1996, where his doctoral research concerned the modeling and numerical simulation of amorphous silicon devices.

After a brief time with Mitel Semiconductors, Kanata, ON, Canada, he joined Cadence Design Systems, San Diego, where he was involved with semiconductor-device modeling for analog and radio-frequency (RF) applications. In 2000, he joined the Watson Research Center, IBM, San Diego, CA, where he was involved with RF integrated circuit design for W-CDMA applications using IBM's SiGe technology. He recently joined Qualcomm, San Diego, CA, where he leads the development of zero intermediate-frequency diversity receiver chips. He also coadvises several graduate students in their Ph.D. research in the Electrical and Computer Engineering Department, University of California, San Diego (UCSD), La Jolla.

Dr. Gudem received the Graduate Teaching Award for the 2001–2002 academic year in recognition of his outstanding teaching of the popular ECE265 course sequence (Communication Circuit Design: I, II, and III).