Modified Derivative Superposition Method for Linearizing FET Low Noise Amplifiers

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Abstract — **The degrading effect of the circuit reactances on the maximum IIP_3 in the conventional derivative superposition (DS) method is explained using the Volterra series analysis. The effect of the subthreshold biasing of one of the FETs in the DS method on NF is also explained. A modified DS method is proposed to increase the maximum IIP_3 at RF. It was used in a 0.25μm Si CMOS LNA designed for cellular CDMA receivers. The LNA achieved +17.2dBm IIP_3 with 15.5dB gain, 1.6dB NF and 9mA@2.6V power consumption.**

Index Terms — **Amplifier noise, intermodulation distortion, MOSFET amplifiers, nonlinearities, Volterra series.**

I. Introduction

The single-tone desensitization requirement for CDMA phones demands a very high LNA IIP_3 in combination with low NF, high gain and low current consumption. This design challenge requires the use of linearization techniques. In [1], feed-forward distortion cancellation was used to achieve a very high IIP_3 of a CMOS LNA. This technique has not been widely adopted because of its high sensitivity to mismatches between the main and auxiliary gain stages and errors in the input signal scaling. A FET can also be linearized by biasing at a gate-source voltage (V_{GS}) at which the 3rd-order derivative of its dc transfer characteristic is zero [2]. The resulting IIP_3 peaks in a very narrow range of V_{GS} making this technique very sensitive to bias variations. To reduce the IIP_3 sensitivity to the bias, the derivative superposition (DS) method was proposed in [3]. It uses two or more parallel FETs of different widths and gate biases to achieve a composite dc transfer characteristic with an extended V_{GS} range in which the 3rd-order derivative is close to zero. However, the IIP_3 improvement in this method is only modest at RF (3dB as reported in [4]). Reducing the source degeneration inductance and the drain load impedance at the 2nd-harmonic frequency of the composite input transistor allowed the authors of [5] to boost IIP_3 in the DS method by as much as 10dB. The main disadvantage of the DS method in general is that it results in a higher NF (by 0.6dB as reported in [5]). This NF increase is not predicted by simulations using BSIM3v3 models.

Here we explain the poor IIP_3 performance of the conventional DS method at RF based on the Volterra series analysis. We also explain the higher NF resulting from the use of this method. We propose a modified DS method to achieve a very high IIP_3 at RF. A cellular CDMA 0.25μm CMOS LNA using this method is described. The measured data is presented to confirm the analytical results.

II. DC Theory of DS Method

Consider a common-source FET biased in saturation. Its small-signal output current can be expanded into the following power series in terms of the small-signal gate-source voltage v_{gs} around the bias point

$$i_d(v_{gs}) = g_1 v_{gs} + g_2 v_{gs}^2 + g_3 v_{gs}^3 + \cdots \quad (1)$$

where g_1 is the small-signal transconductance and the higher-order coefficients (g_2, g_3 etc.) define the strengths of the corresponding nonlinearities. Among these coefficients, g_3 is particularly important because it controls the 3rd-order intermodulation distortion (IMD_3) at low signal levels and, thus, determines IIP_3, which is given by

$$A_{IP3} = \sqrt{\frac{4}{3}\left|\frac{g_1}{g_3}\right|}. \quad (2)$$

The power series coefficients generally depend on the dc gate-source and drain-source voltages, V_{GS} and V_{DS}. However, the dependence on V_{DS} for a FET in saturation can be neglected. Then the coefficients of (1) can be found as

$$g_1 = \frac{\partial I_D}{\partial V_{GS}}, \quad g_2 = \frac{1}{2}\frac{\partial^2 I_D}{\partial V_{GS}^2}, \quad g_3 = \frac{1}{6}\frac{\partial^3 I_D}{\partial V_{GS}^3}. \quad (3)$$

The dependence of g_3 on V_{GS} is such that g_3 changes from positive to negative when V_{GS} transitions from the weak and moderate inversion regions to the strong inversion (SI) region [2]. If a positive g_3 with a certain $g_3(V_{GS})$ curvature of one FET is aligned with a negative g_3 with a similar but mirror-image curvature of another FET by offsetting their gate biases and the g_3 magnitudes are equalized through a relative FET scaling, the resulting composite g_3

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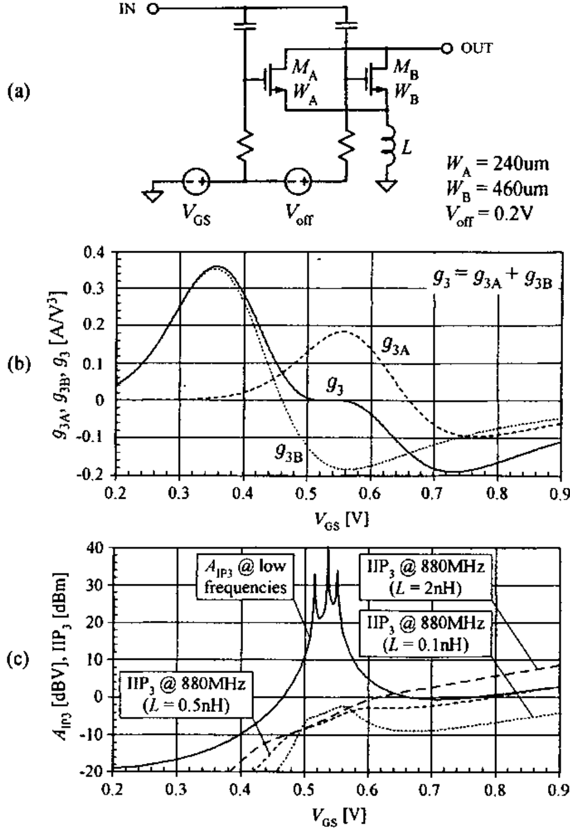

Fig. 1. Derivative superposition method. (a) Composite FET. (b) 3rd-order power series coefficients. (c) Theoretical A_{IP3} at dc and $\mathrm{IIP_3}$ at 880MHz.

will be close to zero and the theoretical A_{IP3} will be significantly improved in a wide range of the gate biases as shown in Fig. 1. This is only valid for very low frequencies at which the effect of circuit reactances is negligible.

III. RF Theory of DS Method

Consider a small-signal nonlinear equivalent circuit shown in Fig. 2 for a composite FET (M_A+M_B) in Fig. 1(a). Z_1 is the transformed output impedance of the signal generator and L is the source degeneration inductance. Here we made the following assumptions

1. The body effect is negligible i.e. $g_{\mathrm{mb}} \approx 0$.
2. All capacitances are zero except for C_{gs}.
3. C_{gs} is bias independent i.e. linear. This assumption is only valid in the weak and strong inversion regions.
4. The FET gate and source series resistances and the dc resistance of the degeneration inductor are zero.
5. The FET output conductance is infinite i.e. there is no channel length modulation.

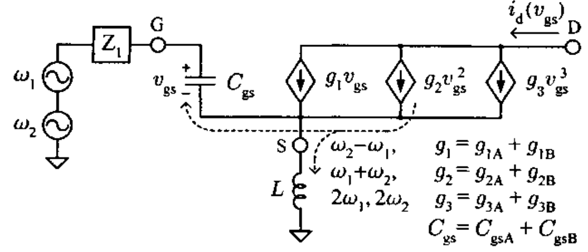

Fig. 2. Small-signal nonlinear equivalent circuit of a composite FET in Fig. 1(a).

6. The input signal is very weak such that the $i_{\mathrm{d}}(v_{\mathrm{gs}})$ nonlinearities of the order higher than three are negligible. This assumption is typical for LNAs because they operate far below their 1dB compression point.

In this *weakly nonlinear* case with the neglected C_{gd}, $\mathrm{IMD_3}$ would be generated entirely by the $g_3 v_{\mathrm{gs}}^3$ component of the drain current if L was zero. The source degeneration inductance creates a feedback path for the drain current to v_{gs}. This feedback is particularly strong for high frequency spectral components of i_{d}. For example, the 2nd harmonics generated by $g_2 v_{\mathrm{gs}}^2$ are fed back across the gate and source adding to the fundamental components of v_{gs}. These spectral components are then mixed in $g_2 v_{\mathrm{gs}}^2$ to produce the responses at $2\omega_1 \pm \omega_2$ and $2\omega_2 \pm \omega_1$. Thus, the 2nd-order nonlinearity of i_{d} also contributes to $\mathrm{IMD_3}$.

Assuming that $\Delta\omega$ $(= \omega_2 - \omega_1)$ is much smaller than ω_1 and ω_2 such that $j\Delta\omega L \approx 0$ and the signal generator is conjugately matched to the FET input at ω $(\omega \approx \omega_1 \approx \omega_2)$, we can derive the following expression for $\mathrm{IIP_3}$:

$$\mathrm{IIP_3} = 4g_1^2\omega^2 L C_{\mathrm{gs}}/(3|\varepsilon|) \tag{4}$$

where

$$\varepsilon = g_3 - \frac{2g_2^2/3}{g_1 + \dfrac{1}{j2\omega L} + j2\omega C_{\mathrm{gs}} + Z_1(2\omega)\dfrac{C_{\mathrm{gs}}}{L}}. \tag{5}$$

As can be seen from (4) and (5), making g_3 zero does not result in an infinite $\mathrm{IIP_3}$ as it does at low frequencies due to the second term in (5). This term represents the contribution of the 2nd-order nonlinearity to $\mathrm{IMD_3}$. As expected, this contribution depends on the degeneration inductance L. Fig. 1(c) shows $\mathrm{IIP_3}$ calculated at 880MHz using (4) and (5) for the composite FET in Fig. 1(a) with an input matching circuit consisting of a series capacitor and shunt inductor. As can be seen, the source degeneration inductance significantly suppresses the high-frequency $\mathrm{IIP_3}$ peaking at V_{GS} where g_3 is close to zero. In fact, for realistic values of L, which are limited by the downbond inductance ($\geq$ 0.5nH), the conventional DS method provides no $\mathrm{IIP_3}$ improvement at all.

According to (5), to minimize the 2nd-order contribution to IMD_3 in the presence of a nonzero L, $Z_1(2\omega)$ must be increased. However, then the feedback through the neglected C_{gd} becomes significant, which also leads to the 2nd-order contribution to IMD_3. To completely eliminate this contribution and achieve a significant IIP_3 improvement in the DS method, the gate and drain terminations of the composite FET at the 2nd-harmonic frequency must be optimized. Our analysis shows that one of these terminations must have a negative real part, which would result in potential instability of the amplifier. The authors of [5] achieved a noticeable IIP_3 improvement using the conventional DS method by simply minimizing the source degeneration inductance and the drain load impedance. However, with a very small L, it is difficult to simultaneously achieve a good VSWR and NF. This is probably why the gain and NF of the LNA in [5] are only 10dB and 2.85dB respectively at 900MHz.

IV. Effect of DS Method on NF

The DS method in general uses two FETs one of which is biased in the weak inversion (WI) region and the other in SI. Intuitively, the overall NF of the composite FET should be dominated by the FET in SI since it draws approximately 20 times more current than the FET in WI. This assumption is confirmed by simulations using BSIM3v3 models. However, it disagrees with our measured data.

The most significant MOSFET noise sources at RF are the drain current noise and the induced gate noise given by

$$\overline{i_{\rm nd}^2} = 4kT\Delta f\gamma g_{\rm d0}, \qquad (6)$$

$$\overline{i_{\rm ng}^2} = 4kT\Delta f\delta\frac{\omega^2 C_{\rm gs}^2}{5g_{\rm d0}}, \qquad (7)$$

where γ and δ are the bias-dependent noise coefficients and $g_{\rm d0}$ is the drain-source conductance at zero $V_{\rm DS}$. For a long-channel FET in SI, $g_{\rm d0} = 2I_{\rm D,sat}/(V_{\rm GS} - V_{\rm TH})$ where $I_{\rm D,sat}$ is the drain saturation current and $V_{\rm TH}$ is the threshold voltage. The two noise currents are partially correlated, with a correlation coefficient defined as

$$c = \overline{i_{\rm ng} \cdot i_{\rm nd}^*} / \sqrt{\overline{i_{\rm ng}^2} \cdot \overline{i_{\rm nd}^2}}. \qquad (8)$$

The values of γ, δ, and c have been derived by van der Ziel [6] for a long channel device in SI. For a saturated FET, they are 2/3, 4/3, and $j0.395$ respectively. The short-channel values of γ and δ are 2-3 times larger. For simplicity, the short-channel effects will be neglected here. Extending the van der Ziel model for a FET in WI, we derived the long-channel values of γ, δ, and c to be 1/2, 5/4, and $j0.707$ respectively. Since the drain current in WI is due to diffusion, $g_{\rm d0}$ is just $I_{\rm D,sat}/\phi_t$ where ϕ_t is the thermal voltage kT/q. Substituting this $g_{\rm d0}$ into (7), we can make an interesting observation. While the FET in WI draws a negligible drain current, its induced gate noise is inversely proportional to the drain current and, thus, can be quite significant. It adds to the induced gate noise current of the FET in SI degrading the overall NF in the DS method.

Fig. 3. Simplified schematic diagram of CMOS LNA using modified DS method.

V. Modified DS Method and LNA Design

For the DS method to significantly boost IIP_3 at RF, it is not necessary to completely eliminate the 2nd-order contribution to IMD_3. It is enough to make it the same magnitude and opposite phase with the 3rd-order contribution. Instead of optimally scaling and rotating the 2nd-order contribution by tuning the 2nd-harmonic terminations of the composite FET, here we propose a method shown in Fig. 3, which is similar to the conventional DS method but uses a tapped inductor for source degeneration to adjust the magnitude and phase of the 3rd-order contribution. The tapped inductor is used to save the die area and, if the latter is no concern, it can be replaced by two inductors in series. $M_{\rm A}$ is biased in WI with a positive $g_{3\rm A}$ and $M_{\rm B}$ is biased in SI with a negative $g_{3\rm B}$. It can be shown that the contributions of $g_{1\rm A}$ and $g_{2\rm A}$ to the overall response of the amplifier are negligible. The purpose of connecting the $M_{\rm A}$ source to the tap of the inductor is to change the magnitude and phase of its $g_{3\rm A}$ contribution to IMD_3 relative to the $g_{2\rm B}$ and $g_{3\rm B}$ contributions of $M_{\rm B}$. With the proper selection of the tapping point, the FET gate widths and biases, the overall IMD_3 can be made near zero for a wide range of biases. One of the advantages of this approach is that it does not require the degeneration inductance to be minimized as in [5] and, therefore, it makes the simultaneous noise-power match possible. The other advantage is that IIP_3 is very insensitive to the input termination at the 2nd-harmonic frequency.

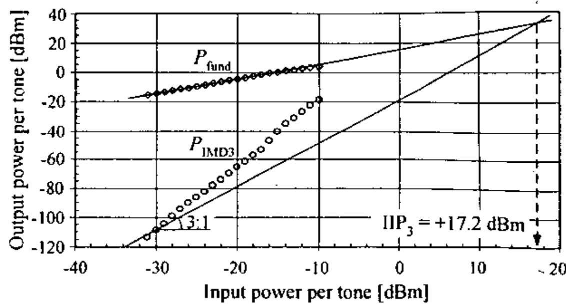

Fig. 4. Measured 2-tone transfer characteristics.

VI. Measured Results

The designed LNA was manufactured in a 0.25μm Si CMOS technology as part of a cellular CDMA zero-IF receiver and packaged in a QFN 32-pin package. Its measured power gain and NF are 15.5dB and 1.6dB respectively with the current consumption of 9mA from 2.6V excluding the bias circuit. The input and output return losses are lower than -11dB. The LNA IIP_3 was tested with two tones at 880MHz and 880.5MHz. The measured output powers of the fundamental and IMD_3 responses as functions of the input power per tone are plotted in Fig. 4. As can be seen, the $P_{IMD3}(P_{in})$ curve rises with a slope steeper than 3:1 at the measured power levels, which means that the composite 3rd-order nonlinearity is negligible and IMD_3 is dominated by the 5th and higher odd-order nonlinearites. As a result, IIP_3 is a function of P_{in}. At $P_{in} = -30$dBm, $IIP_3 = +17.2$dBm. We also measured IIP_3 for different values of the master reference current with the ratio I_{RA}/I_{RB} kept constant. Fig. 5 shows that the LNA maintains high IIP_3 in a wide range of the dc current through the composite FET. The achieved IIP_3 was verified to be insensitive to the input and output harmonic terminations.

We also manufactured an LNA with a single input FET. It achieved 16dB gain, +2dBm IIP_3 and 1.4dB NF with 9mA dc current. So, the proposed modified DS method boosted IIP_3 by about 15dB but degraded NF by 0.2dB due to the induced gate noise of the FET biased in WI. The NF degradation is a common drawback of all DS-based methods.

Table I compares the dynamic range figures of merit (FOM) defined as $OIP_3/[(\text{NoiseFactor-}1)\cdot P_{dc}]$ for this and other state-of-the-art FET LNAs. As can be seen, our LNA using the modified DS method has the highest FOM.

VII. Conclusions

We have shown that the conventional DS method does not provide a significant IIP_3 boost at RF due to the contribution of the 2nd-order nonlinearity to IMD_3. In general, the vector of this contribution is not collinear with the vector of the 3rd-order contribution and, therefore, they can not cancel each other. To give these contributions opposite phases, we proposed a modified DS method that uses a tapped inductor for source degeneration of the composite FET. This method boosted IIP_3 of the designed LNA by 15dB.

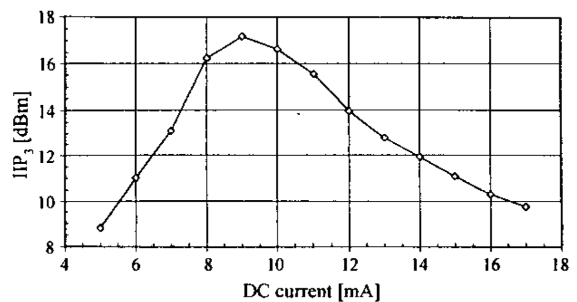

Fig. 5. Measured IIP_3 at $P_{in} = -30$dBm as a function of the combined dc current of the input FETs.

TABLE I
Comparison of State-of-the-Art Linear FET LNAs

Work	Technology	Freq GHz	S21 dB	NF dB	IIP_3 dBm	P_{dc} mA@V	FOM
This work	0.25μm Si CMOS	0.9	15.5	1.6	+17.2	9@2.6	179
[2]	0.25μm Si CMOS	0.9	14.6	1.8	+10.5	2@2.7	117
Ock 2002	0.6μm GaAs MESFET	0.9	17	1.6	+8.5	4.7@2.7	62.8
Youn 2003	0.25μm Si CMOS	2.2	14.9	3	+16.1	9.4@2.5	53.8
[5]	0.35μm Si CMOS	0.9	10	2.8	+15.6	7.8@2.7	19
[1]	0.35μm Si CMOS	0.9	2.5	2.8	+18	15@3	3

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