A High-Efficiency SiGe BiCMOS WCDMA Power Amplifier with Dynamic Current Biasing for Improved Average Efficiency

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Abstract — **This paper demonstrates a WCDMA single-stage power amplifier fabricated in a 0.25μm SiGe BiCMOS process. With dynamic biasing of the collector current, the average power efficiency is improved by more than a factor of two compared to a typical class AB power amplifier. The power amplifier satisfies the 3GPP Class-III WCDMA Adjacent Channel Power Ratio (ACPR) specifications (ACPR_5M=-33dBc and ACPR_10M=-58.8dBc) with 23.9dBm average channel output power. The measured output power at the 1dB compression point is 25.9dBm.**

Index Terms — **Silicon Germanium, power amplifiers, WCDMA, average power efficiency, dynamic biasing.**

I. Introduction

In recent years, Silicon Germanium (SiGe) has become a competitive candidate for the development of handset power amplifiers (PAs), since SiGe exhibits high efficiency, good linearity, high current gain, low-cost and compatibility with BiCMOS technology [1]. For WCDMA PA's, linearity and efficiency are the most critical design parameters. Moreover, average power efficiency (over the full range of output powers), instead of peak power efficiency, is the key factor determining the talk time and battery lifetime for portable wireless applications [2]. Previous efforts using dynamic biasing techniques [3]-[5] did achieve improved average power efficiency, but their power gains changed dramatically when switched from the high-power region into the low-power region, which can create problems in the power control loop operation of the CDMA handset. For Class-III WCDMA handsets, +24dBm maximum output power (+1/-3dB tolerance) and –33dBc ACPR at the highest output power are required [6]. Besides satisfying the above specifications, our approach may substantially increase the average power efficiency, while keeping the power gain roughly constant.

The principle of dynamic current biasing is introduced in Section II, and the detailed design approach is discussed in Section III. Measurement results are shown in Section IV.

II. Dynamic Current Biasing

A. Average Power Efficiency

The average power efficiency is a measure of the ratio of the total energy transmitted to the total energy drawn from the battery [2], i.e.,

$$\langle \eta \rangle = \frac{\langle P_{out} \rangle}{\langle P_{out} \rangle} = \frac{\int P_{out} p(P_{out}) dP_{out}}{\int \frac{P_{out} p(P_{out}) dP_{out}}{\eta(P_{out})}}. \quad (1)$$

Where P_{out} is the output power, $p(P_{out})$ is probability of a certain output power P_{out}, and $\eta(P_{out})$ is the power-added efficiency at P_{out}. The average output power of a CDMA handset is well below the peak output power, where efficiency is a maximum, so it is very desirable to improve the PAE of the amplifier at lower output powers. For ideal Class-A power amplifiers, the average power efficiency (over representative CDMA conditions) is roughly 1.3% [7]. Therefore, improving average power efficiency is one of the key objectives for future power amplifiers.

B. Dynamic Current Biasing

The typical approaches for reducing dc power consumption at lower output powers are reducing either DC bias current through dynamic current biasing (DCB) or DC bias voltage (DVB) (as shown in Fig. 1) or both.

Power amplifiers with dynamic current biasing (DCB) have been proposed [3]-[4], but their power gain changes by more than 10 dB over the range of current variation,. With the decrease of input power, the current swing at the output also becomes smaller and the total bias current can be reduced. However the current density of each transistor drops, resulting in a power gain reduction for the whole power amplifier circuitry. The power gain of the amplifier (including the effects of source impedance and load impedance) is:

$$Gp = \frac{4R_S}{(R_S + r_b)^2} \cdot \left(\frac{\omega_T}{\omega}\right)^2 \cdot \frac{R_L}{(1 + \omega_T R_L C_{je})^2}. \quad (2)$$

Where R_s is the source impedance, r_b is the base resistance, and $_T$ is the unity current gain radian frequency. This illustrates the need to keep the current density of the transistor roughly constant (and hence the f_T constant) even as the current is lowered.

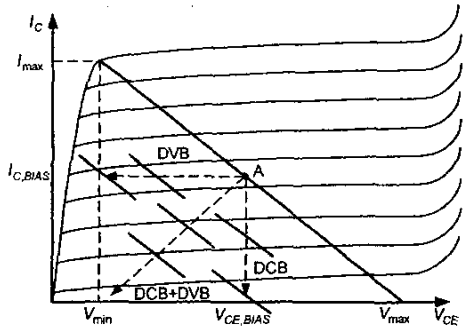

Fig. 1 BJT current versus voltage, demonstrating different dynamic biasing strategies (DC/VB: dynamic current/voltage biasing).

To lower the collector current and keep the power gain roughly constant, we utilize low-loss MOS switches to dynamically bias the SiGe HBTs [8], as depicted in Fig. 2.

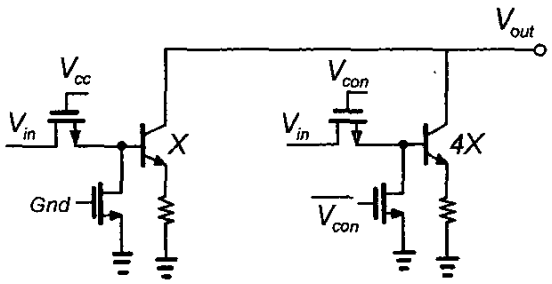

Fig. 2 Output stage with dynamic current biasing. HBTs are biased "on" or "off" in response to output power requirements.

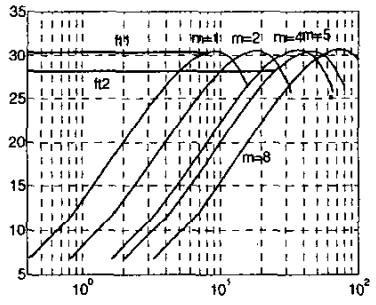

Fig. 3 Simulated HBT cutoff frequency versus collector current with differing device sizes (single device: 25μm²; m represents the number of devices in parallel).

The number of "on" transistors is adjusted in response to changes in the output power; the collector current density increases slightly at the low power region so as to keep power gain constant. As shown in Fig. 3, the power amplifier shifts to a higher transition frequency (ft1) in low power mode, nevertheless it operates at a lower transition frequency (ft2) in high power mode. Operating the transistor at higher transition frequency enables us to keep the gain relatively constant by overcoming the effects of the extra parasitics in low power mode.

III. Design Considerations

Ideally, the dc bias current would change continuously in response to the input power, but it is simpler to vary the current in discrete steps. Simulation results show that a single step variation in dc bias provides the best tradeoff of average power efficiency and circuit complexity. In our case, the high power mode consisted of 100 parallel devices, and the low-power mode consisted of 20 devices. Each bipolar transistor emitter is 0.44μm by 48μm.

The simplified equivalent input circuit is shown in Fig. 4. The NFET switches at the bases of transistors will reduce the power gain. The gain loss can be expressed as:

$$\Delta Gain = \Delta Gain\_R_{MOS} + \Delta Gain\_C_{MOS} \quad (3a)$$

$$\approx 10\log\frac{R_{in}^2}{(R_{MOS}+R_{in})^2}. \quad (3b)$$

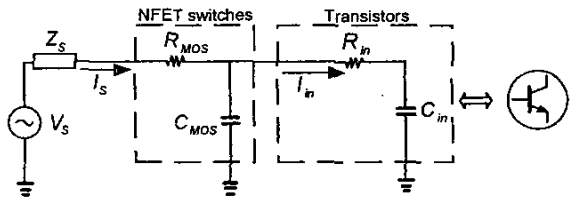

Fig. 4 Equivalent input circuit. For 100 parallel devices, R_{MOS}=0.3ohm, C_{MOS}=3.26pF, Rin=1ohm, and Cin=204pF.

The effects of the NFET switch size on both power gain and 1dB compression point of the power amplifier were simulated. The results are shown in Fig. 5. There are two sources for power loss: series resistance loss and shunt capacitance loss. Based on the simulation results that match the expression in (3b), an optimum MOS switch size of 3 finger × 15μm × 0.26μm was chosen. The corresponding gain loss at 1.95GHz was 2.5dB.

The bias network consists of a β helper and a low impedance buffer, as shown in Fig. 6. This topology

provides a constant voltage biasing to the base of the power amplifier and also terminates the sub-harmonic ($\Delta\omega$) frequency at the input, to improve the overall linearity [9]. In order to effectively terminate the sub-harmonic component, the buffer needs to satisfy certain bandwidth requirements. For WCDMA handset power amplifiers, the channel bandwidth is 3.84MHz, so the minimum bandwidth of the bias network has to be larger than 3.84MHz. Simulation shows $Z_{Bias}(\Delta\omega) \approx 0,\ \Delta\omega \leq 5MHz$.

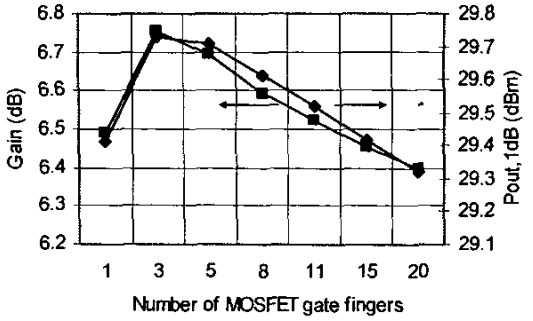

Fig. 5 Effects of gate finger on Gain and 1dB compression. Each finger is 15μmx0.25μm finger and the HBT is 0.44μm by 48μm.

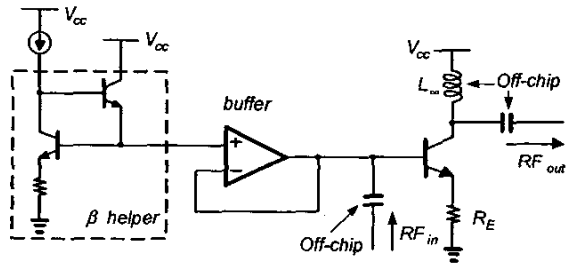

Fig. 6 Power amplifier bias schematic.

IV. Measurement Results

The single-stage power amplifier was fabricated in the 0.25μm IBM BiCMOS 6HP process [10]. The chip size, including the bias network, is 0.9mm×1.2mm. The die photograph is shown in Fig. 7. The devices were tested in Micro Lead Frame (MLF12) packages. The output matching network (OMN) is implemented off-chip to achieve high Q for optimum PAE.

Fig. 8 compares the measured DC currents for different biasing approaches for a single-stage WCDMA power amplifier, superimposed on a typical probability distribution function for the output power [2]. These approaches include constant base voltage (CV) biasing with a fixed number of parallel transistors and DCB with a fixed base voltage. Using (1), average power efficiencies are calculated as 2.5% for CV biasing and 8.0% for DCB – a substantial improvement with the new approach.

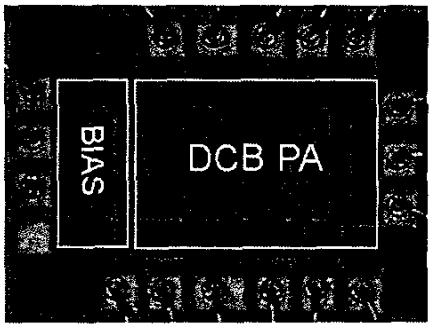

Fig. 7 Photo of DCB SiGe HBT power amplifier die.

Fig. 9 compares the measured gain variation between DCB and CV. The gain change for DCB is less than 2dB, and is much more constant than DCB where the number of HBTs is fixed and the current density per device is reduced to vary the current.

The linearity of the DCB amplifier is measured for a WCDMA signal in Fig. 10, and the circuit satisfies the 3GPP Class-III WCDMA ACPR specification with 23.9dBm channel output power.

Fig. 11 shows measured power added efficiencies (PAEs) with DCB and CV approaches. The peak PAE is not as high as other III-V WCDMA amplifiers reported [11], but the average power efficiency is improved, based on DC current data given for those amplifiers.

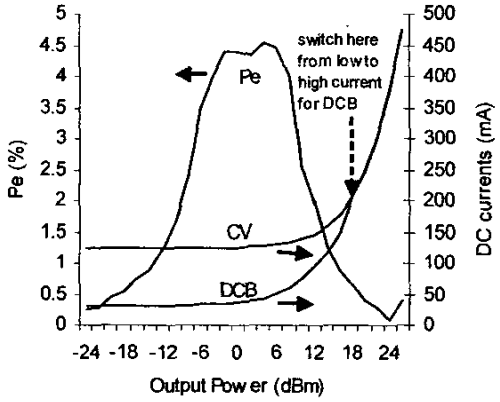

Fig. 8 Output power probability distribution Pe and measured DC current comparison for different biasing techniques. The switch point from 100 devices to 20 devices occurs at Pout = 18 dBm. V_{cc}=3V.

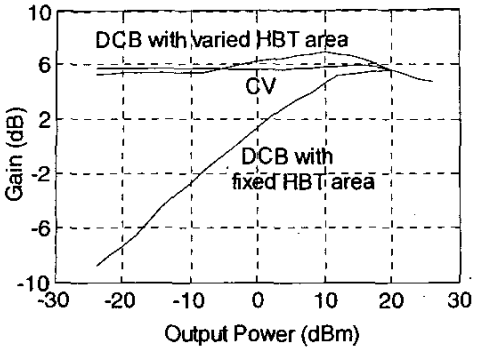

Fig. 9 Measured power gain with CV, DCB with varied HBT area and DCB with fixed HBT area power amplifier.

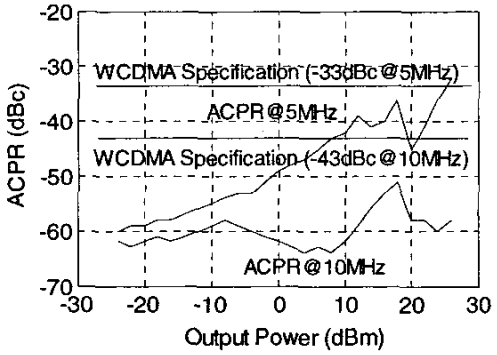

Fig. 10 Measured ACPRs of DCB SiGe HBT power amplifier.

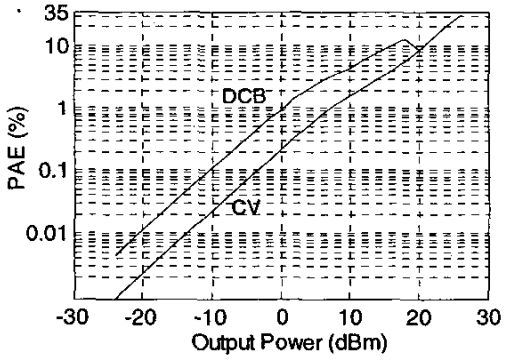

Fig. 11 Measured power added efficiencies (PAEs) with CV and DCB power amplifier.

V. Conclusions

An integrated single-stage power amplifier chip with dynamic current biasing for WCDMA applications was fabricated and measured. The measured 1dB compression point is 25.9dBm, and peak PAE is 31%. The average power efficiency is improved from 2.5% to 8.0%. The power amplifier satisfies the ACPR specification for uplink with 23.9dBm channel output power.

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References

[1] J. Pusl, S. Sridharan, P. Antognetti, D. Helms, A. Nigam, J. Griffiths, K. Louie, M. Doherty, "SiGe Power Amplifier ICs with SWR Protection for Handset Applications", *Microwave Journal*, June 2001

[2] J. F. Sevic, "Statistical characterization of RF power amplifier efficiency for CDMA wireless communication systems", in *Wireless Communications Conference*, pp.110-113, Aug 1997

[3] D. Dening, "Setting Bias Points For Linear RF Amplifiers", *Microwaves & RF*, pp.71-78, June 2002.

[4] T. Fowler, K. Burger, N. S. Cheng, A. Samelis, E. Enobakhare, and S. Rohlfing, "Efficiency Improvement Techniques at Low Power Levels for Linear CDMA and WCDMA Power Amplifiers", *IEEE Radio Frequency Integrated Circuits Symposium*, 2002, pp. 41-44

[5] G. Hanington, P. Chen, P. M. Asbeck, L. E. Larson, "High-efficiency power amplifier using dynamic power-supply voltage for CDMA applications", *Microwave Theory and Techniques, IEEE Transactions on*, vol. 47, pp. 1471-1476, Aug 1999.

[6] 3GPP TS 25.101, V5.3.0, June 2002.

[7] P. Asbeck, Private Communication.

[8] M. Rofougaran, A. Rofougaran, C. Olgaard, A. A. Abidi, "A 900 MHz RF Power Amplifier with Programmable Output", *Digest of Technical Papers, 1994 Symposium on VLSI Circuits*, pp. 193-194, June 1994.

[9] V. Aparin, C. Persico, "Effect of out-of-band terminations on intermodulation distortion in common-emitter circuits", *Microwave Symposium Digest, 1999 IEEE MTT-S International*, vol. 3, pp. 977-980, June 1999.

[10] S. A. St. Onge, D. L. Harame, J. S. Dunn, S. Subbanna, D. C. Ahlgren, G. Freeman, B. Jagannathan, J. Jeng, K. Schonenberg, K. Stein, R. Groves, D. Coolbaugh, N. Feilchenfeld, P. Geiss, M. Gordon, P. Gray, D. Hershberger, S. Kilpatrick, Johns, "A 0.24 μm SiGe BiCMOS mixed-signal RF production technology featuring a 47 GHz ft HBT and 0.18 μm Lett CMOS", *1999 BCTM*, pp. 117-120, Sept 1999.

[11] Y. Bito, T. Kato, N. Iwata, "High efficiency power amplifier module with novel enhancement-mode heterojunction FETs for wide-band CDMA handsets", *Gallium Arsenide Integrated Circuit (GaAs IC) Symposium, 2000*, pp. 255-258, Nov 2000.